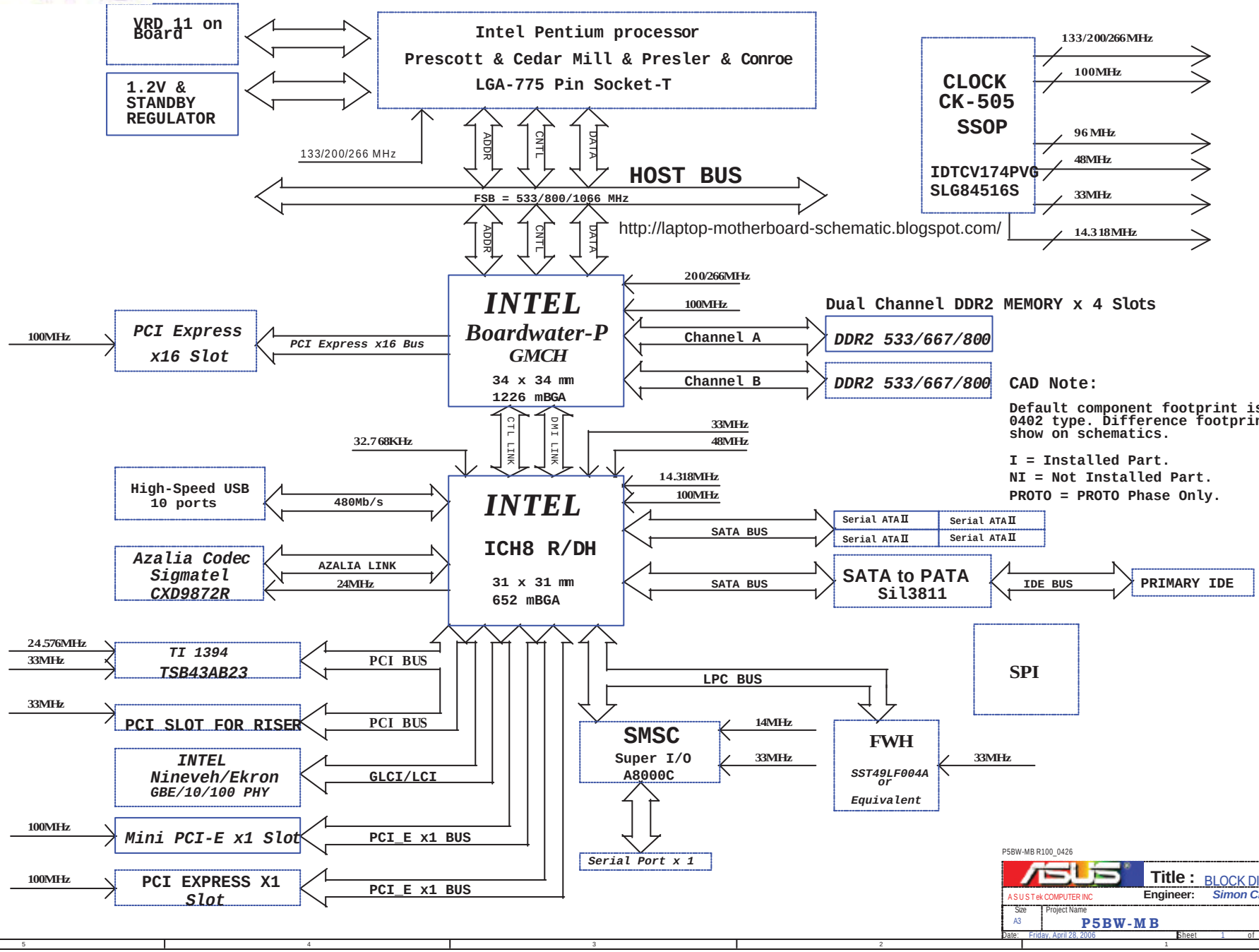
P5BW-MB *Revision: 1.00 -- (03/29/2006)*



P5BW-MB R100_0426

ASUSTek COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: Simon Chang

Size	Project Name	Rev
A3	P5BW-MB	1.00

Date: Friday, April 28, 2006 Sheet 1 of 55

ASUS ECN Control Table

ECN Document Number	DATE	Schematics Revision	BOM Part Number	PCBA Revision	PCB Revision

ASUSTeK COMPUTER INC	Title : ECN CONTROL		
	Engineer: Simon Chang		
Size: A3	Project Name: P5BW-MB		Rev: 1.00
Date: Friday, April 28, 2006	Sheet 2 of 55		

Schematics Change History

Version	Comments
1.00	First release for EVT.

PAGE REF. LIST

PAGE	TITLE
01	BLOCK DIAGRAM
02	ECN CONTROL TABLE
03	GHANGE HISTORY
04	CLOCKS DISTRIBUTION
05	RESET MAP
06	POWER DISTRIBUTION
07	POWER FLOW
08	POWER SEQUENCE
09	CLOCK CK505
10~13	INTEL CONROE CPU 1 - 4
14~20	BROADWATER 1 - 7
21	DDR2 - CHANNEL A
22	DDR2 - CHANNEL B
23	DDR2 - TERMINATION A&B
24	PCI EXPRESS X 16
25~29	ICH8 1-5
30	RTC/COM/KB/MS CIRCUIT
31	SATA CON
32	USB2.0 CONNECTOR
33	USB POWER
34	AUDIO CONNECTOR & MDC
35	PCI EXPRESS X 1
36	PCI SLOT
37	MINI PCIE CON
38	IEEE 1394 CONNECTOR
39	TI IEEE 1394
40~41	LAN NINEVEH & EKRON
42	LAN+USB CON
43	SMSC SIO A8000C
44	SPI FLASH
45	Sil3811 SATA-PATA Bridge
46	+1.8_DUAL & VTT_DDR
47	VCORE CONTROLLER
48	VCORE_DRIVERS
49	+1.25V GMCH CORE
50	+3V_DUAL & +5V_DUAL & +3VSB
51	1.25V_DUAL1.05V_ICH1.5VICH
52	ATX POWER CONNECTOR
53	FAN CONTROL
54	SONY CONTROL_PANNEL
55	EMI CAP.

ASUS

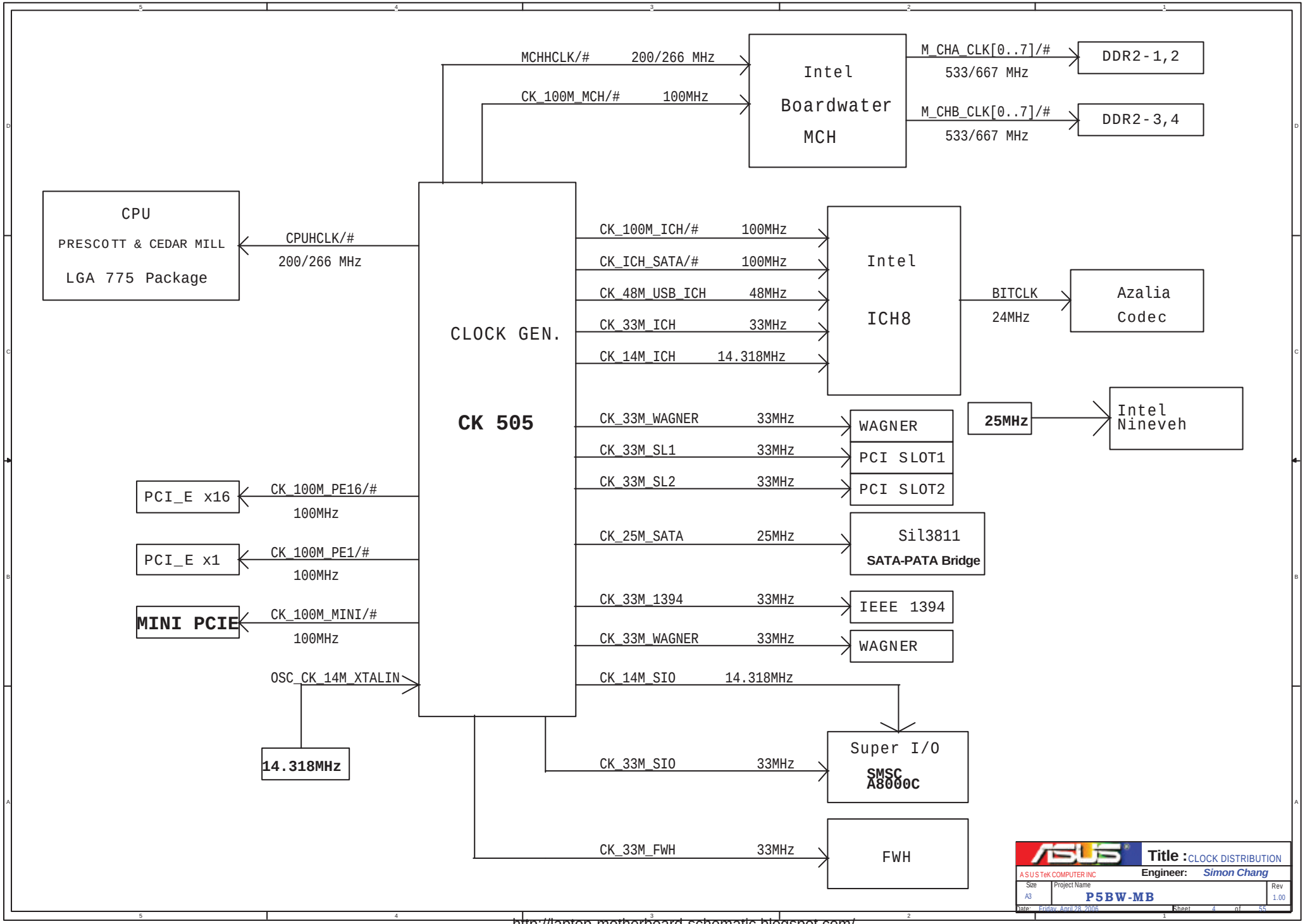
Title : CHANGE HISTORY

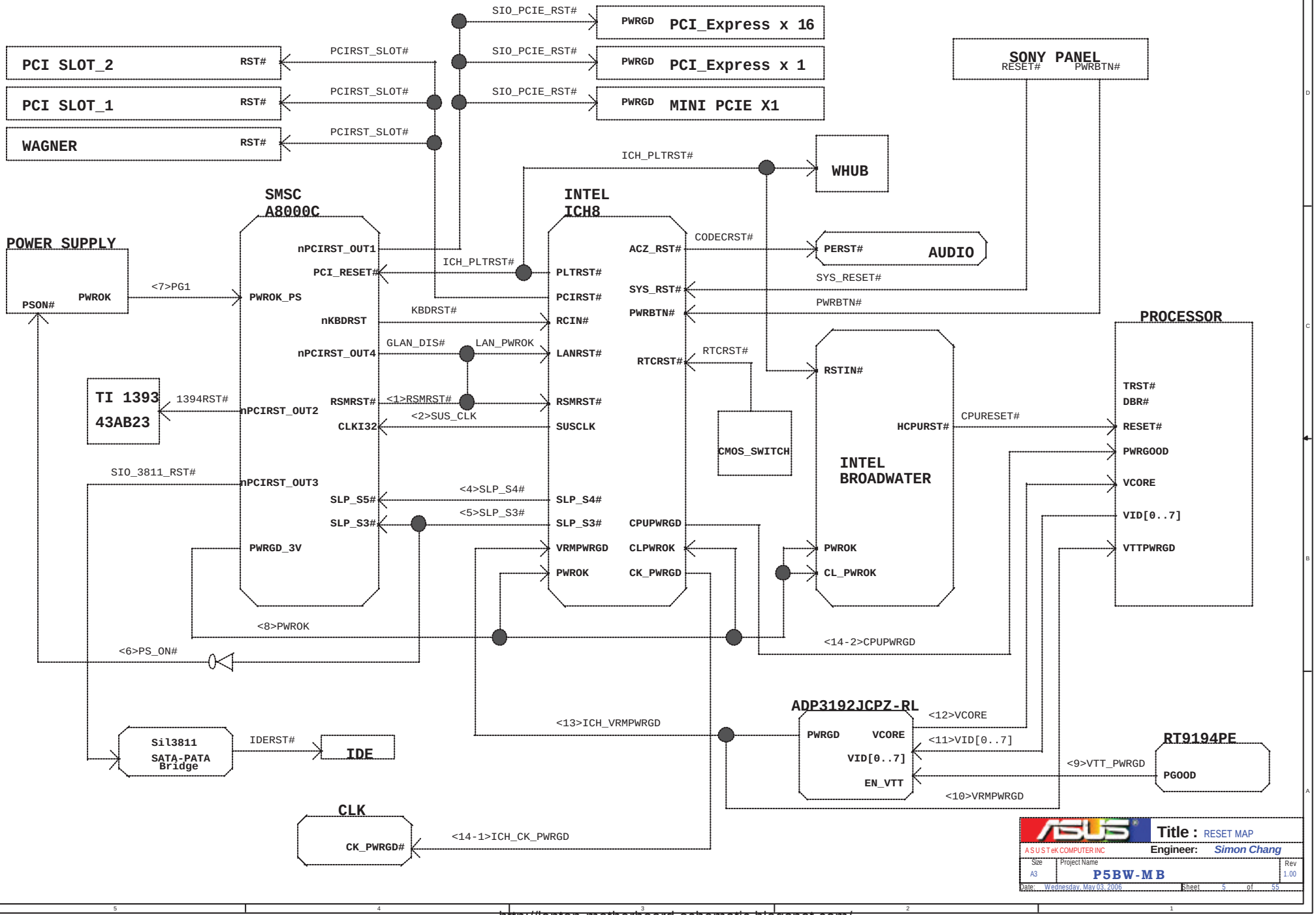
A S U S TeK COMPUTER INC.

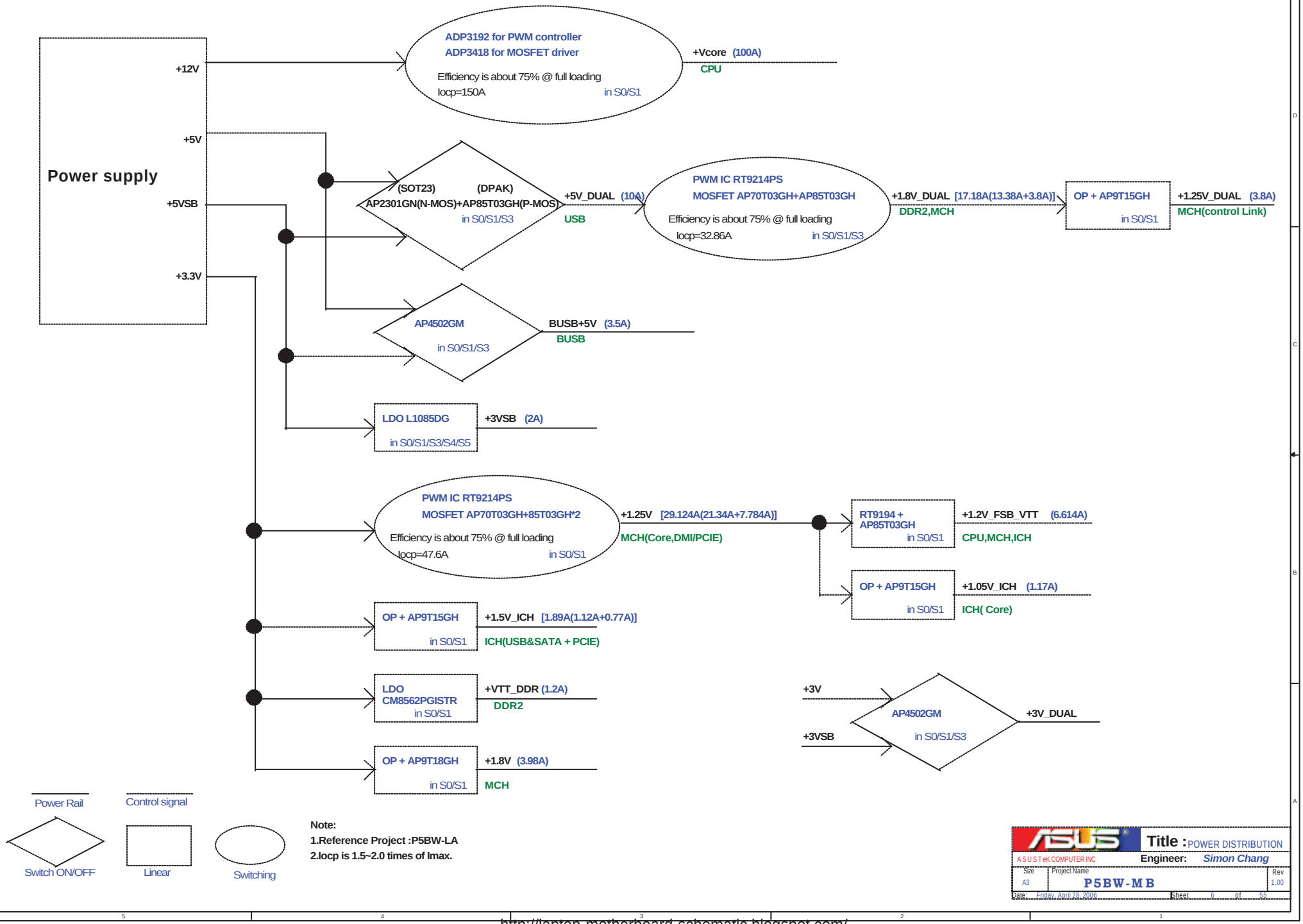
Engineer: Simon Chang

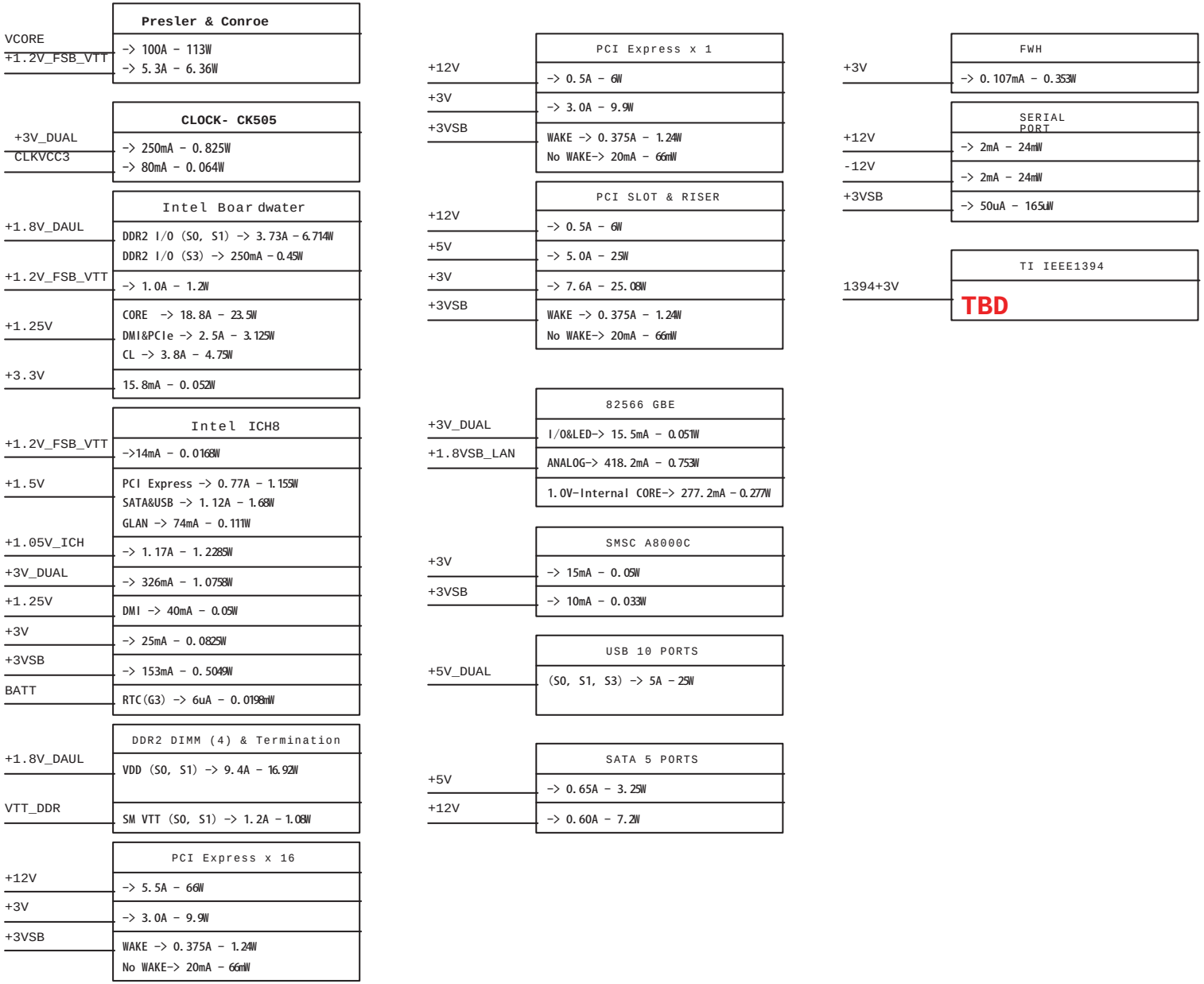
Size	Project Name	Rev
A3	P5BW-MB	1.00

Date: Thursday, May 04, 2006 Sheet 3 of 55

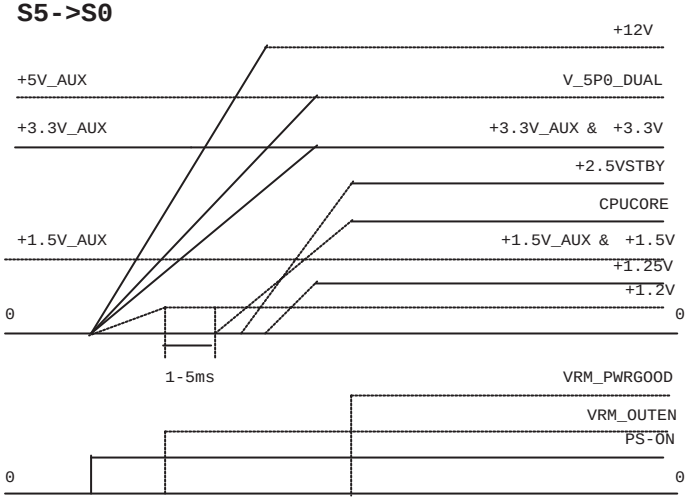




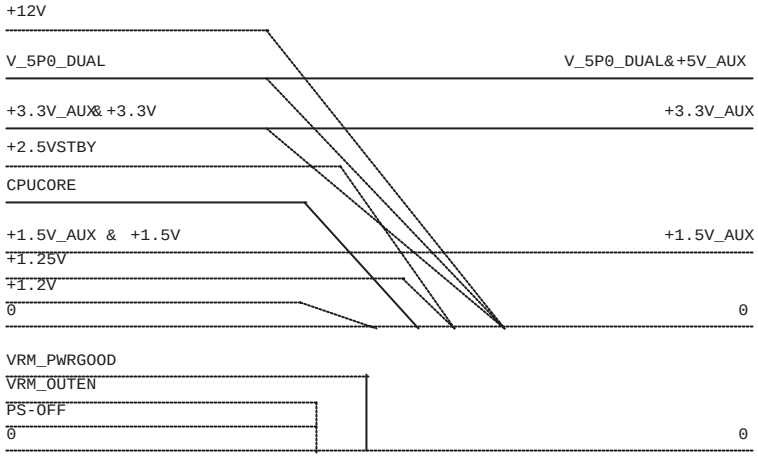




S5->S0

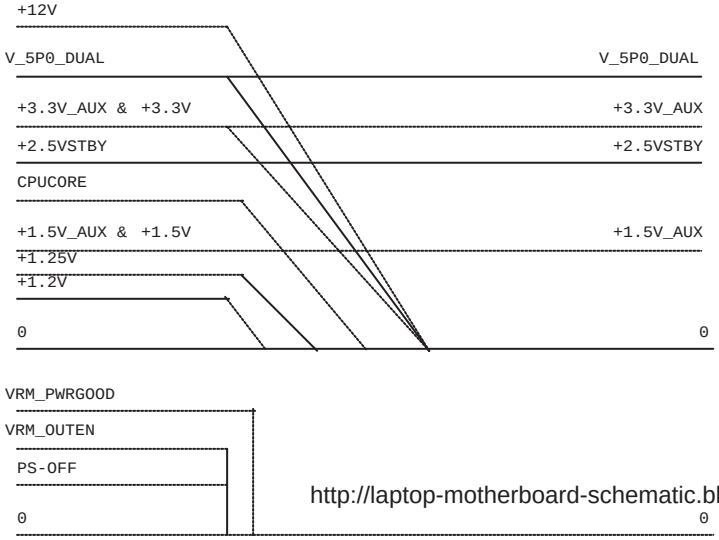


S0->S5

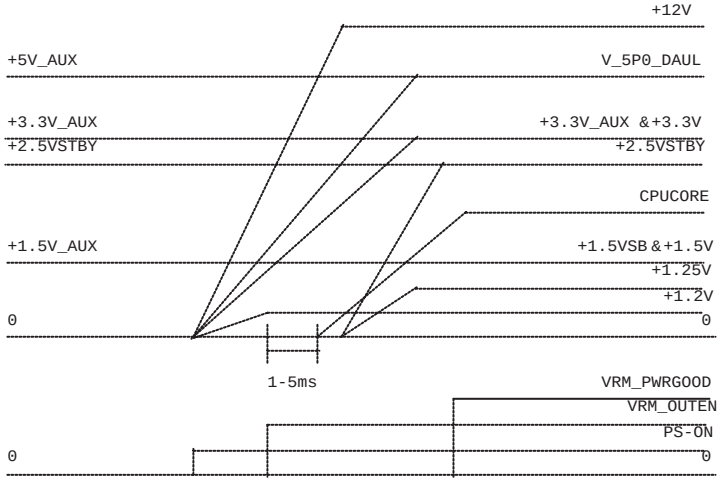


1.CPUCORE must rise after the voltage across 90% of +1.2V,andthe interval is within 1-5ms
2.VRM_OUTEN rises after the voltage across 90% of its specified value

S0->S3



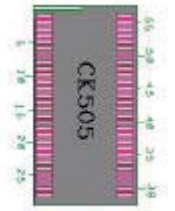
S3->S0



1.CPUCORE must rise after the voltage across 90% of +1.2V,andthe interval is within 1-5ms
2.VRM_OUTEN rises after the voltage across 90% of its specified value

S0: Windows Running+12V,V_5P0_DUAL,+3.3V,+3.3V_AUX,+2.5VSTBY,CPUCORE,+1.5V,+1.5V_AUX,+1.25V,+1.2V existed
S3: Windows StandbyV_5P0_DUAL,+3.3V_AUX,+1.5V_AUX,+2.5VSTBY existed
S5: AC Power On Only+5V_AUX,+3.3V_AUX,+1.5V_AUX existed

ASUSTeK COMPUTER INC	Title : POWER SEQUENCE	
	Engineer: Simon Chang	
Size: A3	Project Name: P5BW-MB	Rev: 1.00
Date: Friday, April 28, 2006	Sheet 8 of 55	



U1

FSBSEL2	FSBSEL1	FSBSEL0	CPU
0	0	0	266
0	1	0	200
0	0	1	133

TME(Trust Mode Enable):
0: Over clock enable
1: Over clock disable

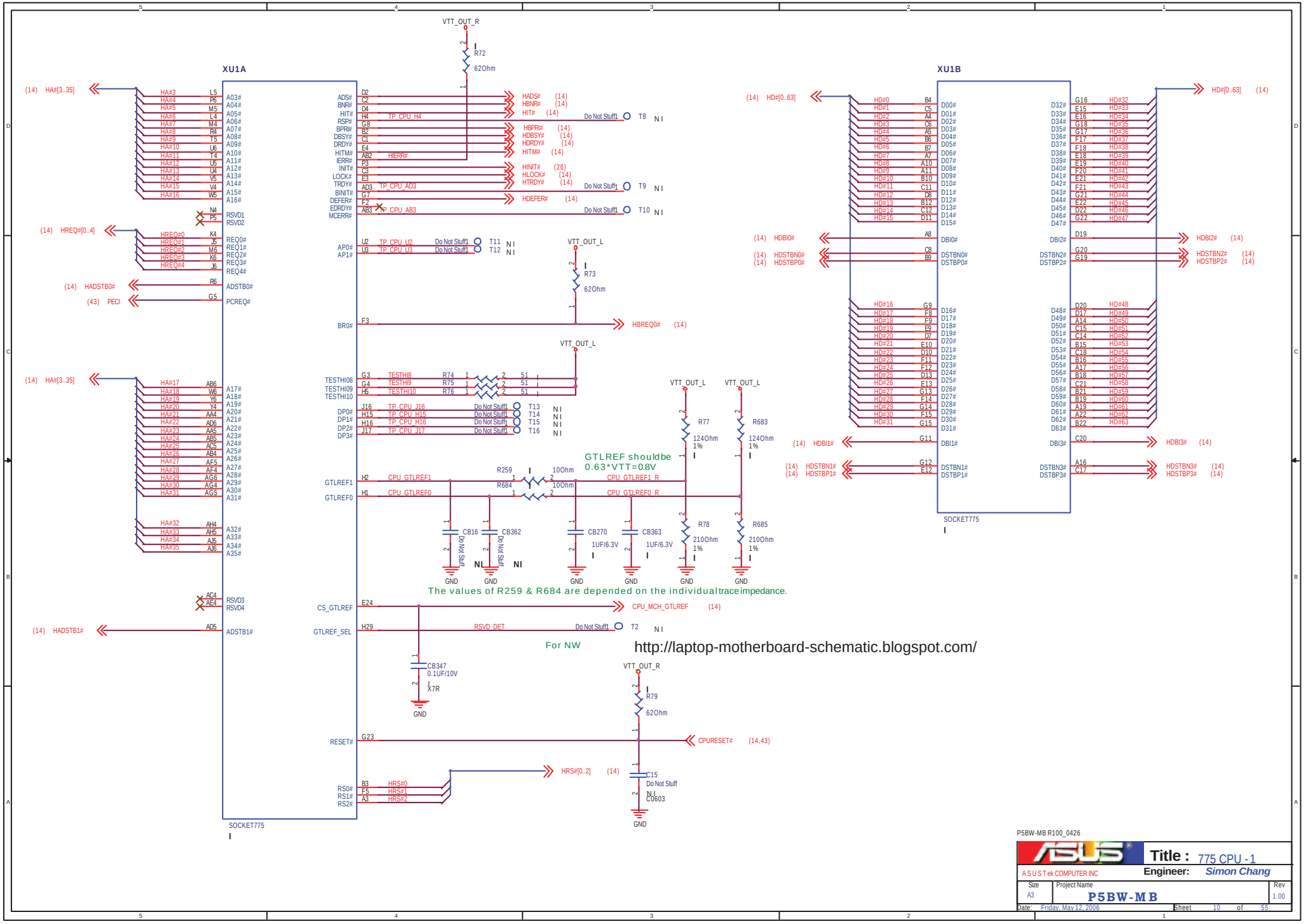
ITP_EN:
1: CPU_ITP
0: SRCCLK

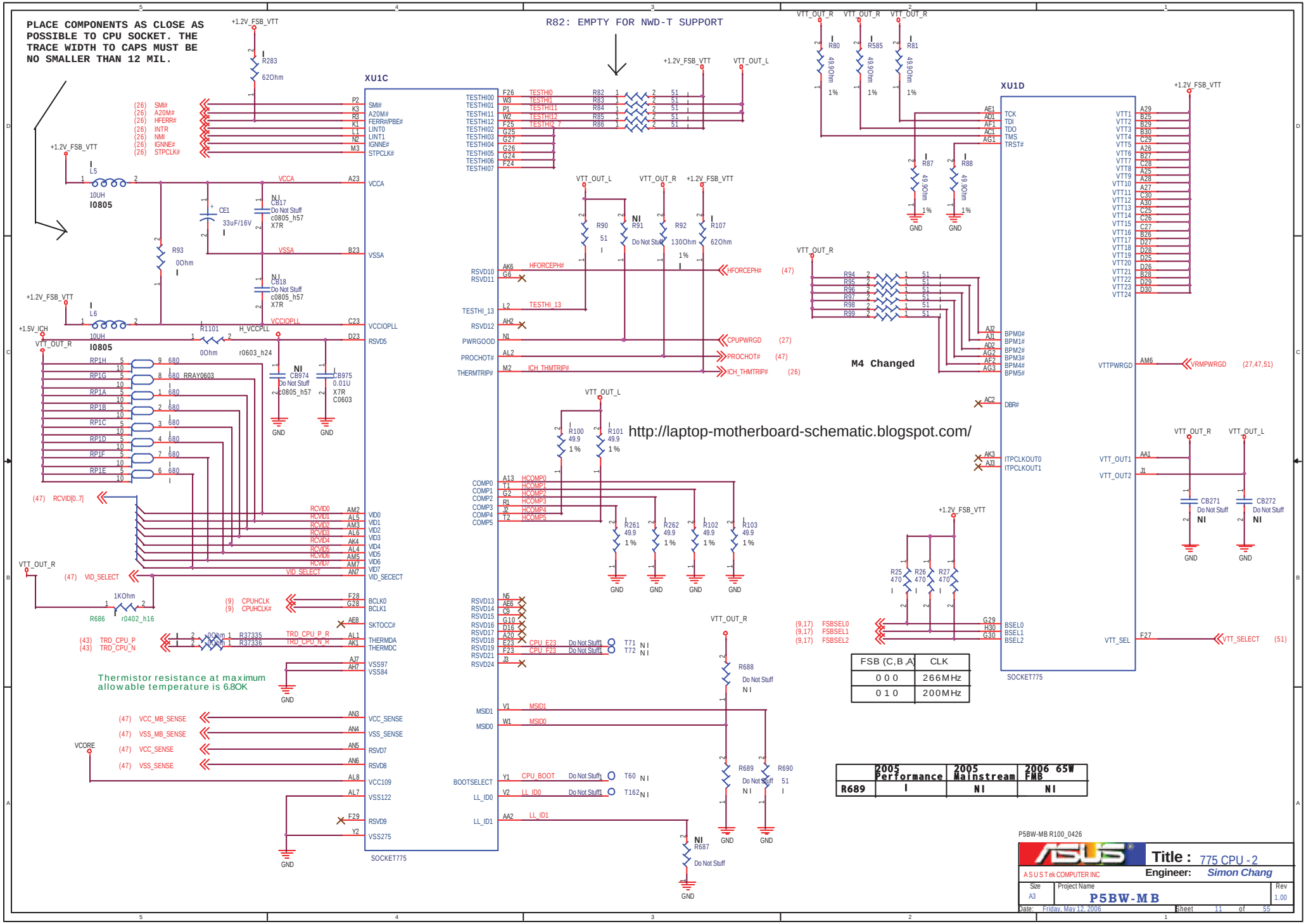
TEST_SEL:
0: NORMAL
1: TEST MODE

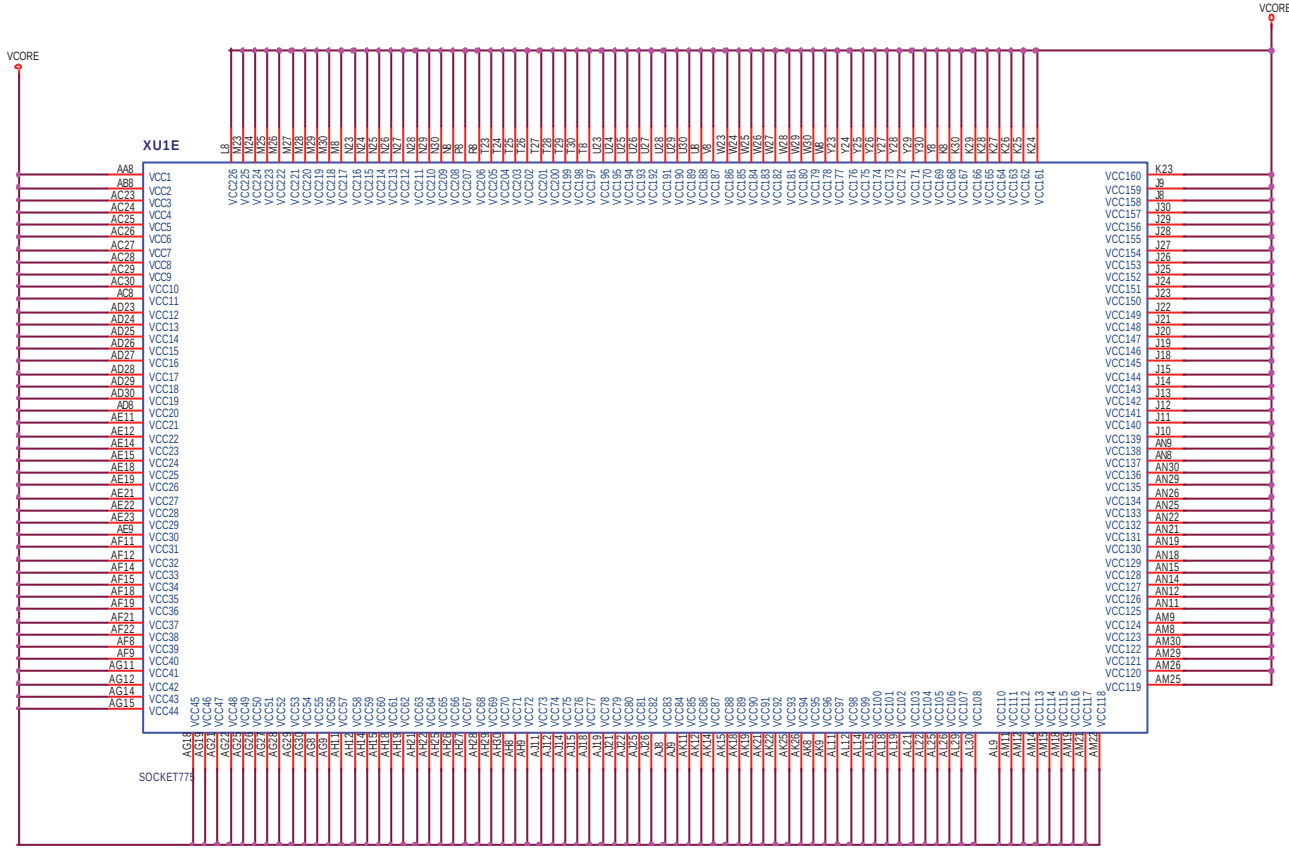
http://laptop-motherboard-schematic.blogspot.com/

SLG84516S SSOP56 : 06G011377011
IDTCV174PVG SSOP-56 : 06G011358021
CY505YC56DST SSOP-56: 06G011368031

Title :	CLOCK CK505
ASUSTeK COMPUTER INC	Engineer: Simon Chang
Size: A3	Project Name: P5BW-MB
Rev: 1.00	
Date: Friday, May 12, 2006	Sheet 9 of 55

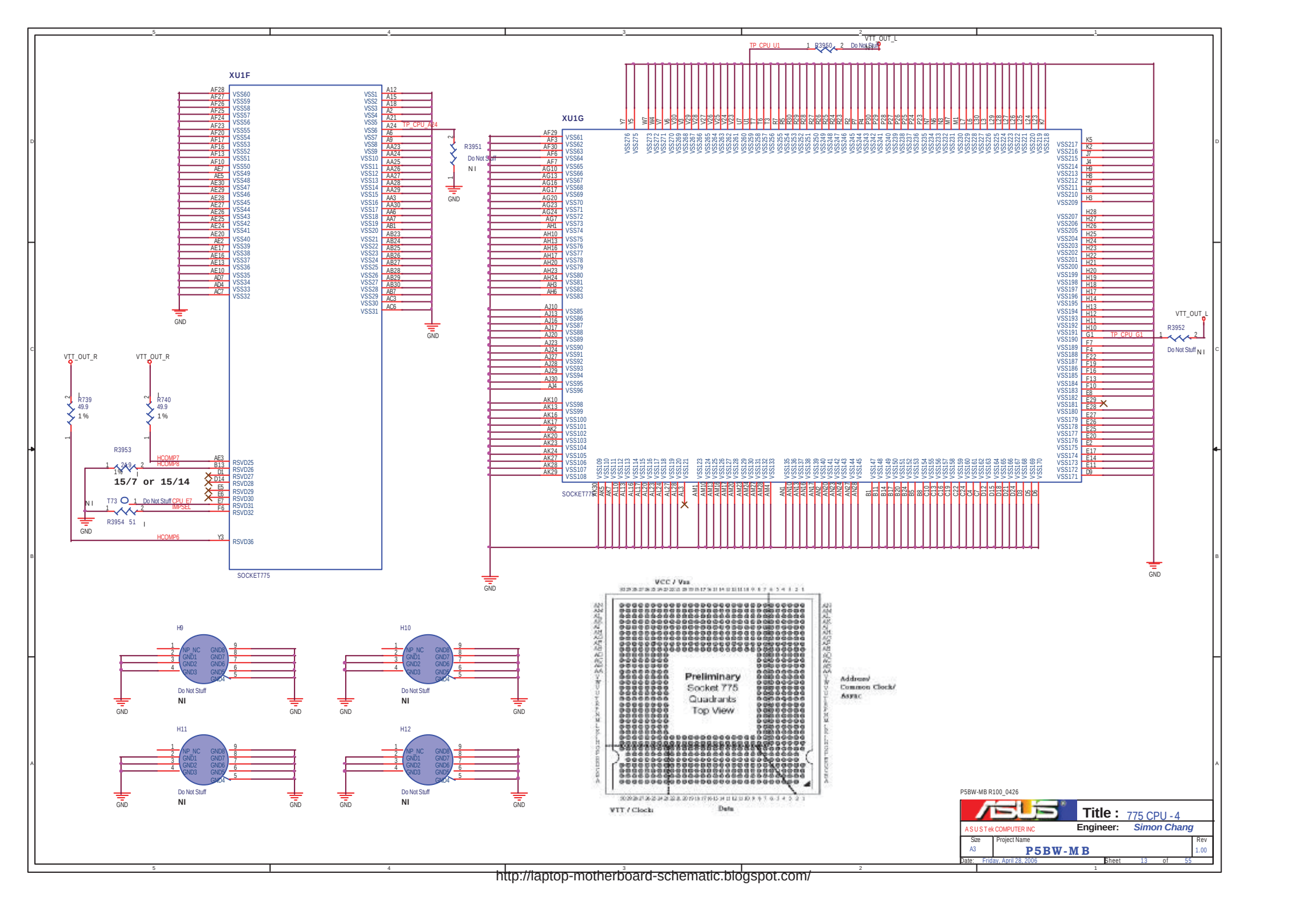

XU1A
XU1B
SOCKET775
VTT_OUT_R
R72
62Ohm
VTT_OUT_L
R73
R74
R75
R76
51
R77
R683
124Ohm
1%
R78
R685
210Ohm
R259
R684
10Ohm
CB616
CB362
CB270
CB363
1UF/6.3V
Do Not Stuff
NI
GND
GTLREF shouldbe
0.63*VTT=0.8V
The values of R259 & R684 are depended on the individual trace impedance.
For NW
http://laptop-motherboard-schematic.blogspot.com/
CB347
0.1UF/10V
X7R
R79
C15
Do Not Stuff
C0603
P5BW-MB R100_0426
Title : 775 CPU - 1
ASUSTek COMPUTER INC
Engineer: Simon Chang
Size A3
Project Name P5BW-MB
Rev 1.00
Date: Friday, May 12, 2006
Sheet 10 of 55

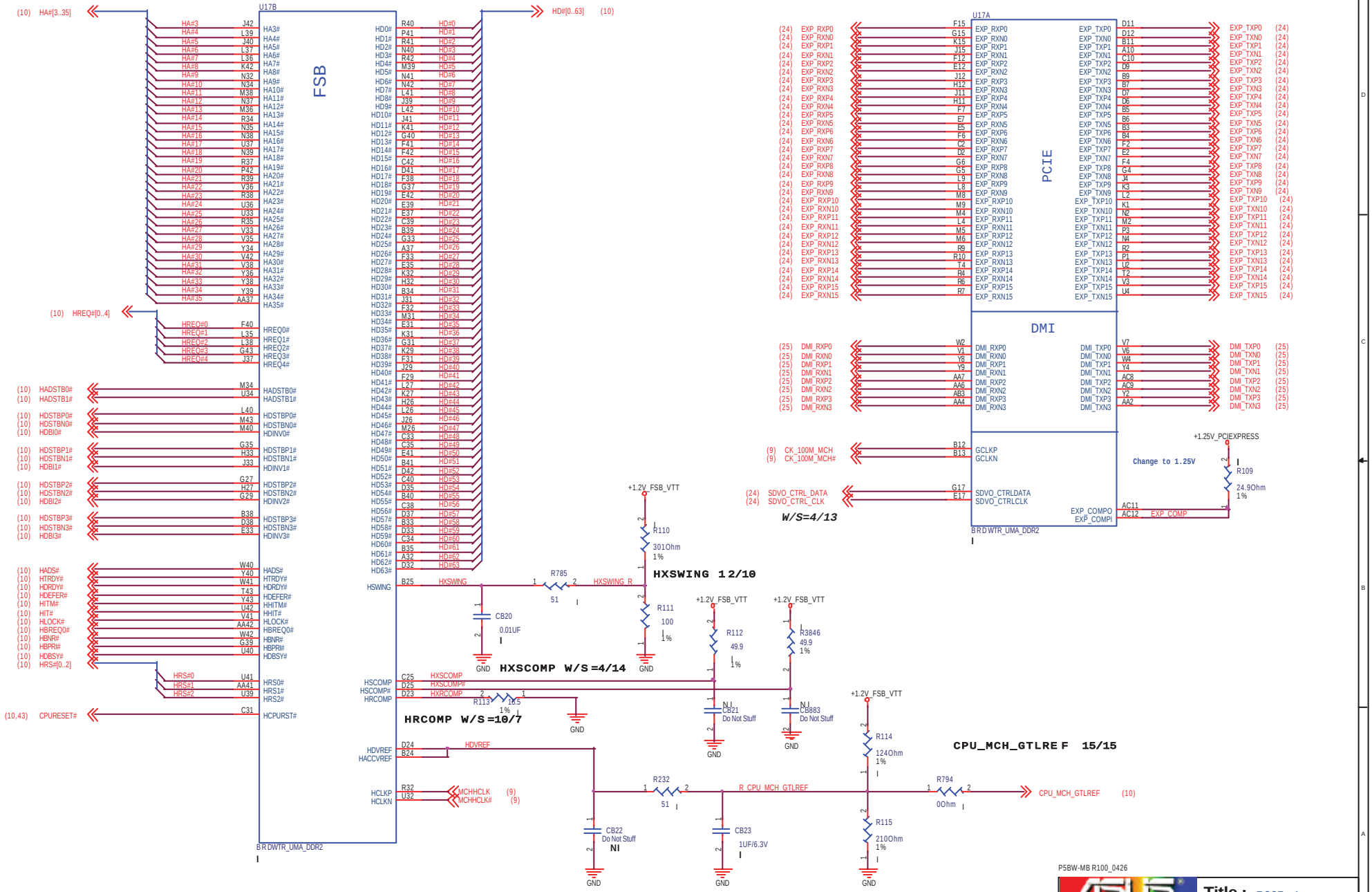

PLACE COMPONENTS AS CLOSE AS POSSIBLE TO CPU SOCKET. THE TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12 MIL.
R82: EMPTY FOR NWD-T SUPPORT
XU1C
XU1D
SOCKET775
M4 Changed
http://laptop-motherboard-schematic.blogspot.com/
Thermistor resistance at maximum allowable temperature is 6.8OK
FSB (C,B,A) CLK
000 266MHz
010 200MHz
2005 Performance
2005 Mainstream
2006 65W FMB
R689
Title : 775 CPU -2
ASUSTek COMPUTER INC
Engineer: Simon Chang
P5BW-MB
Project Name
Size
Rev
Date: Friday, May 12, 2006
Sheet 11 of 55



P5BW-MB R100_0426

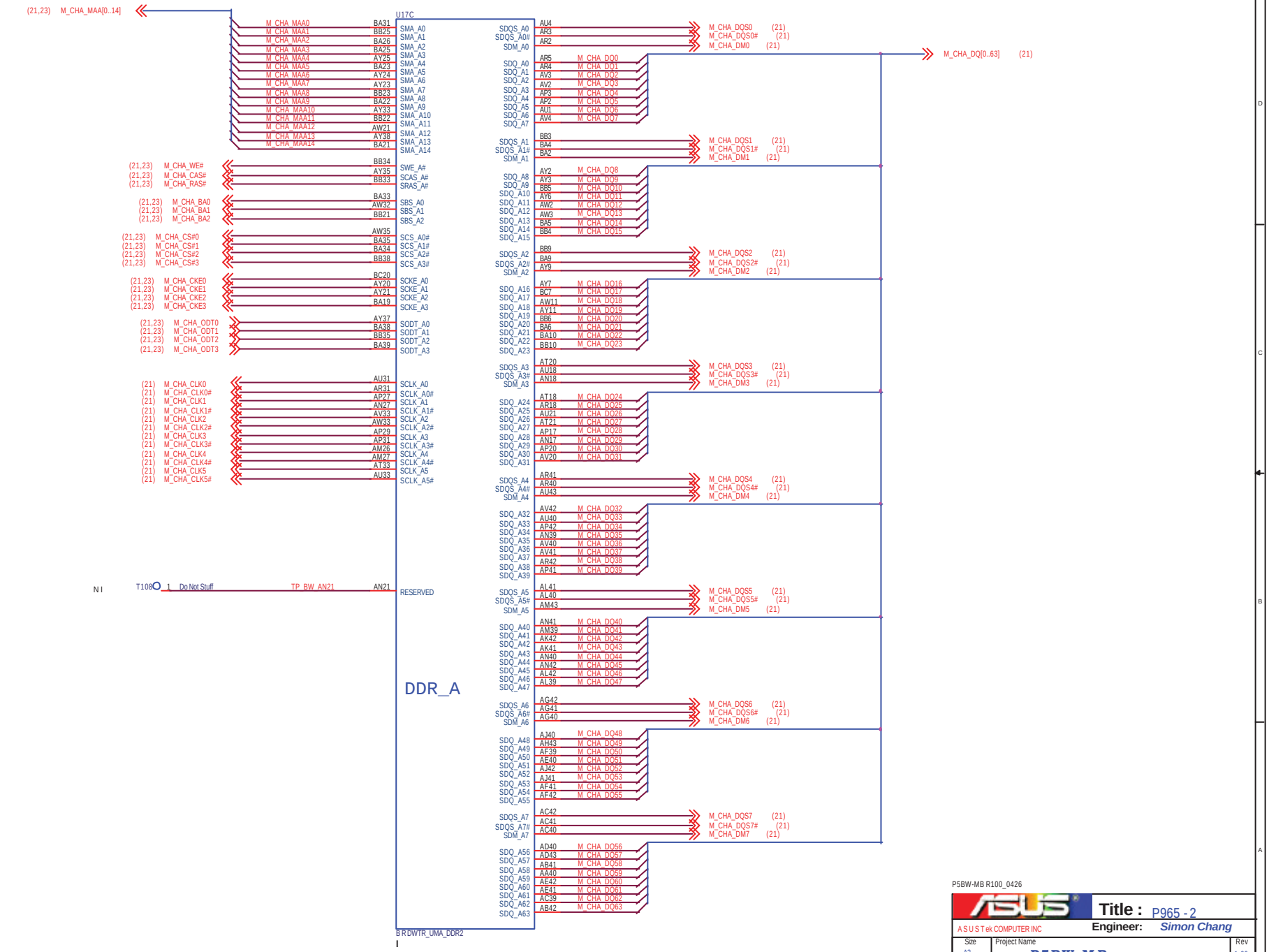
ASUSTek COMPUTER INC	Title : 775 CPU - 3	
	Engineer: Simon Chang	
Size: A3	Project Name: P5BW-MB	Rev: 1.00
Date: Friday, April 28, 2006	Sheet 12 of 55	

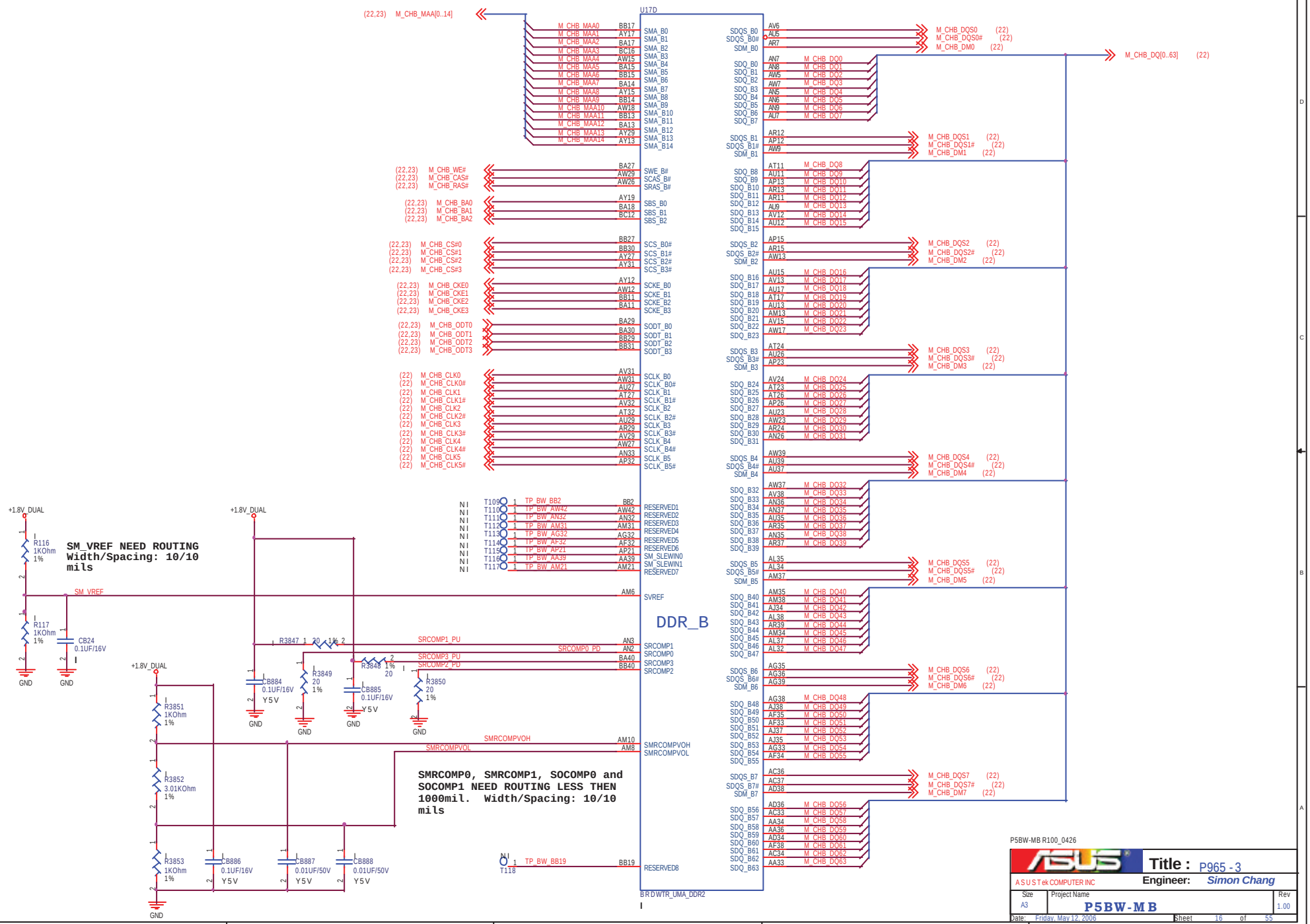


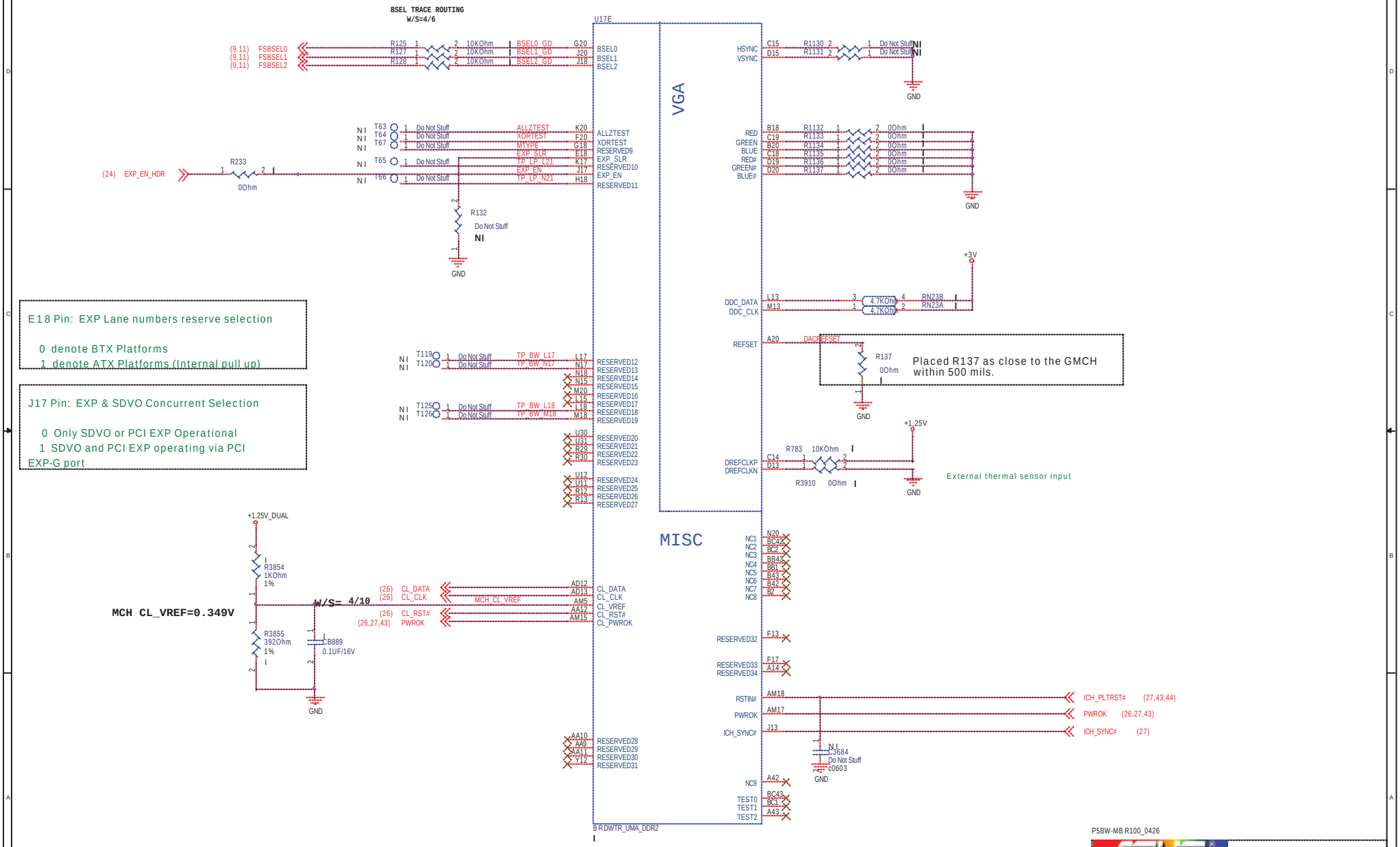


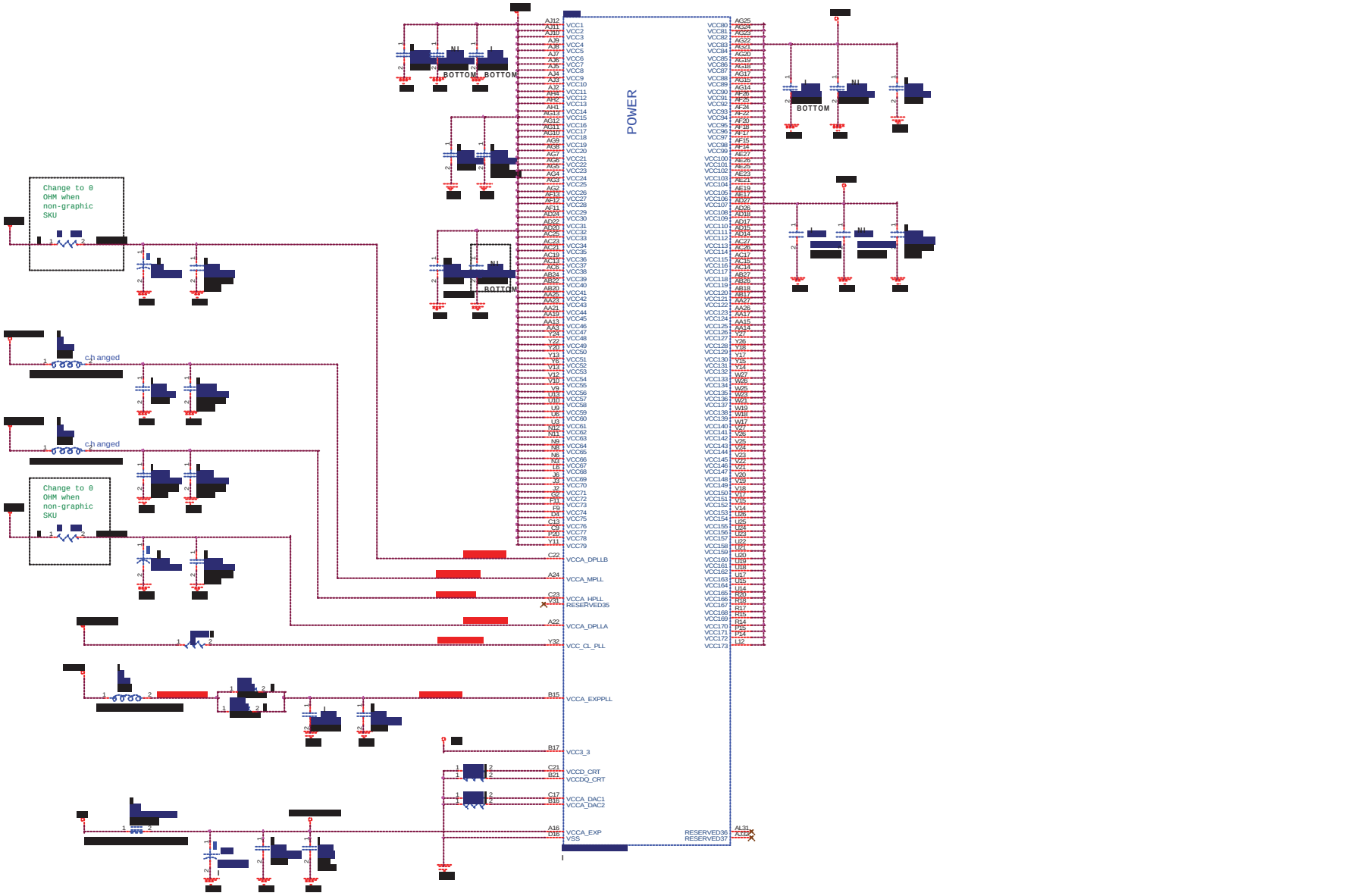
P5BW-MB R100_0426

ASUSTek COMPUTER INC	Title : P965 - 1	
	Engineer: Simon Chang	
Size: A3	Project Name: P5BW-MB	Rev: 1.00
Date: Friday, May 12, 2006	Sheet 14 of 55	

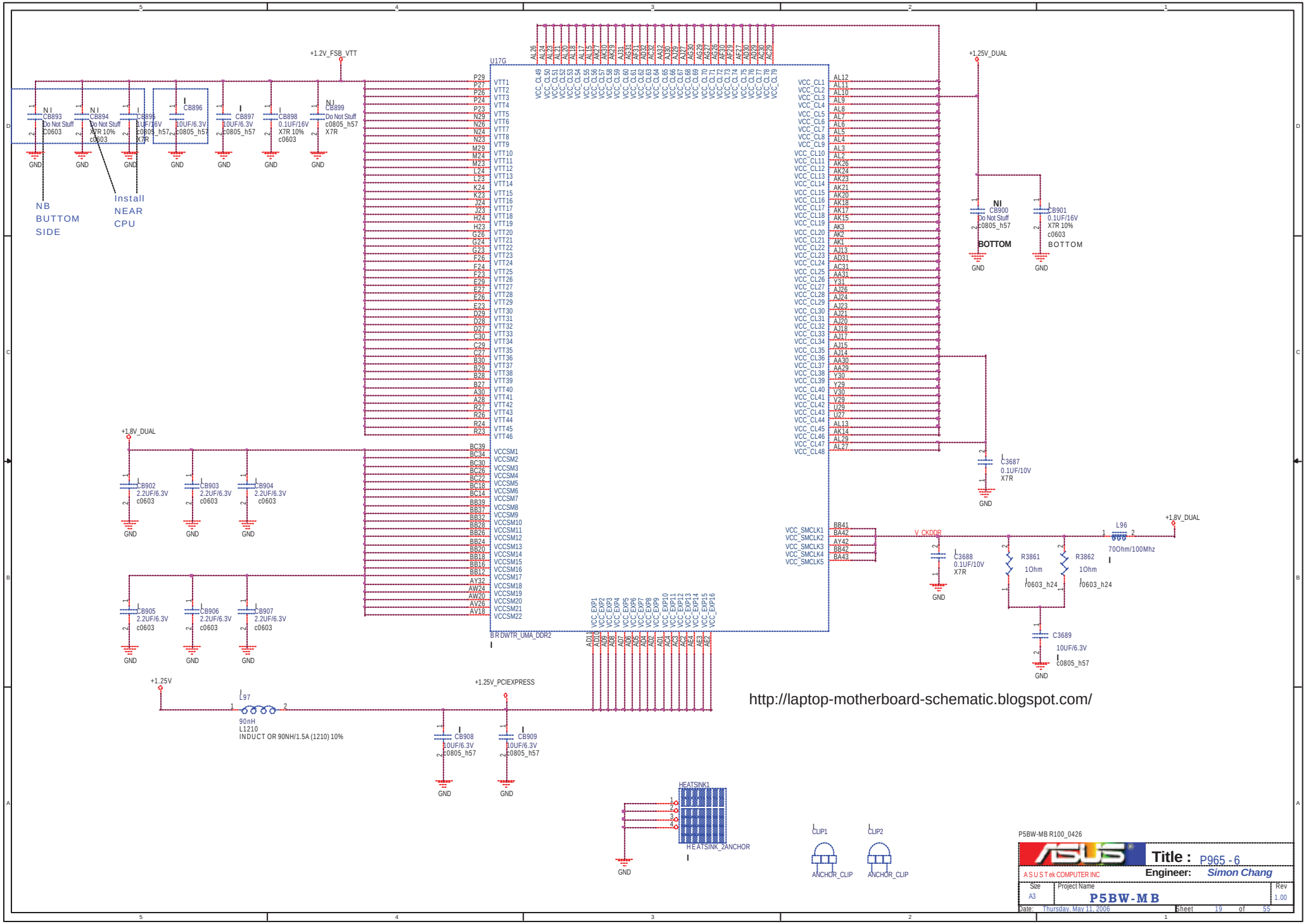


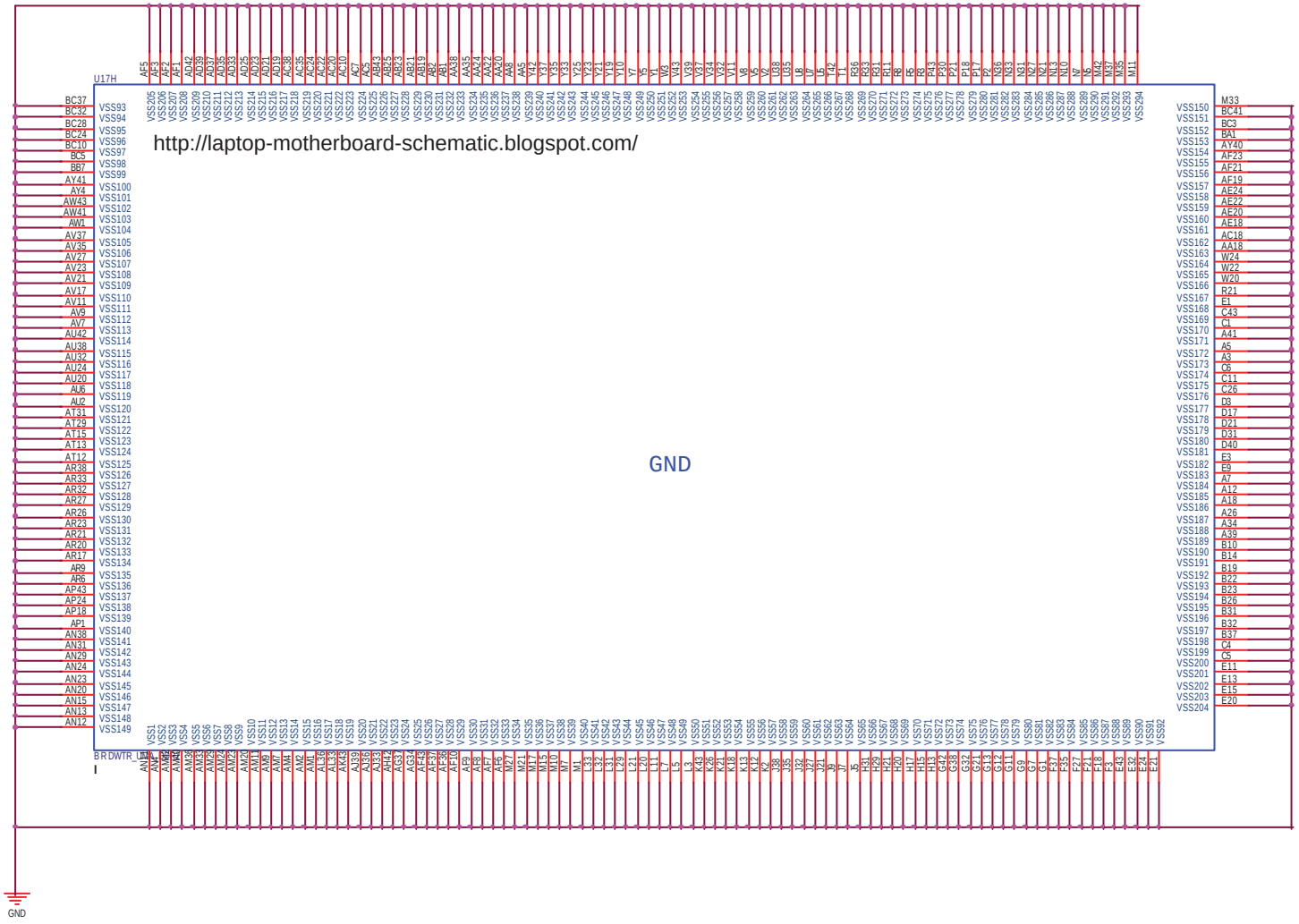






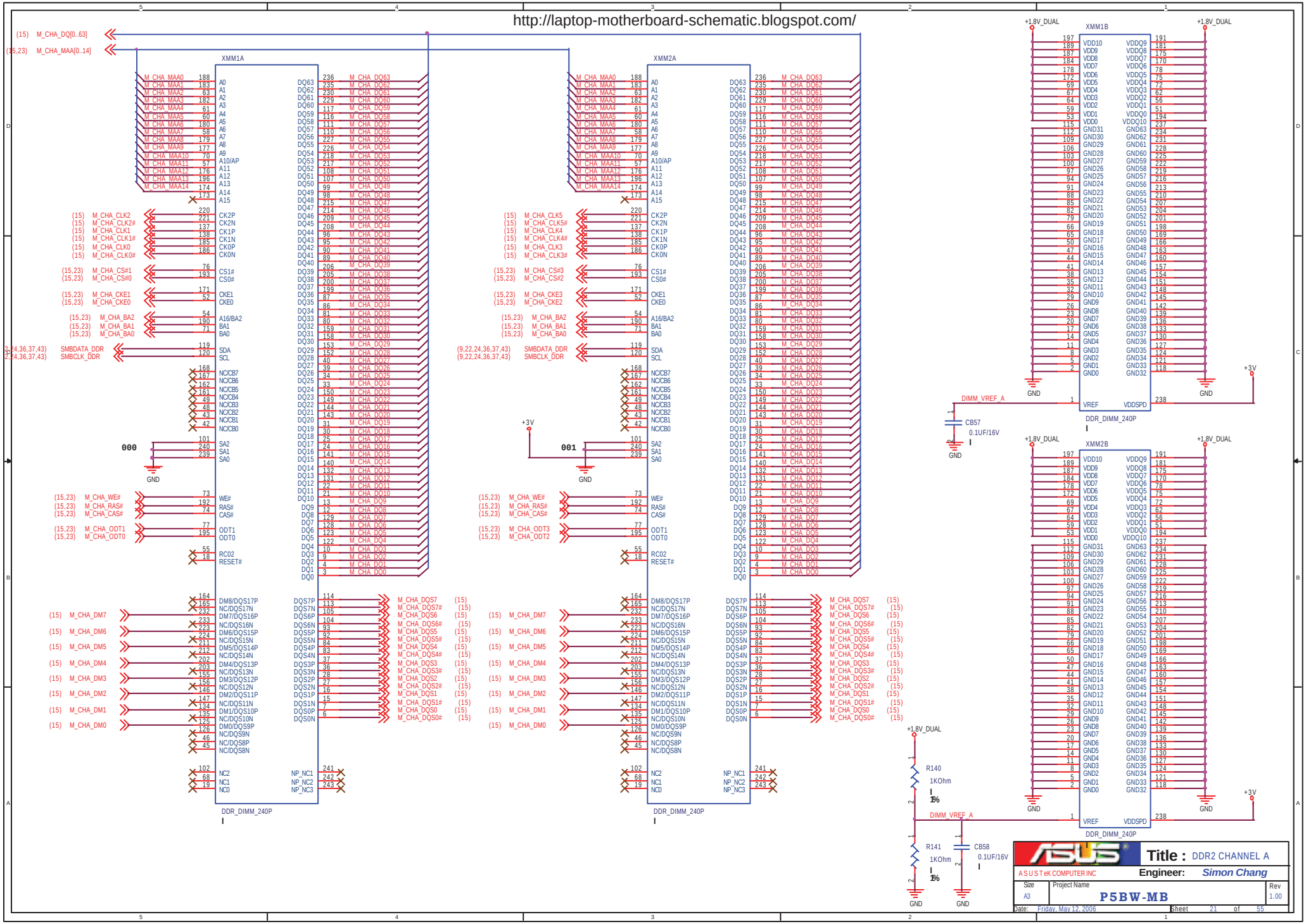
Title : P965 - 5
Engineer: Simon Chang
P5BW-MB

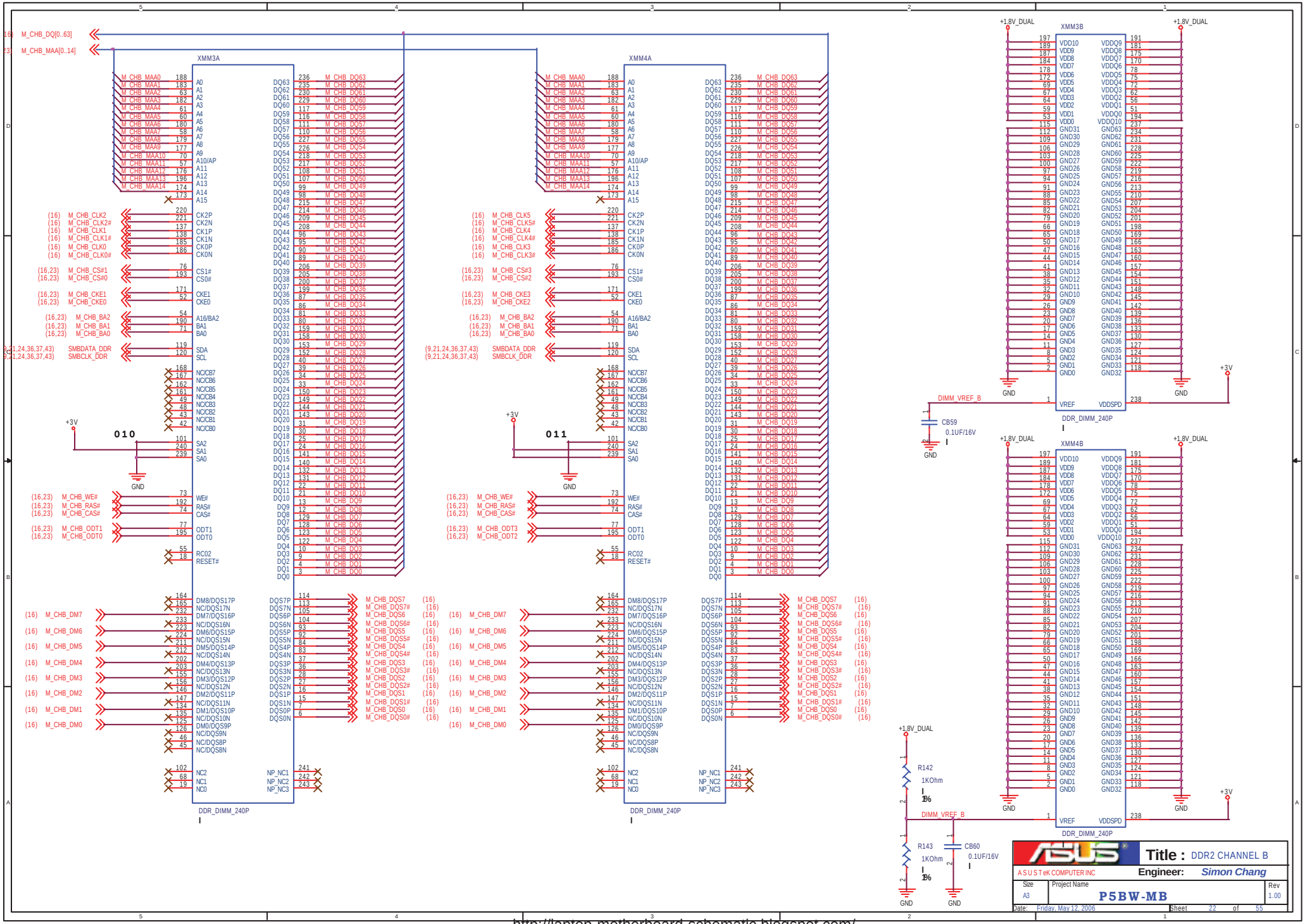

+1.2V_FSB_VTT
U17G
NI CB893 Do Not Stuff c0603
NI CB894 Do Not Stuff X7R 10% c0603
I CB895 1UF/16V c0805_h57 X7R
I CB896 10UF/6.3V c0805_h57
I CB897 10UF/6.3V c0805_h57
I CB898 0.1UF/16V X7R 10% c0603
NI CB899 Do Not Stuff c0805_h57 X7R
GND
NB BUTTOM SIDE
Install NEAR CPU
VTT1 VTT2 VTT3 VTT4 VTT5 VTT6 VTT7 VTT8 VTT9 VTT10 VTT11 VTT12 VTT13 VTT14 VTT15 VTT16 VTT17 VTT18 VTT19 VTT20 VTT21 VTT22 VTT23 VTT24 VTT25 VTT26 VTT27 VTT28 VTT29 VTT30 VTT31 VTT32 VTT33 VTT34 VTT35 VTT36 VTT37 VTT38 VTT39 VTT40 VTT41 VTT42 VTT43 VTT44 VTT45 VTT46
VCCSM1 VCCSM2 VCCSM3 VCCSM4 VCCSM5 VCCSM6 VCCSM7 VCCSM8 VCCSM9 VCCSM10 VCCSM11 VCCSM12 VCCSM13 VCCSM14 VCCSM15 VCCSM16 VCCSM17 VCCSM18 VCCSM19 VCCSM20 VCCSM21 VCCSM22
BRDWTR_UMA_DDR2
+1.25V_DUAL
NI CB900 Do Not Stuff c0805_h57 BOTTOM
CB901 0.1UF/16V X7R 10% c0603 BOTTOM
C3687 0.1UF/10V X7R
+1.8V_DUAL
CB902 2.2UF/6.3V c0603
CB903 2.2UF/6.3V c0603
CB904 2.2UF/6.3V c0603
CB905 2.2UF/6.3V c0603
CB906 2.2UF/6.3V c0603
CB907 2.2UF/6.3V c0603
V_CKDDR
C3688 0.1UF/10V X7R
R3861 1Ohm 0603_h24
R3862 1Ohm 0603_h24
L96 70Ohm/100Mhz
C3689 10UF/6.3V c0805_h57
+1.25V
L97 90nH L1210 INDUCTOR 90NH/1.5A (1210) 10%
+1.25V_PCIEXPRESS
CB908 10UF/6.3V c0805_h57
CB909 10UF/6.3V c0805_h57
HEATSINK1
HEATSINK_2ANCHOR
CLIP1
CLIP2
ANCHOR_CLIP
http://laptop-motherboard-schematic.blogspot.com/
P5BW-MB R100_0426
Title : P965 - 6
A S U S Tek COMPUTER INC
Engineer: Simon Chang
Size A3
Project Name P5BW-MB
Rev 1.00
Date: Thursday, May 11, 2006
Sheet 19 of 55

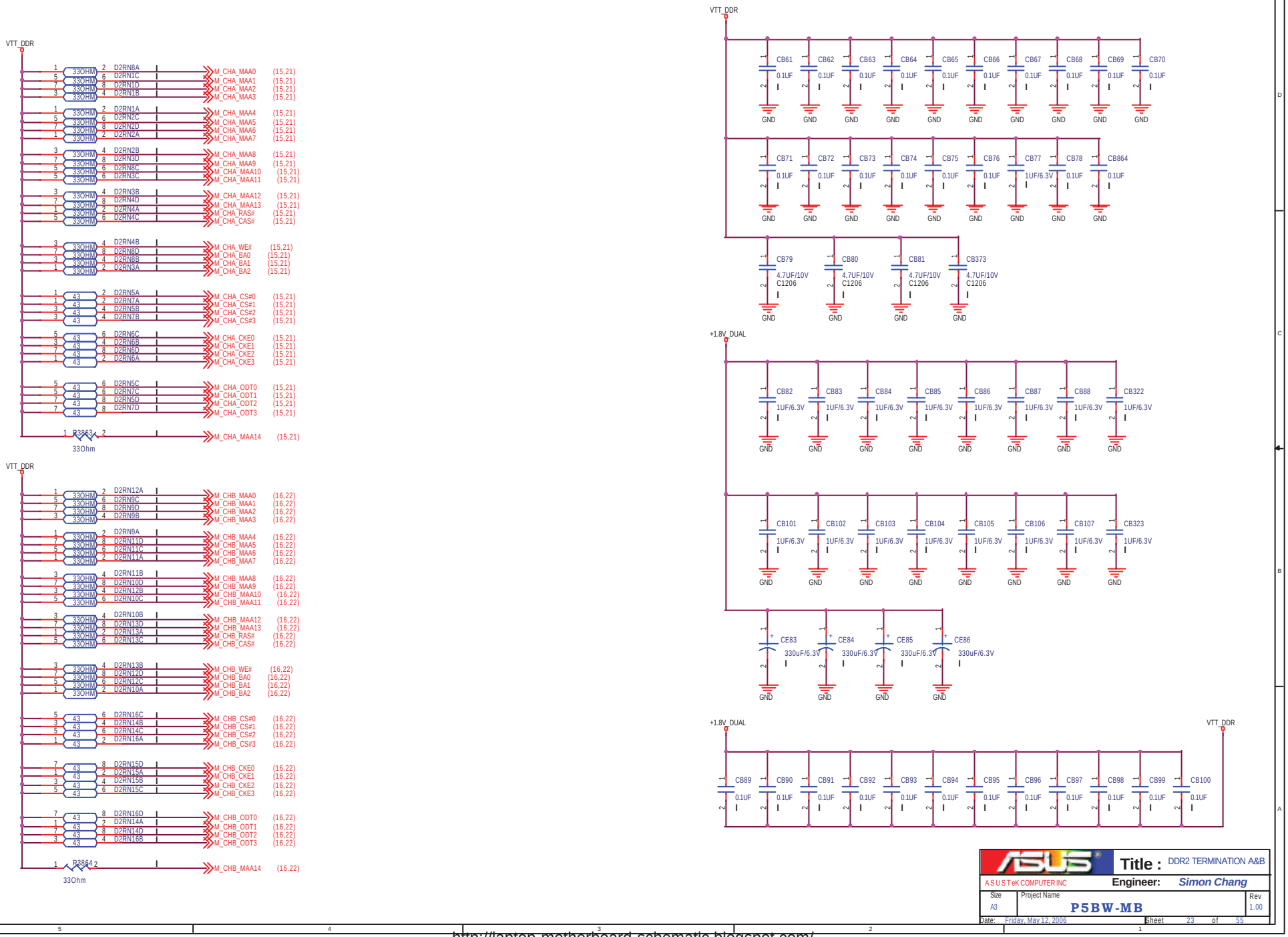


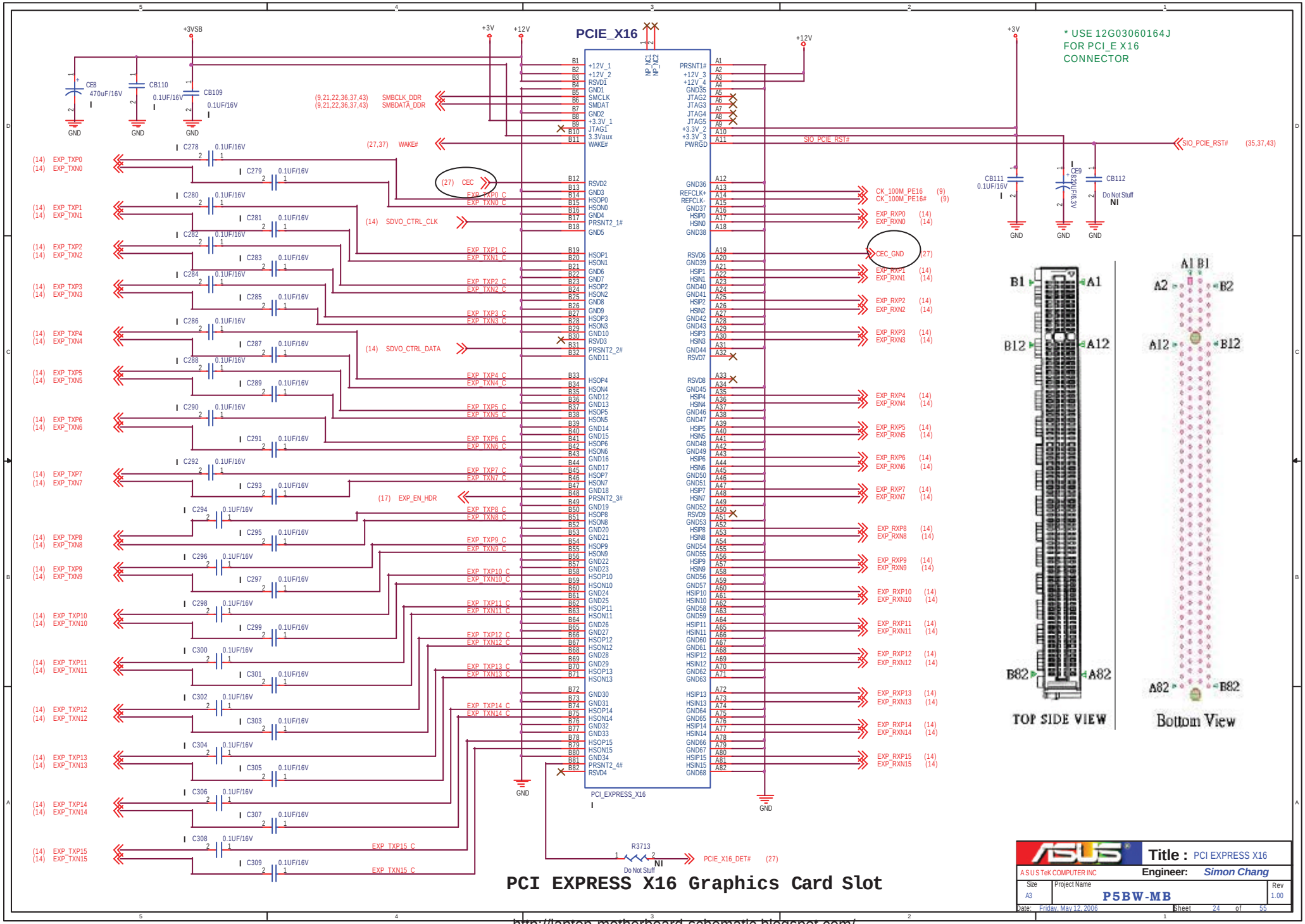
P5BW-MB R100_0426

ASUSTek COMPUTER INC	Title : P965 - 7		
	Engineer: Simon Chang		
Size: A3	Project Name: P5BW-MB		Rev: 1.00
Date: Thursday, May 11, 2006	Sheet 20 of 55		



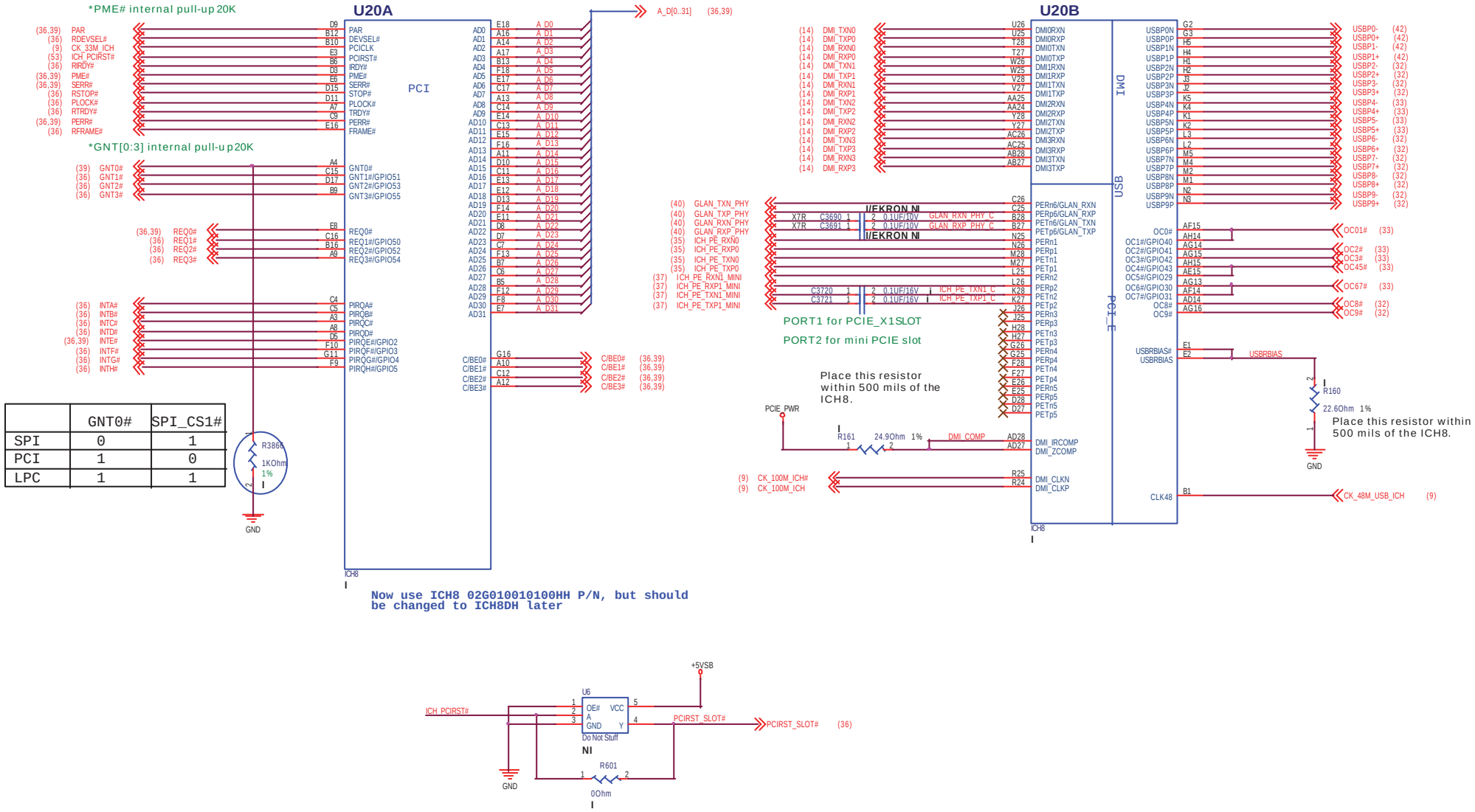






PCI EXPRESS X16 Graphics Card Slot

DEVICE	REQ#	GNT#	INTERRUPT	ID_SEL
IEEE 1394	0	0	E	AD_19
Wagner	1	1	C	AD_26
PCI SLOT 1	2	2	BCDA	AD_21
PCI SLOT 2	3	3	ABCD	AD_20



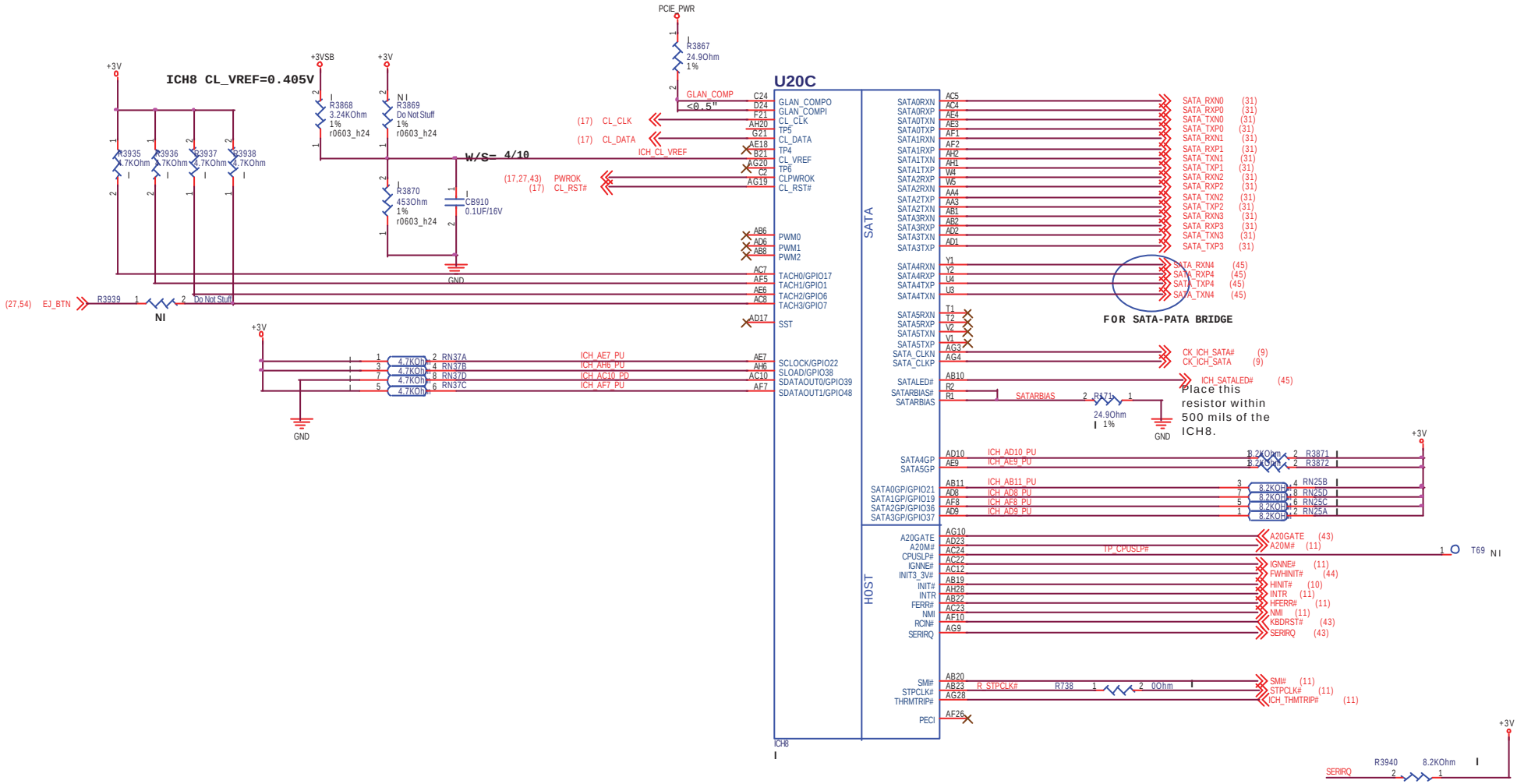
Title : ICH8 CONTROL - 1

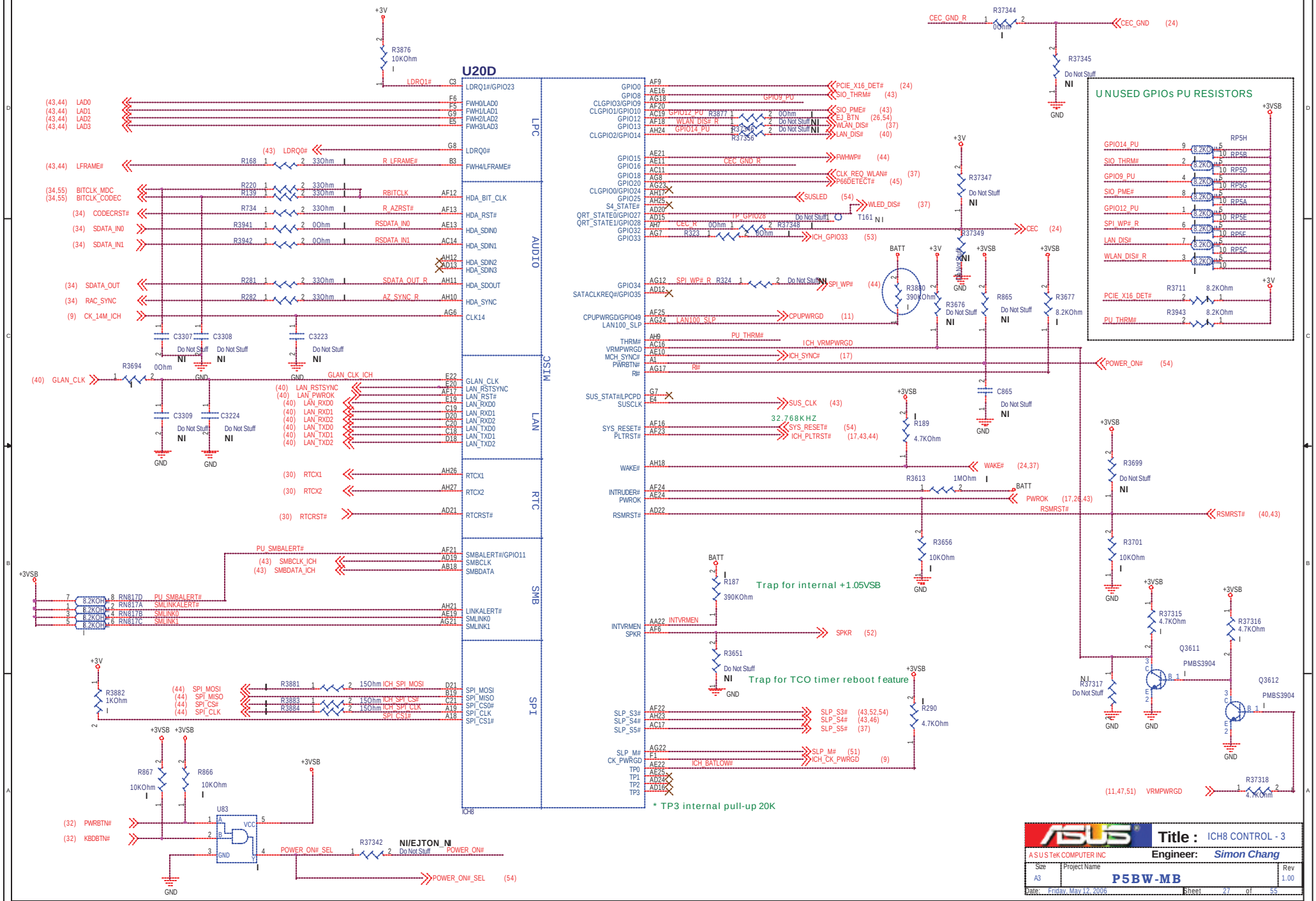
ASUSTeK COMPUTER INC

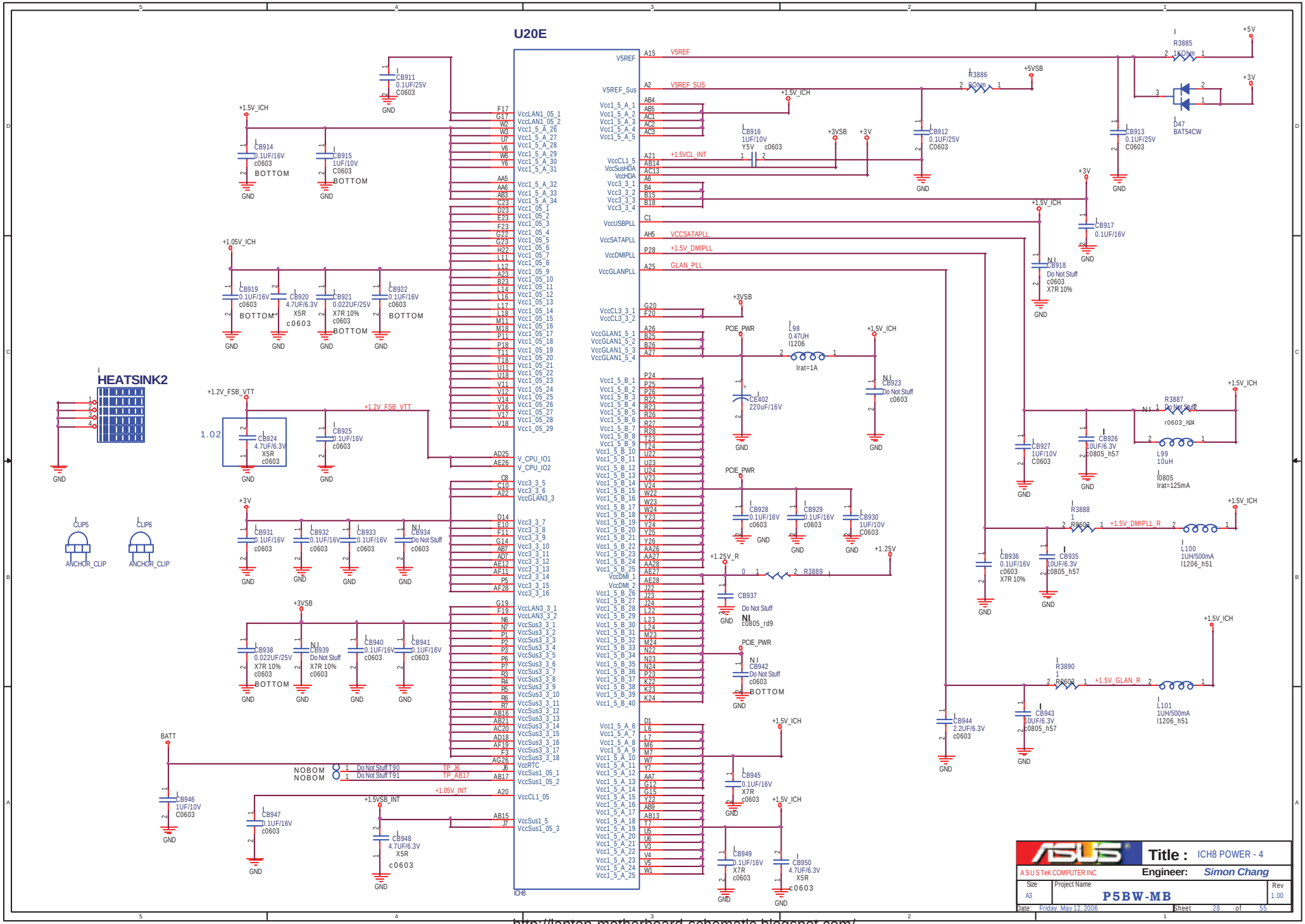
Engineer: Simon Chang

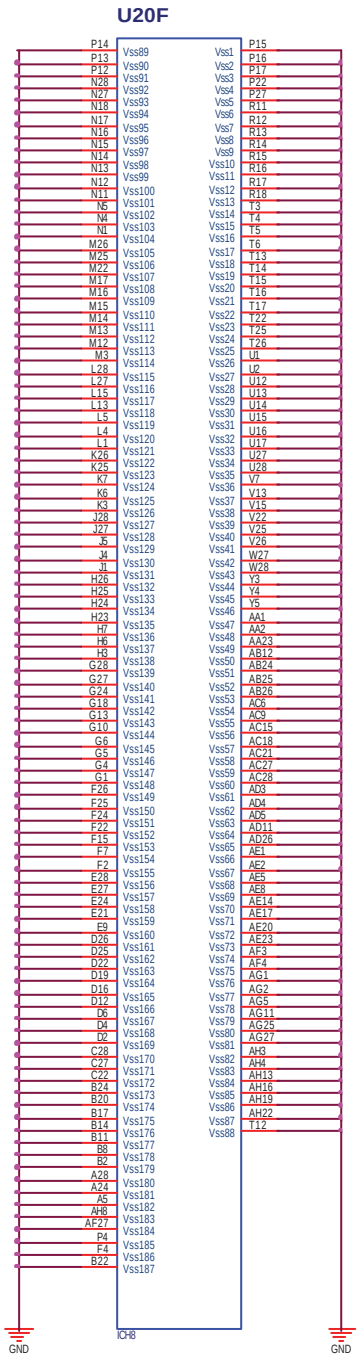
Size	Project Name	Rev
A3	P5BW-MB	1.00

Date: Friday, May 12, 2006 Sheet 25 of 55









Name	Default	Power status	Type	Description	Note
GPIO55	Native	3.3V (Main)	I/O	Muxed with GNT3#	Strap pin
GPIO54	Native	5V (Main)	I/O	Muxed with REQ3#	
GPIO53	Native	3.3V (Main)	I/O	Muxed with GNT2#	Strap pin
GPIO52	Native	5V (Main)	I/O	Muxed with REQ2#	
GPIO51	Native	3.3V (Main)	I/O	Muxed with GNT1#	Strap pin
GPIO50	Native	5V (Main)	I/O	Muxed with REQ1#	
GPIO49	Native	+1.2V_FSB_VTT	I/O	Muxed with CPUPWRGD	
GPIO48	GPI	3.3V (Main)	I/O	Muxed with SDATAOUT1	
GPIO[43:40]	Native	3.3V (Standby)	I/O	Muxed with OC[4:1]#	
GPIO39	GPI	3.3V (Main)	I/O	Muxed with SDATAOUT0	
GPIO38	GPI	3.3V (Main)	I/O	Muxed with SLOAD	
GPIO37	GPI	3.3V (Main)	I/O	Muxed with SATA3GP	
GPIO36	GPI	3.3V (Main)	I/O	Muxed with SATA2GP	
GPIO35	GPO(Low)	3.3V (Main)	I/O	Muxed with SATACLKREQ#	
GPIO34	GPO(Low)	3.3V (Main)	I/O	Unmuxed	
GPIO33	GPO(High)	3.3V (Main)	I/O	Unmuxed	
GPIO32	GPO(High)	3.3V (Main)	I/O	Unmuxed	
GPIO31	Native	3.3V (Standby)	I/O	Muxed with OC7#	
GPIO30	Native	3.3V (Standby)	I/O	Muxed with OC6#	
GPIO29	Native	3.3V (Standby)	I/O	Muxed with OC5#	
GPIO28	GPO(Low)	3.3V (Standby)	I/O	Muxed with EL_STATE1	
GPIO27	GPO(Low)	3.3V (Standby)	I/O	Muxed with EL_STATE0	
GPIO26	GPO	3.3V (Standby)	I/O	Muxed with S4_STATE#	
GPIO25	GPO(High)	3.3V (Standby)	I/O	Unmuxed	
GPIO24	GPO	3.3V (Standby)	I/O	Muxed with CLGPIO0. Not cleared by CF9h reset event.	
GPIO23	Native	3.3V (Main)	I/O	Muxed with LDRQ1#	
GPIO22	GPI	3.3V (Main)	I/O	Muxed with SCLOCK	
GPIO21	GPI	3.3V (Main)	I/O	Muxed with SATA0GP	
GPIO20	GPO(High)	3.3V (Main)	I/O	Unmuxed	Strap pin
GPIO19	GPI	3.3V (Main)	I/O	Muxed with SATA1GP	
GPIO18	GPO(High)	3.3V (Main)	I/O	Unmuxed	
GPIO17	GPI	3.3V (Main)	I/O	Muxed with TACH0	
GPIO16	GPO(Low)	3.3V (Main)	I/O	Unmuxed	
GPIO15	GPO(High)	3.3V (Standby)	I/O	Unmuxed	
GPIO14	GPI	3.3V (Standby)	I/O	Muxed with CLGPIO2	
GPIO13	GPI	3.3V (Standby)	I/O	Unmuxed	
GPIO12	GPI	3.3V (Standby)	I/O	Unmuxed	
GPIO11	Native	3.3V (Standby)	I/O	Muxed with SMBALERT#	
GPIO10	Native	3.3V (Standby)	I/O	Muxed with CLGPIO1	
GPIO9	Native	3.3V (Standby)	I/O	Muxed with CLGPIO3	
GPIO8	GPI	3.3V (Standby)	I/O	Unmuxed	
GPIO[7:6]	GPI	3.3V (Main)	I/O	Muxed with TACH[3:2]	
GPIO[5:2]	GPI	5V (Main)	I/OD	Muxed with PIRQ[H:E]#	
GPIO1	GPI	3.3V (Main)	I/O	Muxed with TACH1	
GPIO0	GPI	3.3V (Main)	I/O	Unmuxed	

GPIO[0:15] can be configured to cause a SMI# or SCI.

All default GPI need a pull up if no use

ASUS

Title : ICH8 POWER - 5

A S U S TeK COMPUTER INC

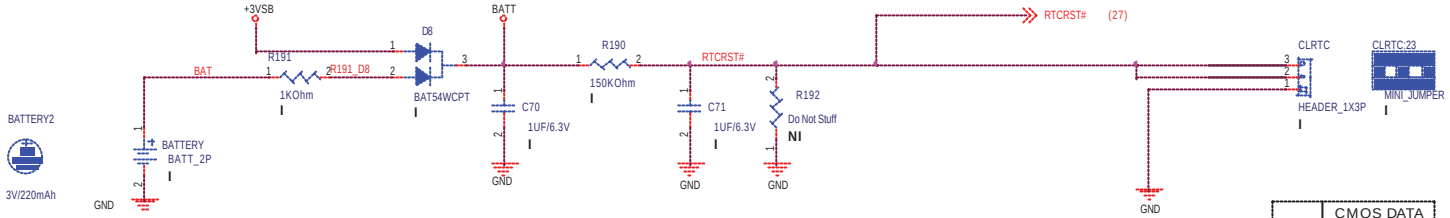
Engineer: Simon Chang

Size	Project Name	Rev
A3	P5BW-MB	1.00

Date: Friday, May 12, 2006 Sheet 29 of 55

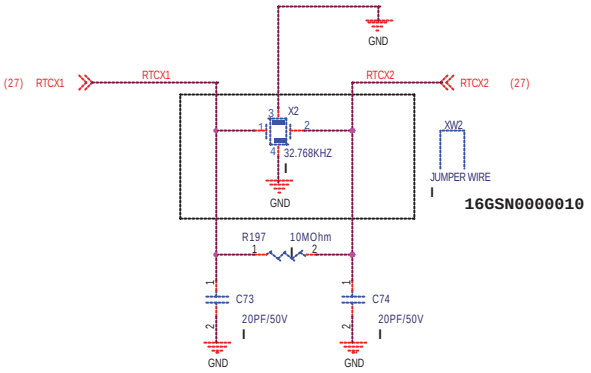
External RTC Circuitry

CLEAR CMOS

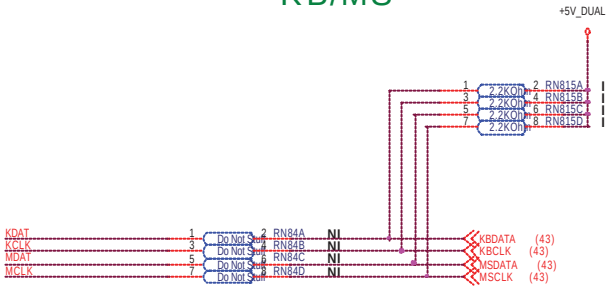


	CMOS DATA
1-2	CLEAR
2-3	Default

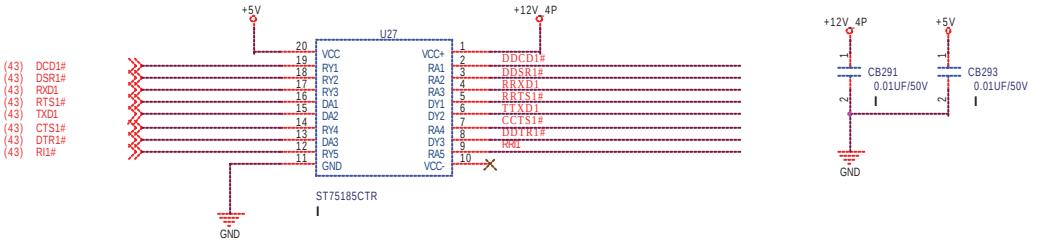
Battery Socket

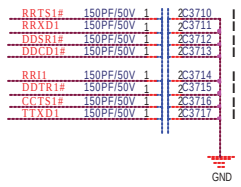


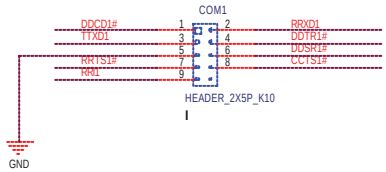
KB/MS

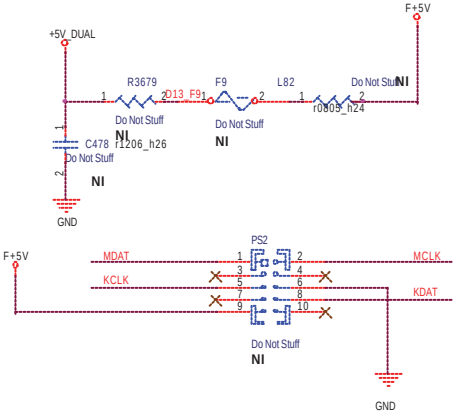


SERIAL PORT for debugging









ASUSTeK COMPUTER INC

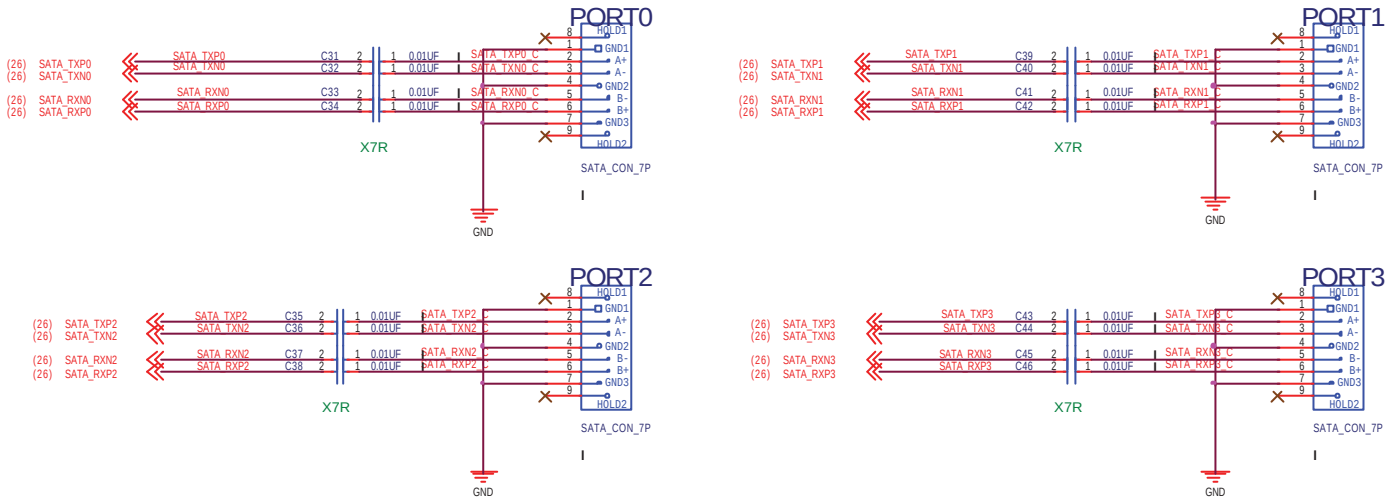
Title : RTC/COM/KB/MS CIRCUIT

Engineer: Simon Chang

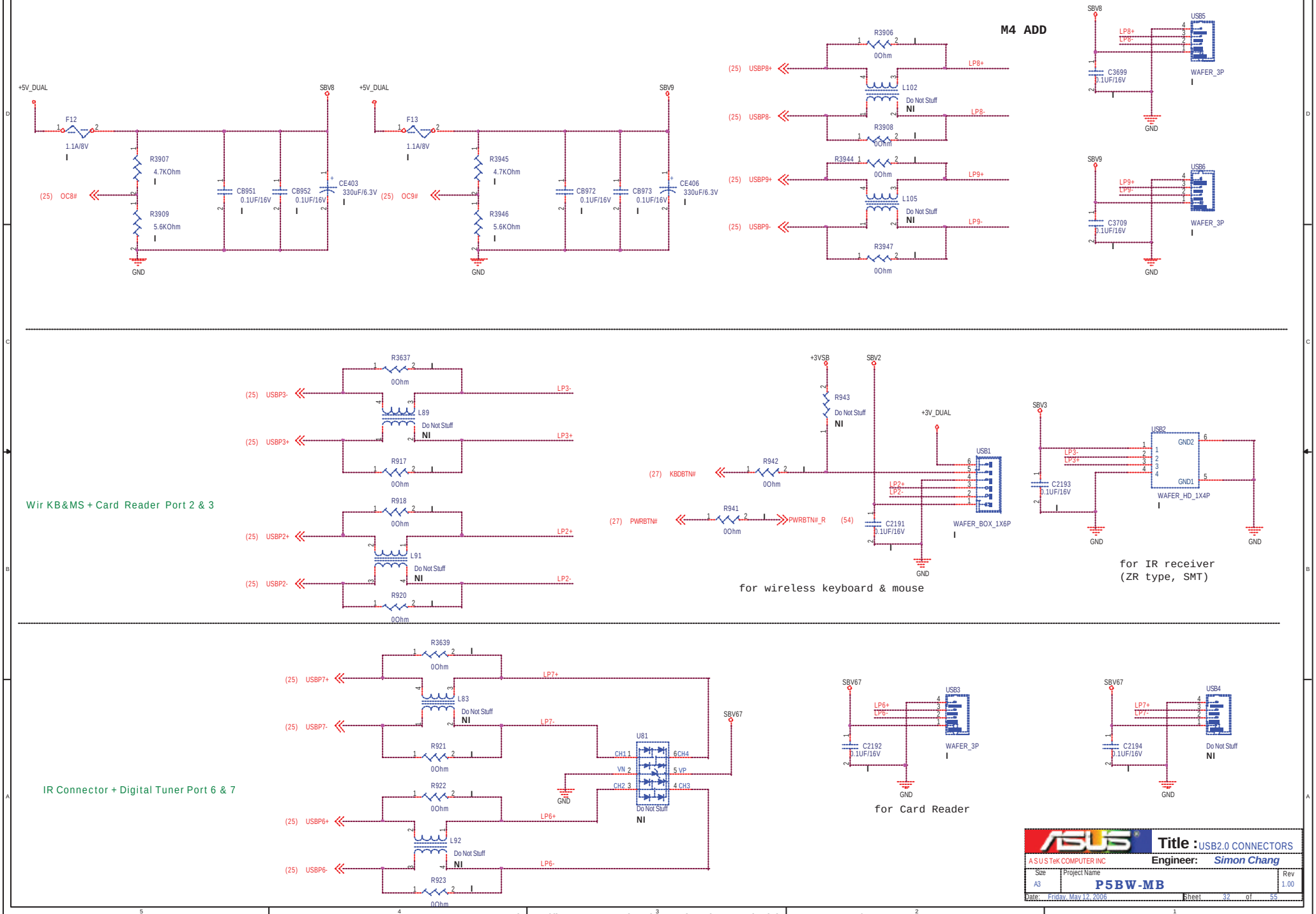
Size	Project Name	Rev
A3	P5BW-MB	1.00

Date: Friday, May 12, 2006 Sheet 30 of 55

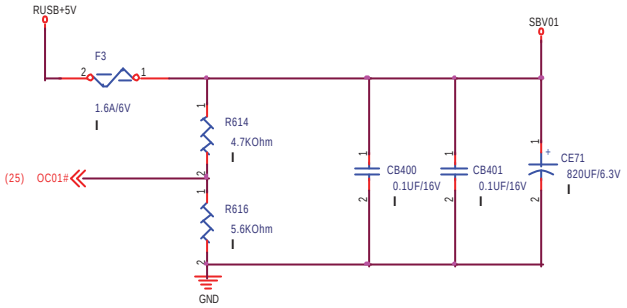
SATA CONNECTOR

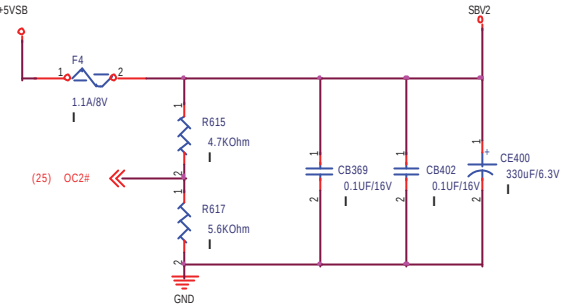


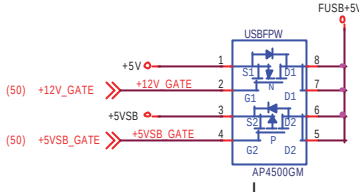
ASUSTeK COMPUTER INC	Title : SATA CON	
	Engineer: Simon Chang	
Size: A3	Project Name: P5BW-MB	Rev: 1.00
Date: Friday, May 12, 2006	Sheet 31 of 55	



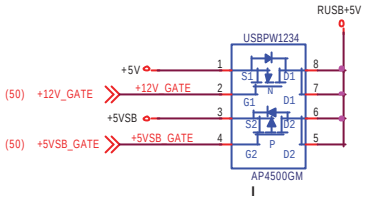
USB POWER CIRCUIT





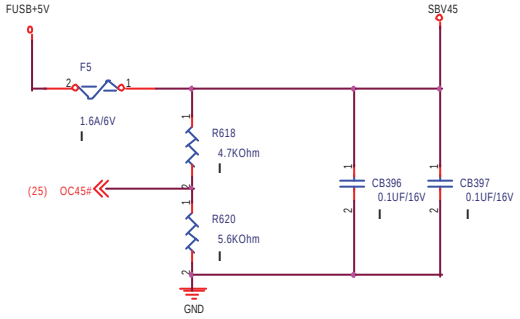


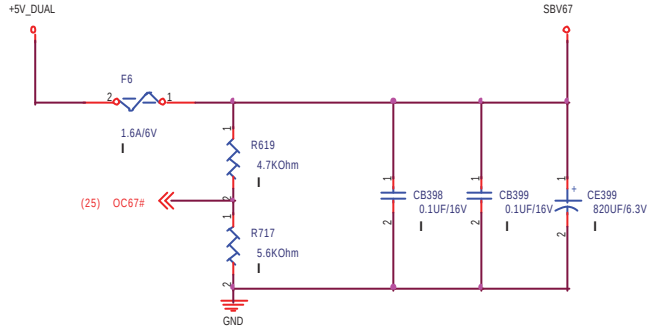
NMOS Suppose to 7A
PMOS Suppose to 4.5A

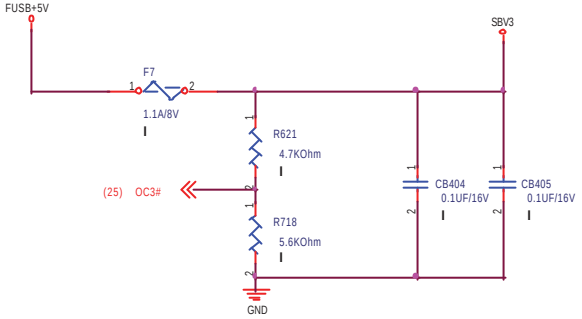


NMOS Suppose to 7A
PMOS Suppose to 4.5A

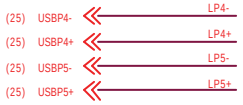
USB POWER OF REAR PORTS



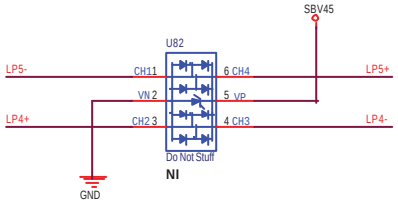


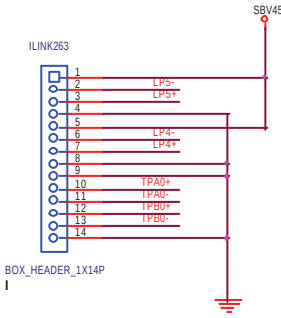


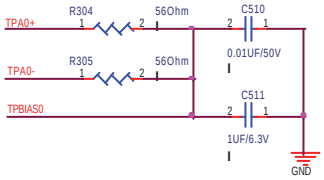
USB POWER OF FRONT I/O PORTS

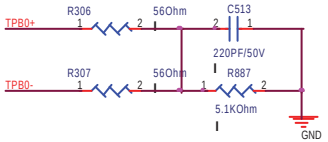


IEEE 1394 + Front USB Port 4 & 5



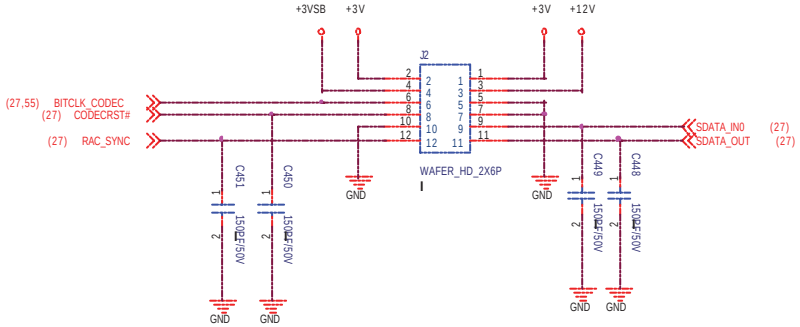


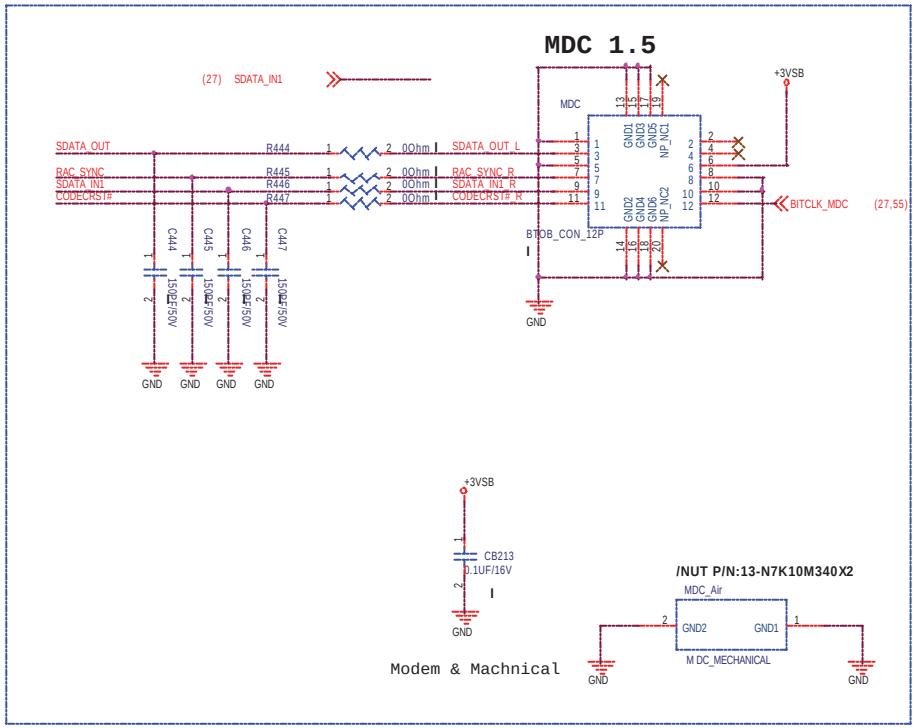




http://laptop-motherboard-schematic.blogspot.com/

ASUSTeK COMPUTER INC	Title : USB POWER	
	Engineer: Simon Chang	
Size: A3	Project Name: P5BW-MB	Rev: 1.00
Date: Friday, May 12, 2006	Sheet 33 of 55	



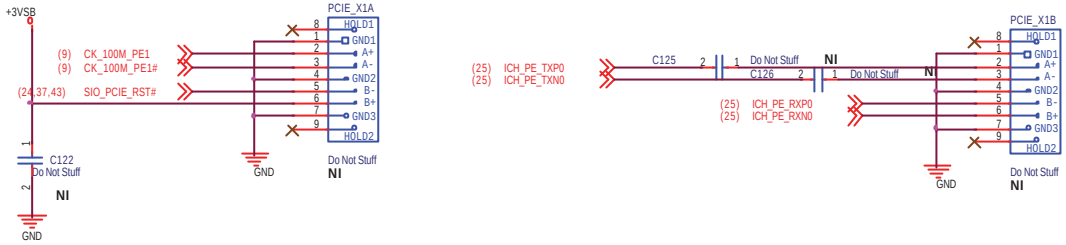


<Variant Name>

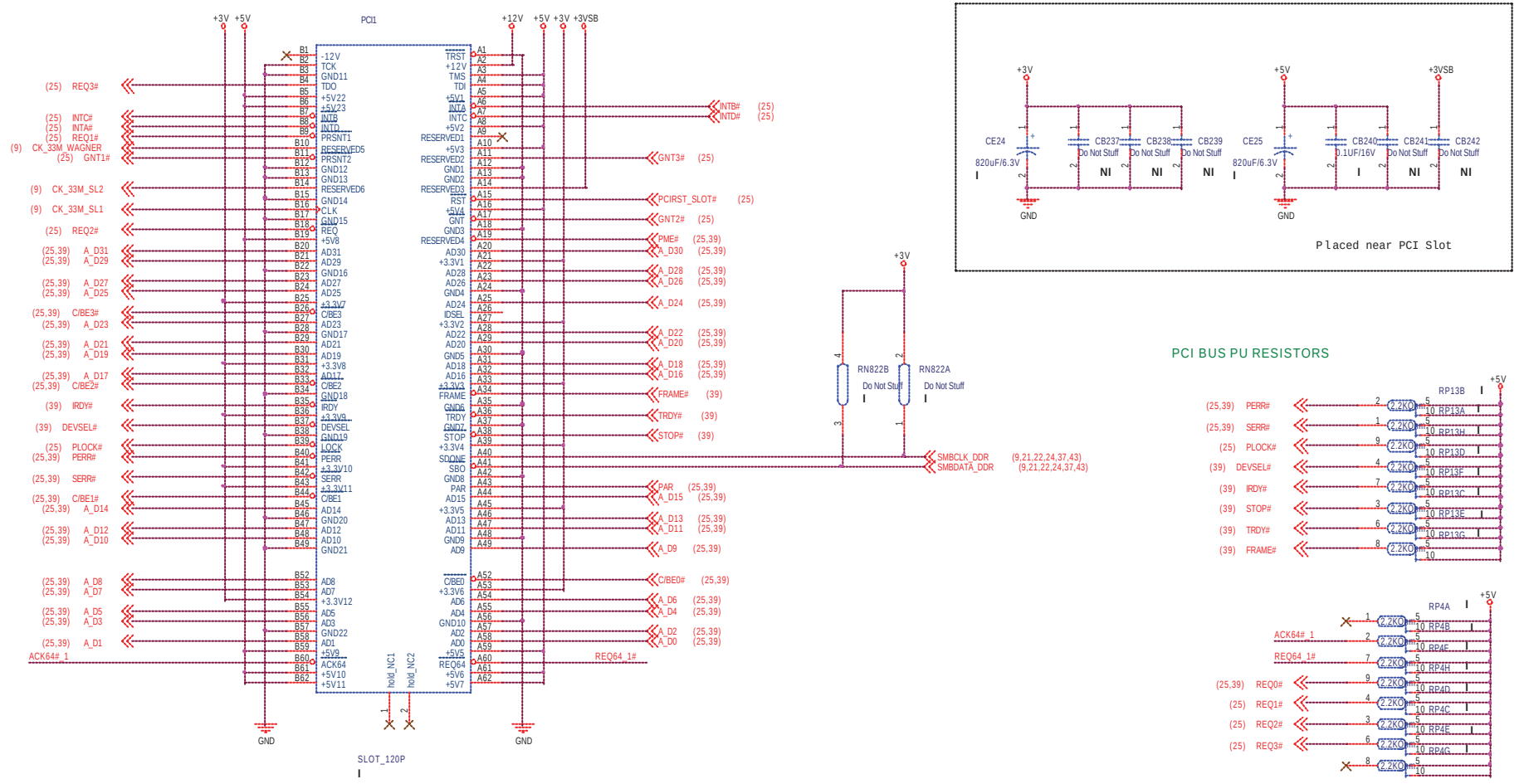
ASUSTeK COMPUTER INC	Title : AUDIO CONNECTOR & MDC	
	Engineer: Simon Chang	
Size: A3	Project Name: P5BW-MB	Rev: 1.00
Date: Friday, May 12, 2006	Sheet 34 of 55	

PCI EXPRESS X1 SLOT

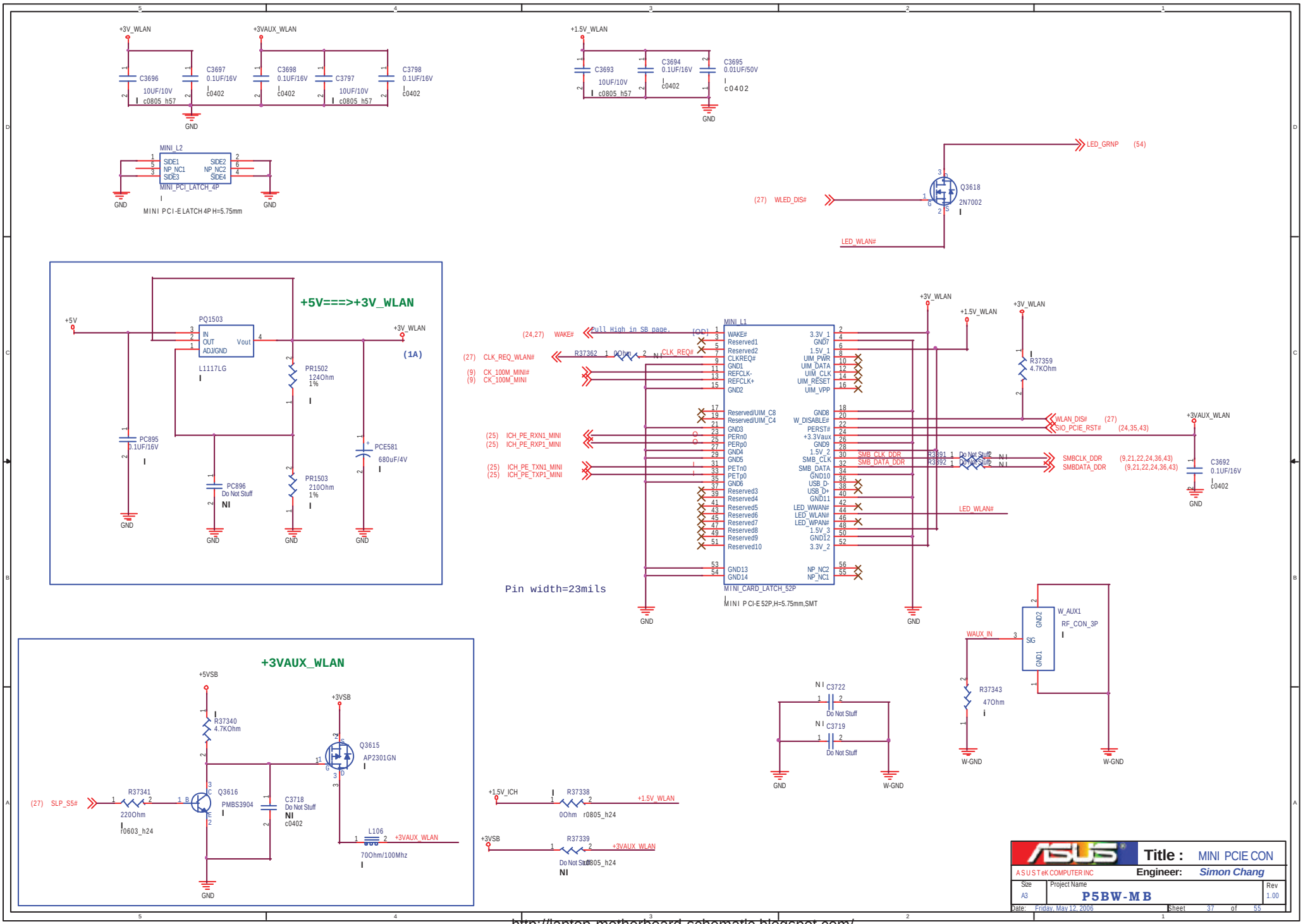
X7R
Please put C125,C126
near SB Side

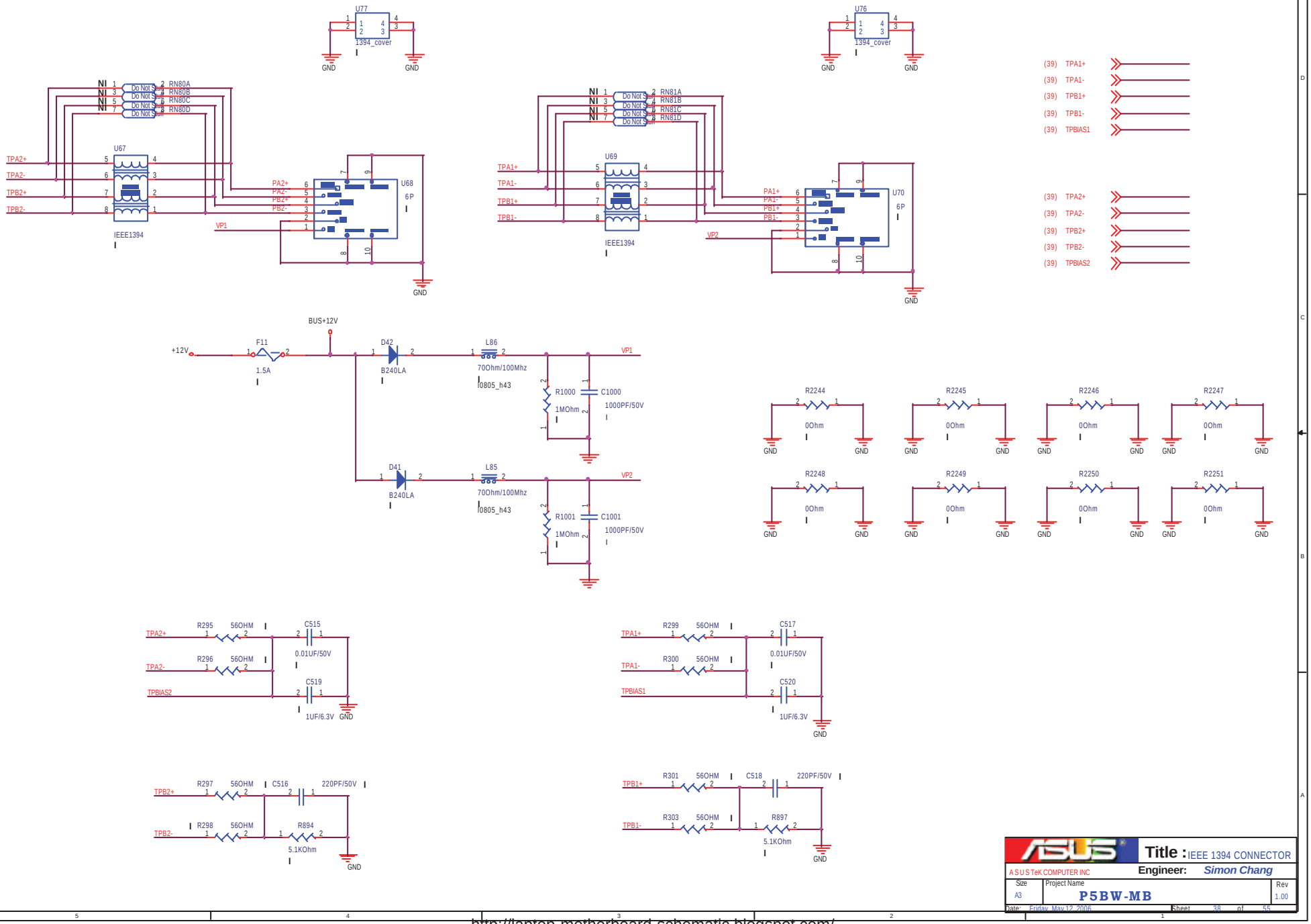


ASUSTeK COMPUTER INC	Title : PCI EXPRESS X1	
	Engineer: Simon Chang	
Size: A3	Project Name: P5BW-MB	Rev: 1.00
Date: Friday, May 12, 2006	Sheet 35 of 55	

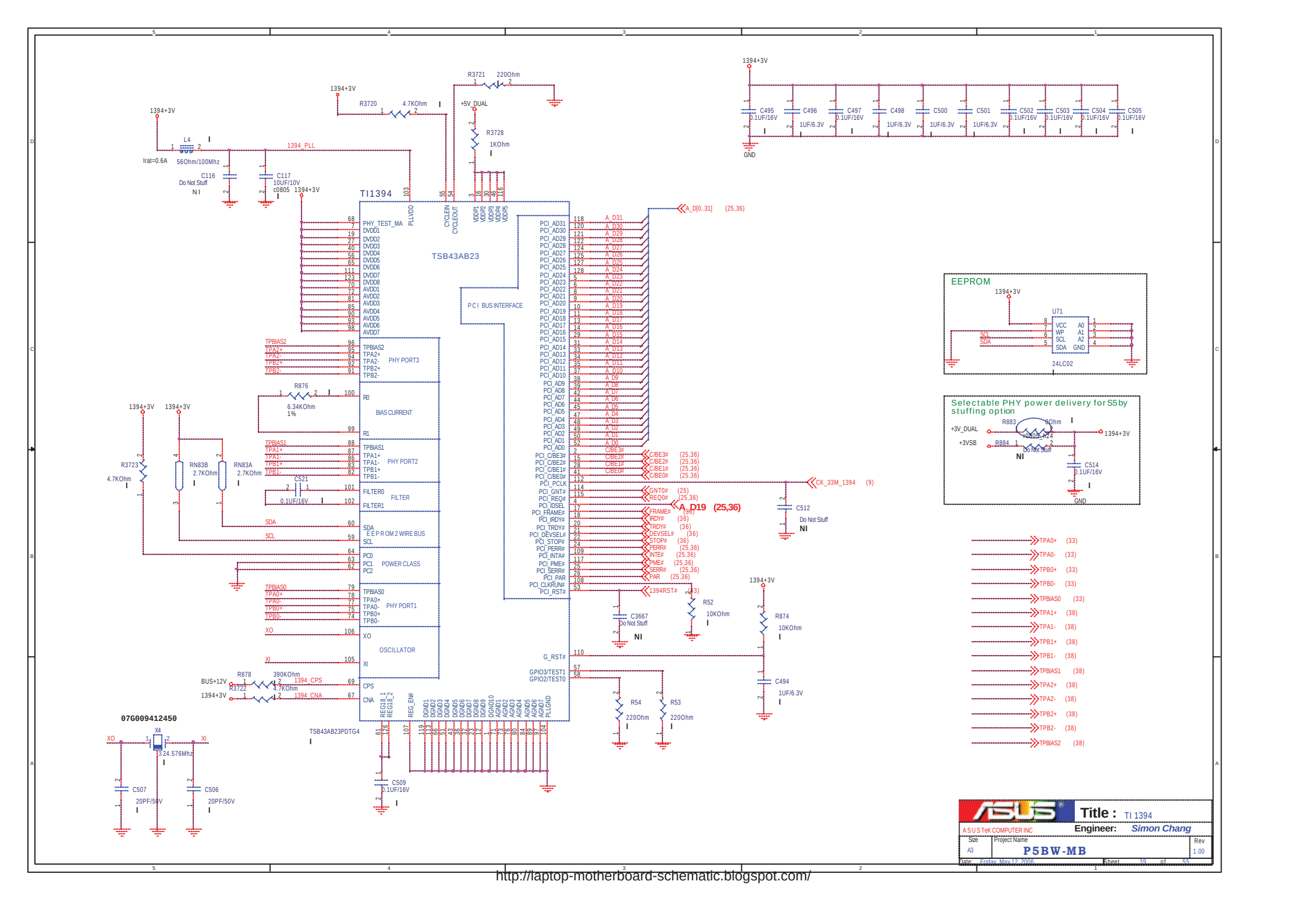


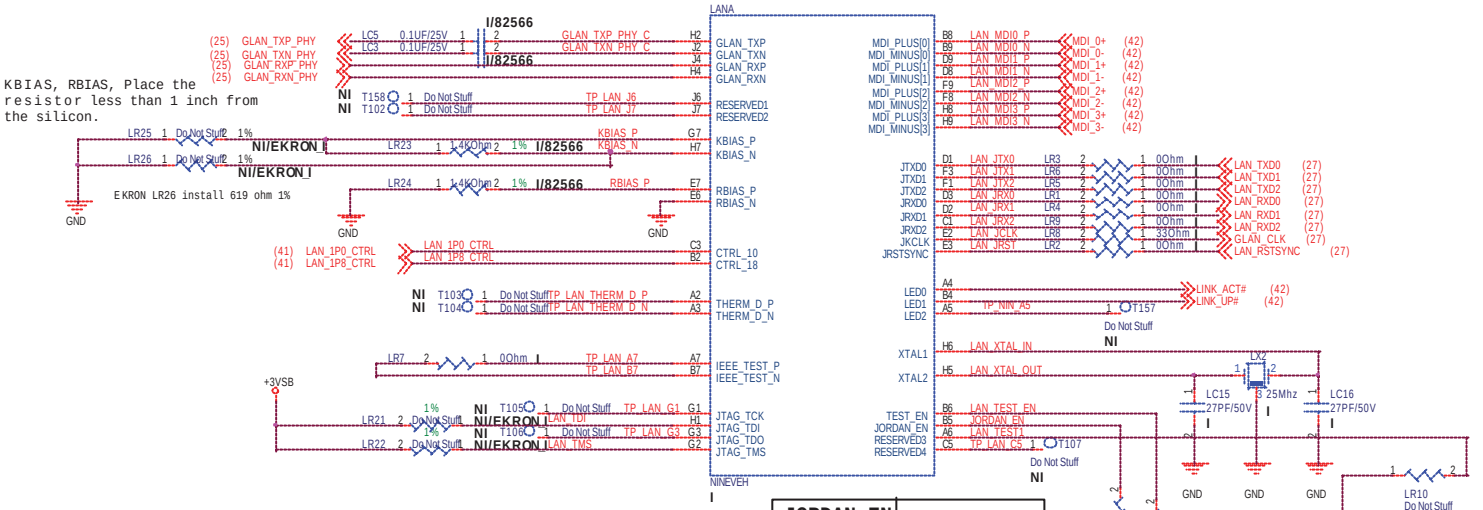
Title :	PCI SLOT	
ASUSTeK COMPUTER INC	Engineer:	Simon Chang
Size: A3	Project Name: P5BW-MB	Rev: 1.00
Date: Friday, May 12, 2006	Sheet 36 of 55	



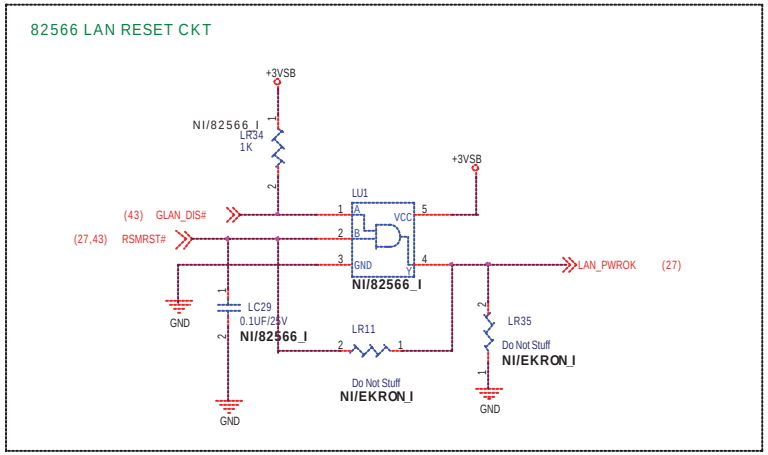


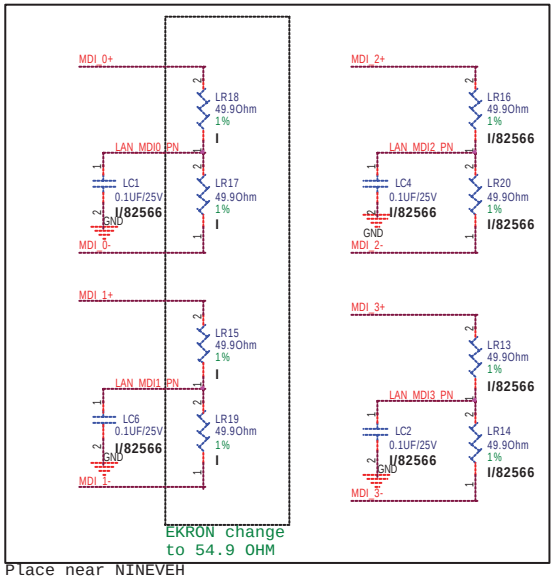
ASUSTeK COMPUTER INC	Title : IEEE 1394 CONNECTOR	
	Engineer: Simon Chang	
Size: A3	Project Name: P5BW-MB	Rev: 1.00
Date: Friday, May 12, 2006	Sheet 38 of 55	

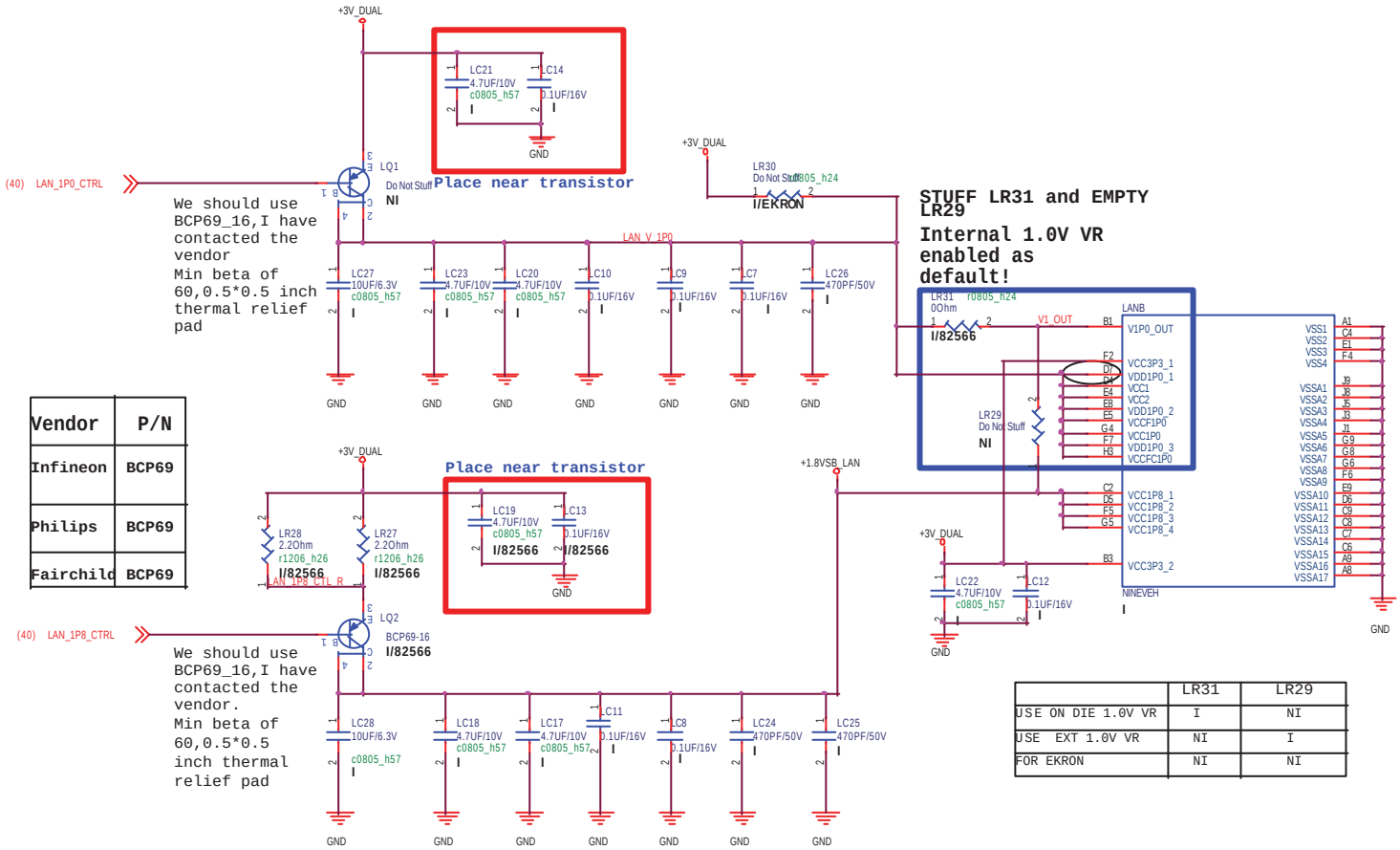




JORDAN_EN (LR33)	Function
I	GLCI Only
NI	GLCI + LCI







Vendor	P/N
Infineon	BCP69
Philips	BCP69
Fairchild	BCP69

	LR31	LR29
USE ON DIE 1.0V VR	I	NI
USE EXT 1.0V VR	NI	I
FOR EKRON	NI	NI

<Variant Name>

ASUS

Title : NINEVEH-2

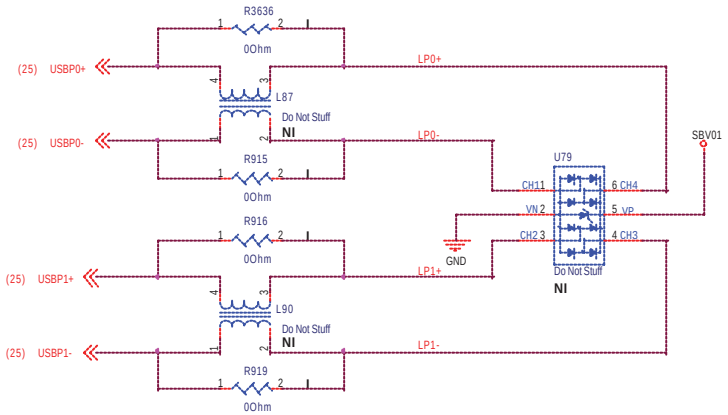
A S U S TeK COMPUTER INC

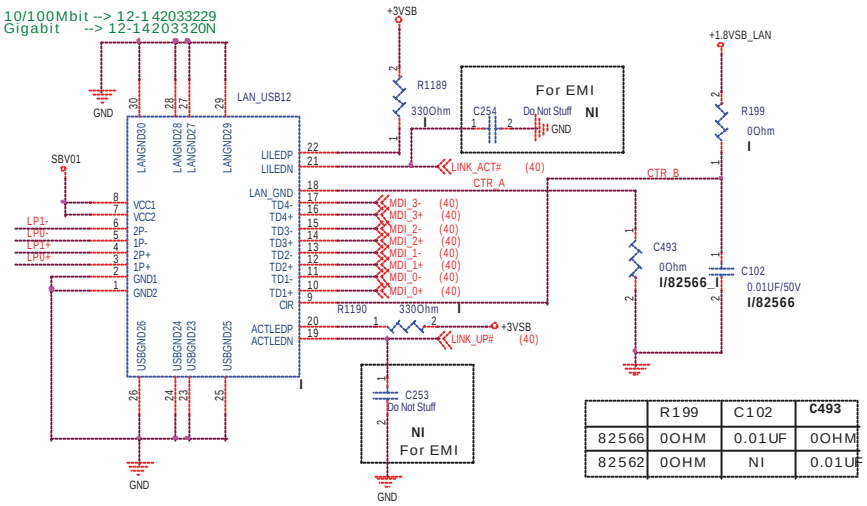
Engineer: Simon Chang

Size	Project Name	Rev
A3	P5BW-MB	1.00

Date: Friday, May 12, 2006 Sheet 41 of 55

L A N + Dual USB CONNECTOR Port 0 & 1





	R199	C102	C493
82566	0OHM	0.01UF	0OHM
82562	0OHM	NI	0.01UF

<Variant Name>

ASUS

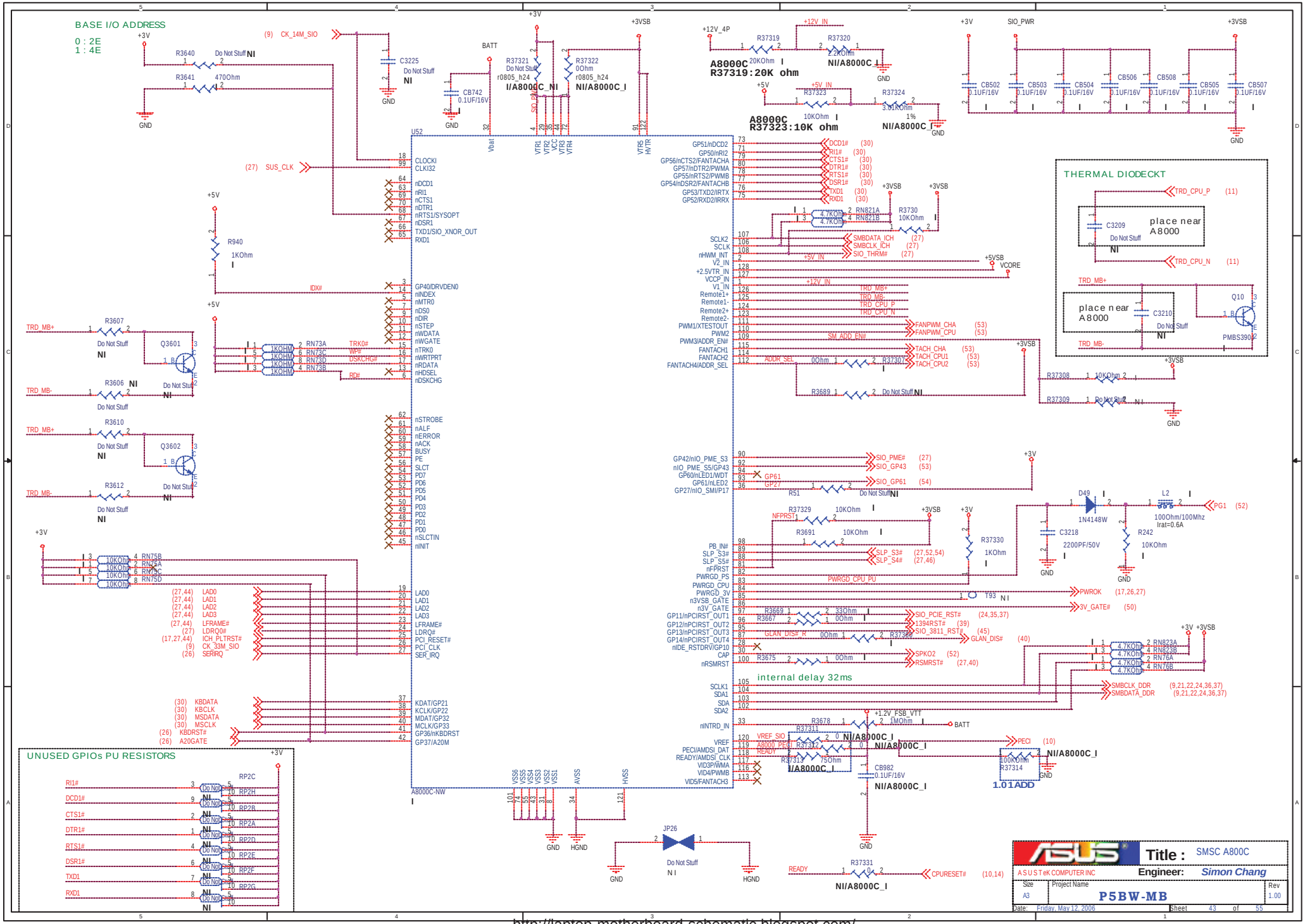
Title : LAN+USB CON

A S U S TeK COMPUTER INC

Engineer: Simon Chang

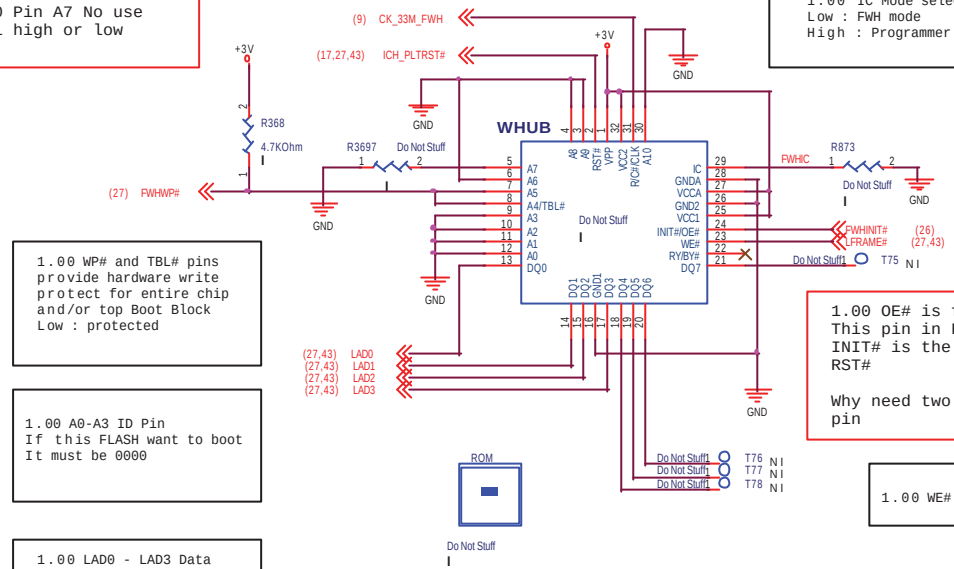
Size	Project Name	Rev
A3	P5BW-MB	1.00

Date: Friday, May 12, 2006 Sheet 42 of 55



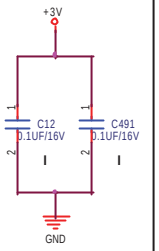
FWH Flash

1.00 Pin A7 No use
pull high or low
TBD



1.00 IC Mode select pin
Low : FWH mode
High : Programmer mode

1.00 FWH Decoupling
capacitor



1.00 For ICH6
INIT# is connected to
ICH6 INIT3_3V#

1.00 WP# and TBL# pins
provide hardware write
protect for entire chip
and/or top Boot Block
Low : protected

1.00 OE# is for another package
This pin in FWH is INIT#
INIT# is the same function with
RST#

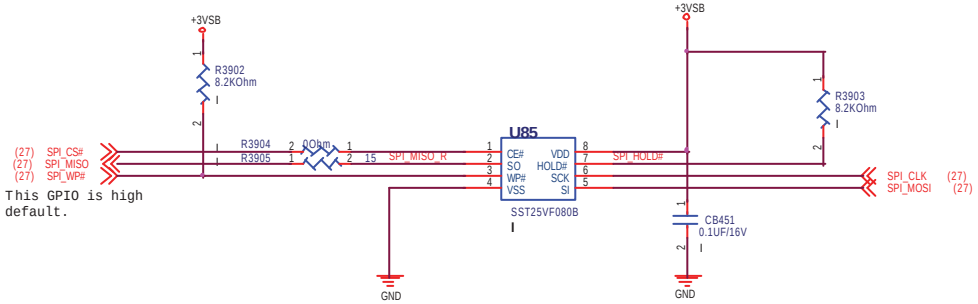
Why need two the same function
pin

1.00 A0-A3 ID Pin
If this FLASH want to boot
It must be 0000

1.00 WE# Write Enable

1.00 LAD0 - LAD3 Data
In/Out

SPI BIOS ROM



This GPIO is high
default.

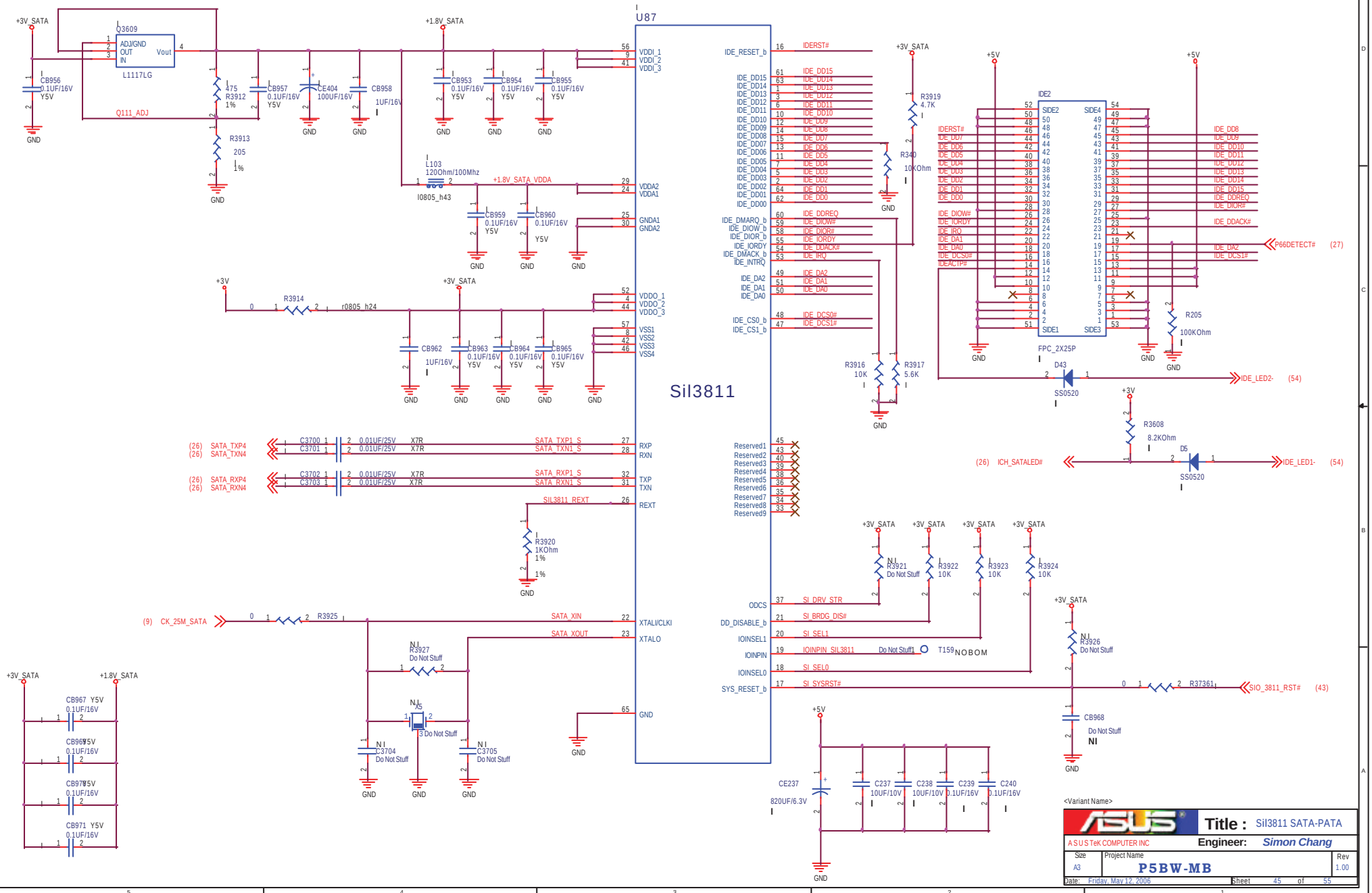
SOCKET 12G048000080

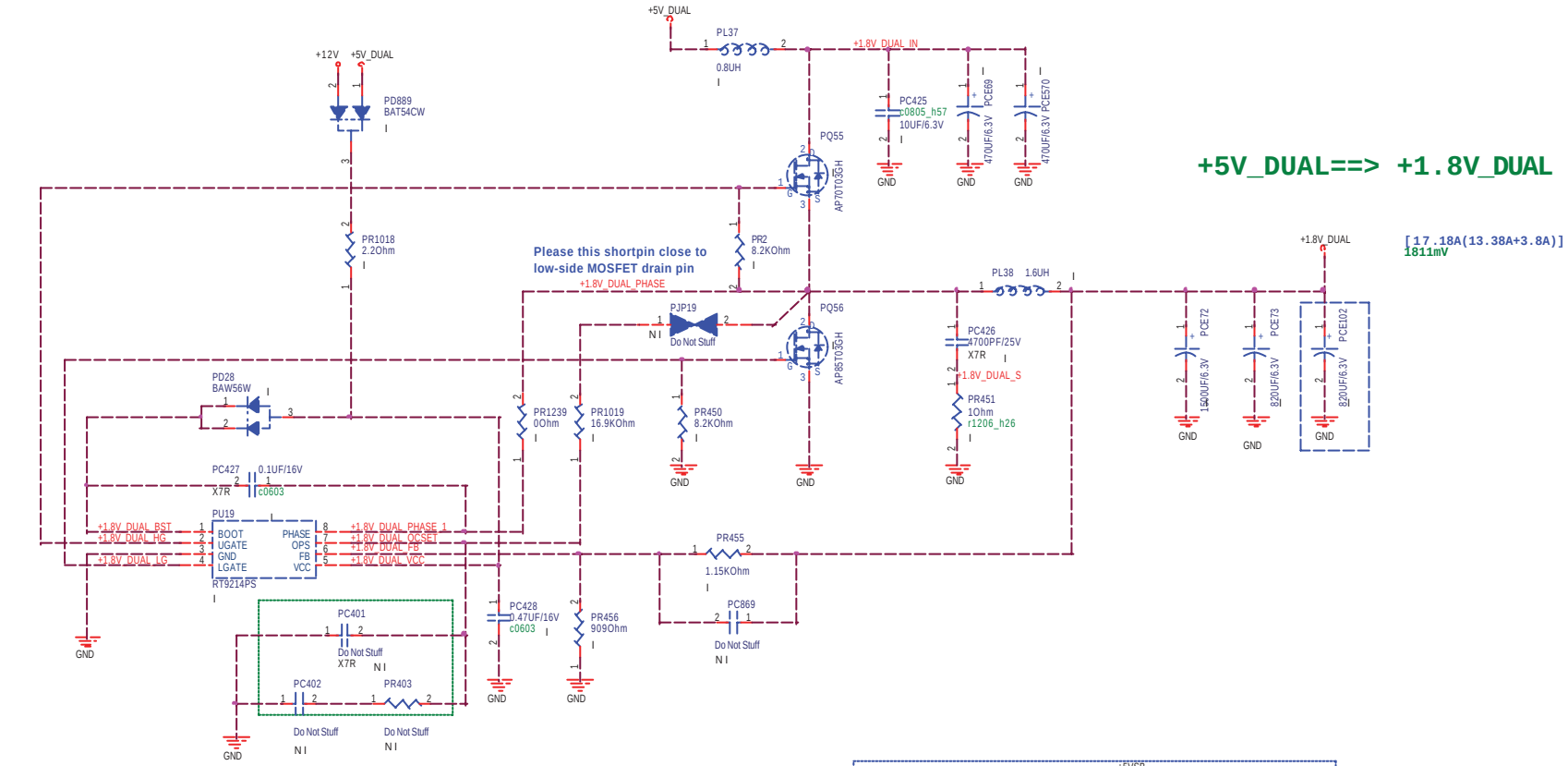
SPI ROM 05G00120A010

<Variant Name>

ASUSTeK COMPUTER INC	Title : SPI/FWH BIOS	
	Engineer: Simon Chang	
Size: A3	Project Name: P5BW-MB	Rev: 1.00
Date: Friday, May 12, 2006	Sheet 44 of 55	

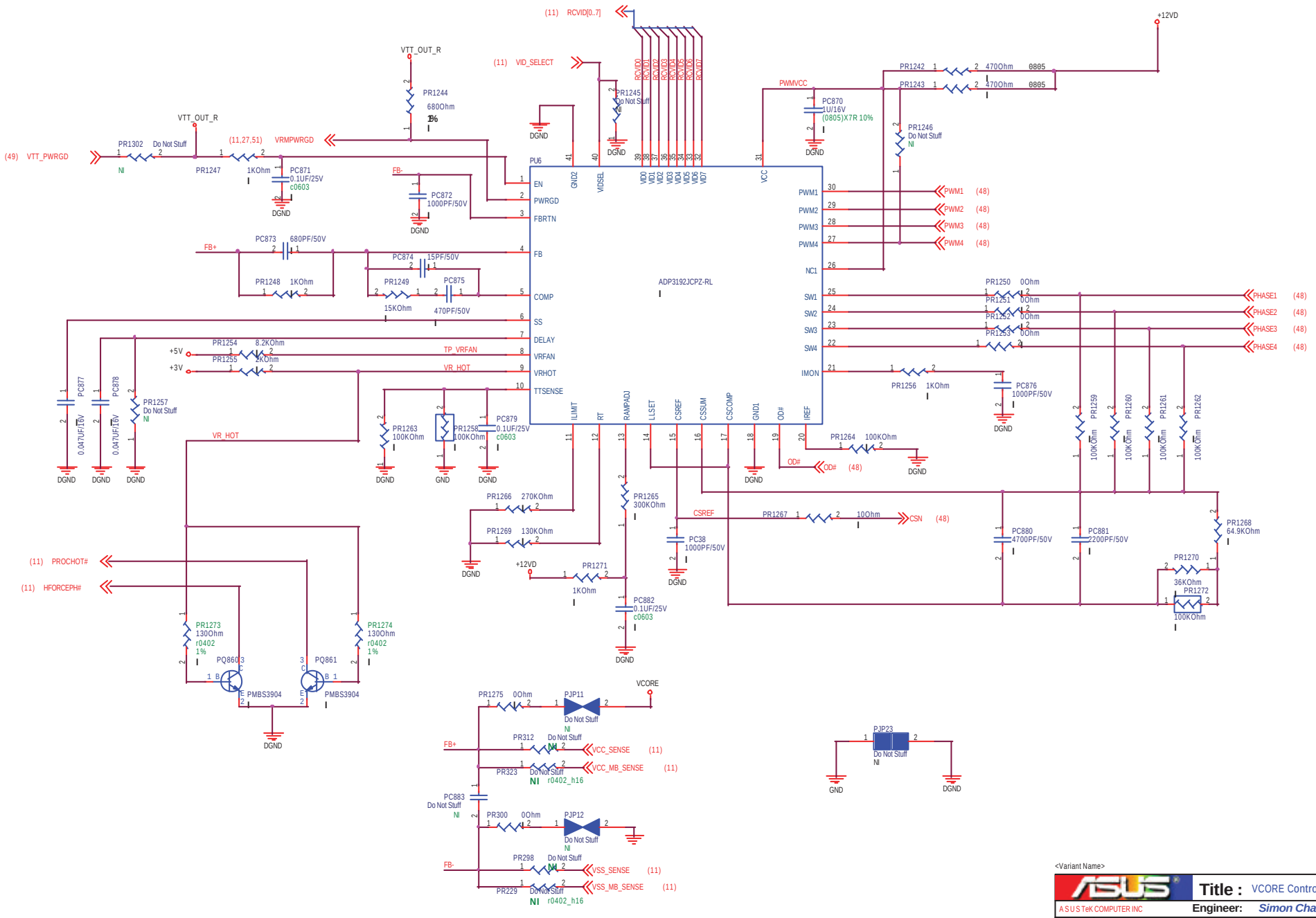
The voltage difference between 1.8V and 3.3V supplies must never be greater than 2.0V

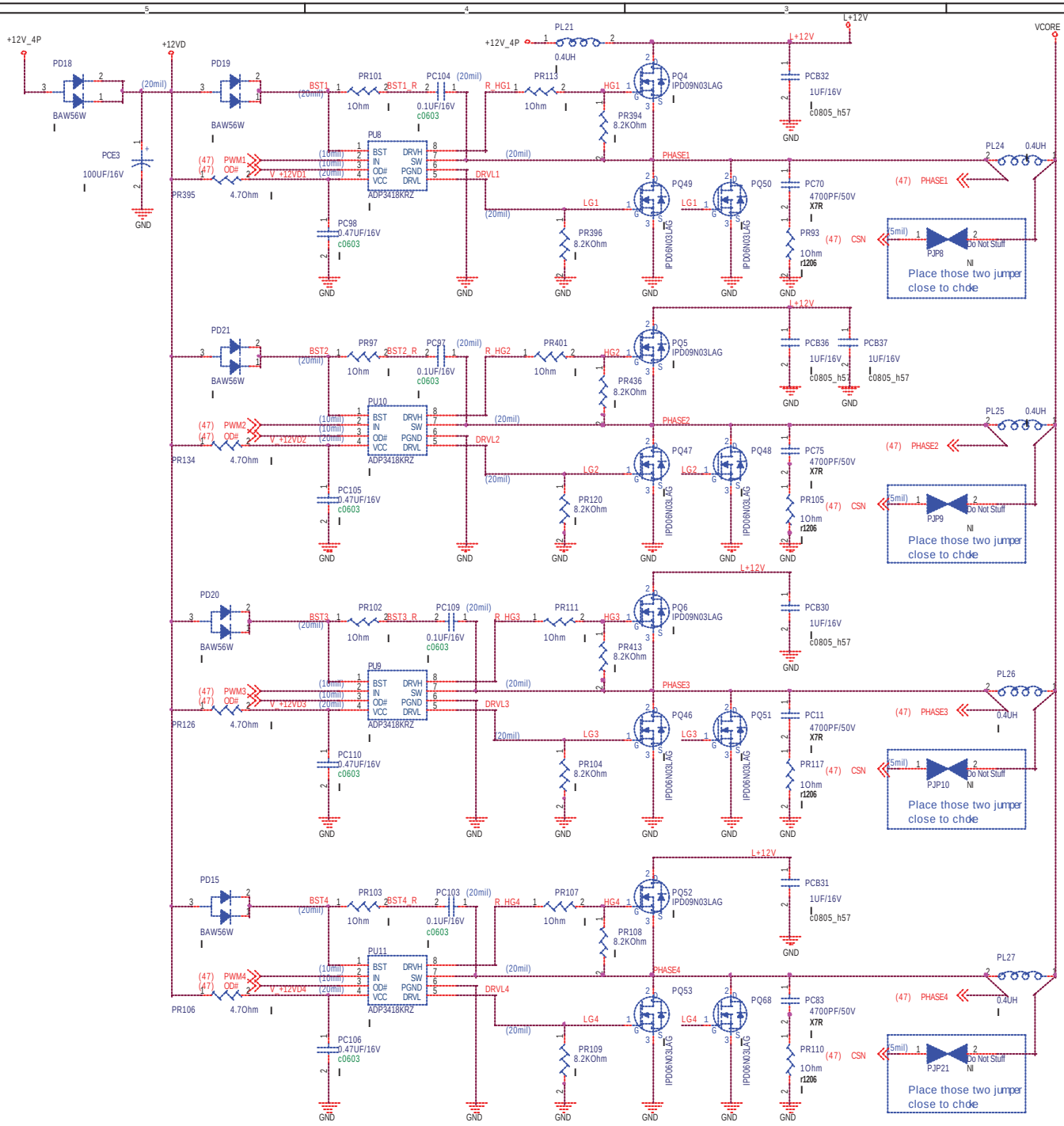




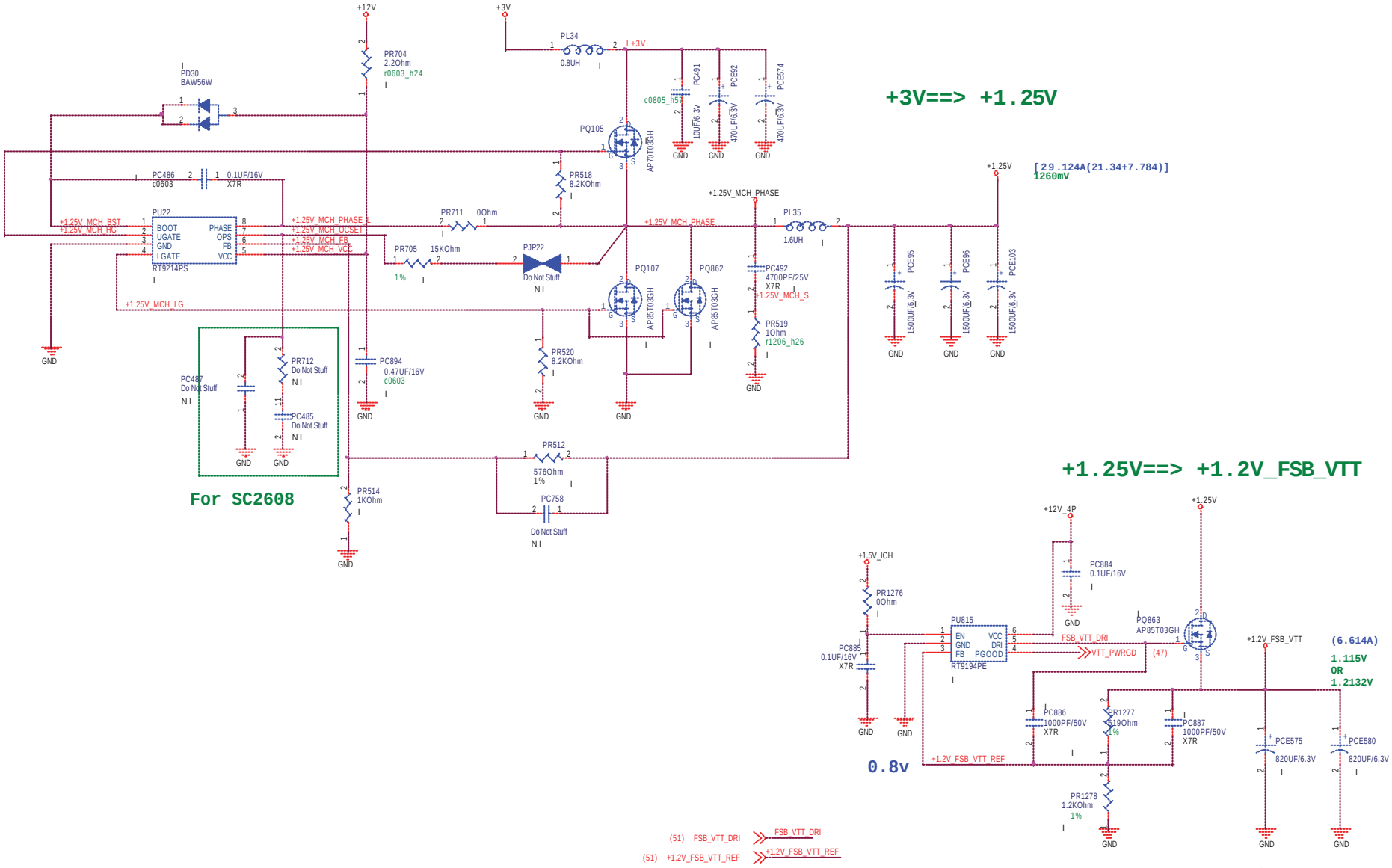
<Variant Name>

Title :	+1.8V_DUAL
A S U S TeK COMPUTER INC	Engineer: Simon Chang
Size: A3	Project Name: P5BW-MB
Rev: 1.00	
Date: Friday, May 12, 2006	Sheet 46 of 55





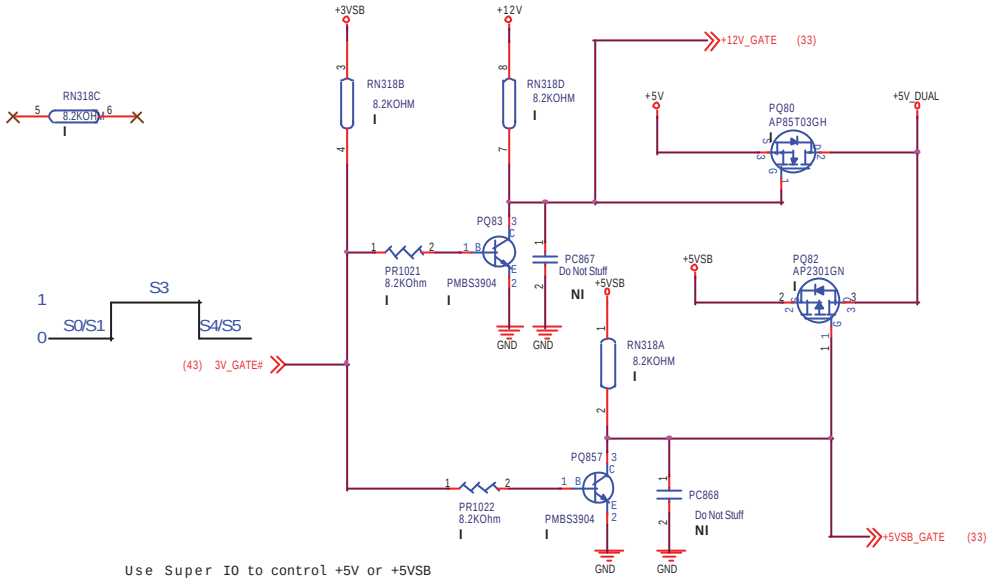
Title :	VCORE DRIVER
A S U S TeK COMPUTER INC	Engineer: Simon Chang
Size: A3	Project Name: P5BW-MB
Rev: 1.00	
Date: Friday, May 12, 2006	Sheet 48 of 55



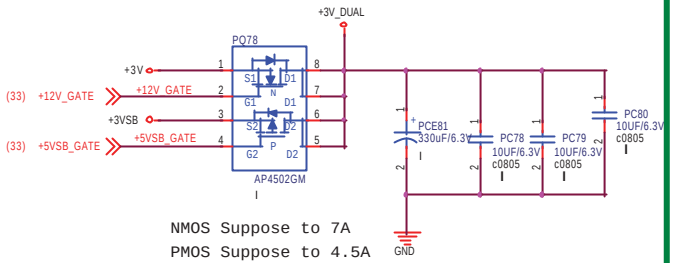
<Variant Name>

ASUS	Title : +1.25V GMCH CORE	
A S U S TeK COMPUTER INC	Engineer: Simon Chang	
Size: A3	Project Name: P5BW-MB	Rev: 1.00
Date: Friday, May 12, 2006	Sheet 49 of 55	

+5V_DUAL VOLTAGE SWITCH & POWER CIRCUIT

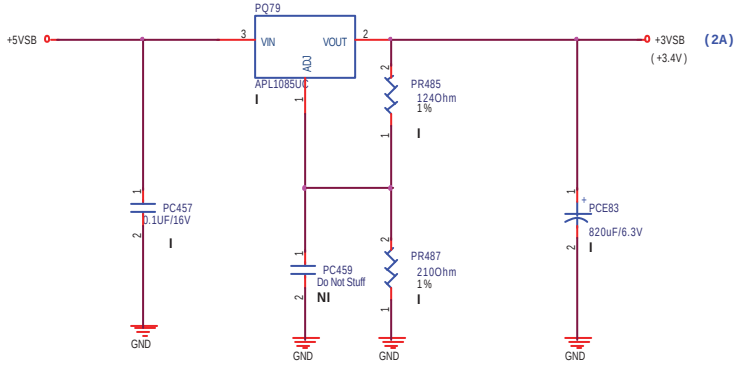


+3V & +3VSB ===>+3V_DUAL
For CLK gen & UPD72874GC



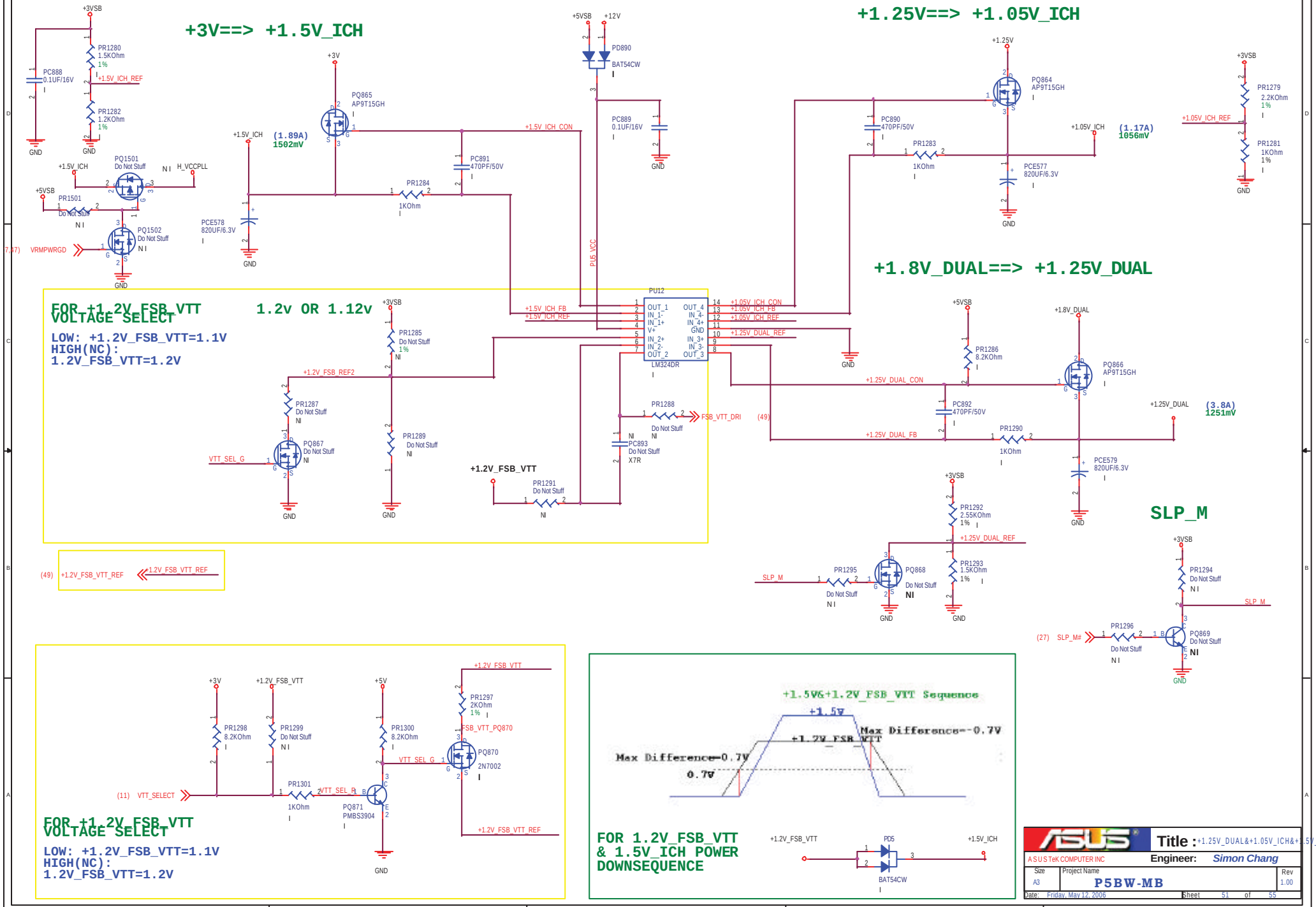
NMOS Suppose to 7A
PMOS Suppose to 4.5A

+5VSB ====>+3VSB

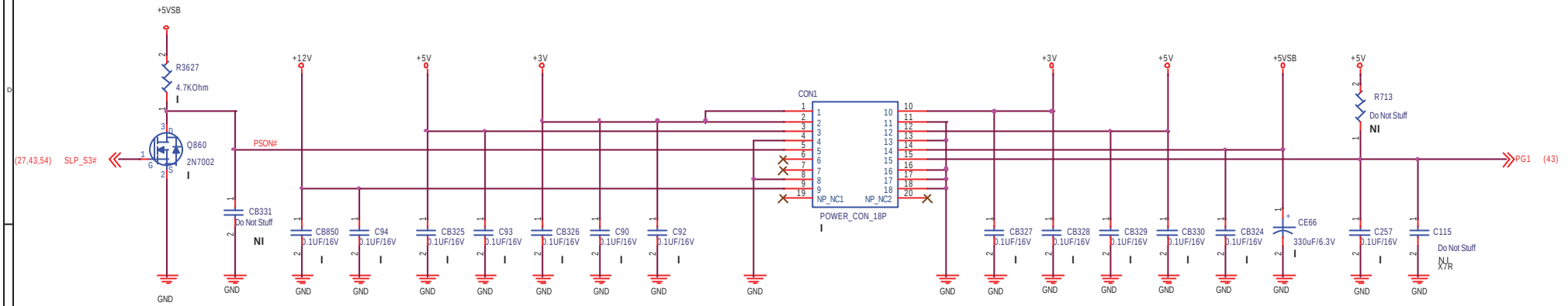


<Variant Name>

ASUS	Title :	+3V_DUAL&+5V_DUAL&+3VSB
A S U S TeK COMPUTER INC	Engineer:	Simon Chang
Size: A3	Project Name: P5BW-MB	Rev: 1.00
Date: Friday, May 12, 2006	Sheet 50 of 55	

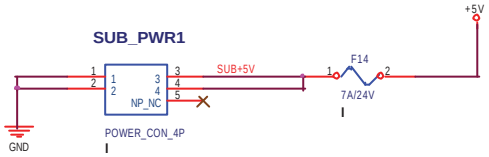


ATX POWER SUPPLY CONNECTOR



Around the ATX Power Connector

Around the ATX Power Connector

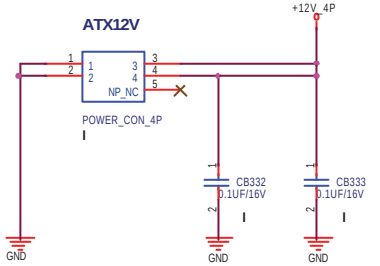


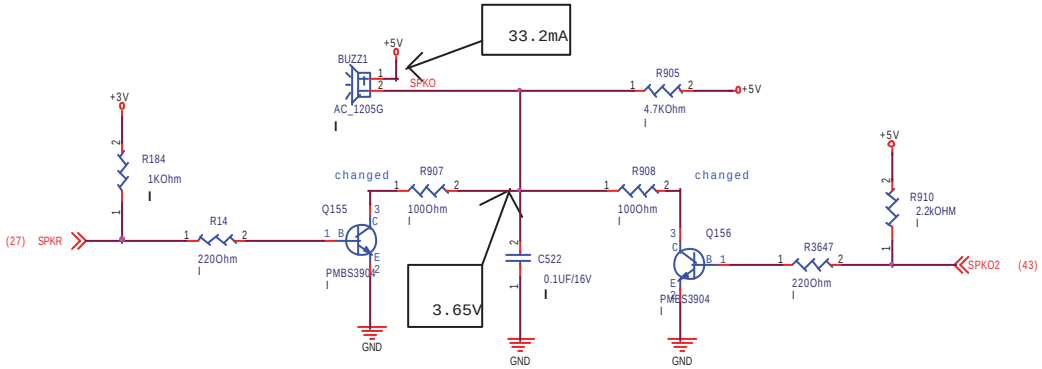
SUB POWER CON FOR Digital tuner(US VERSION)

PCB

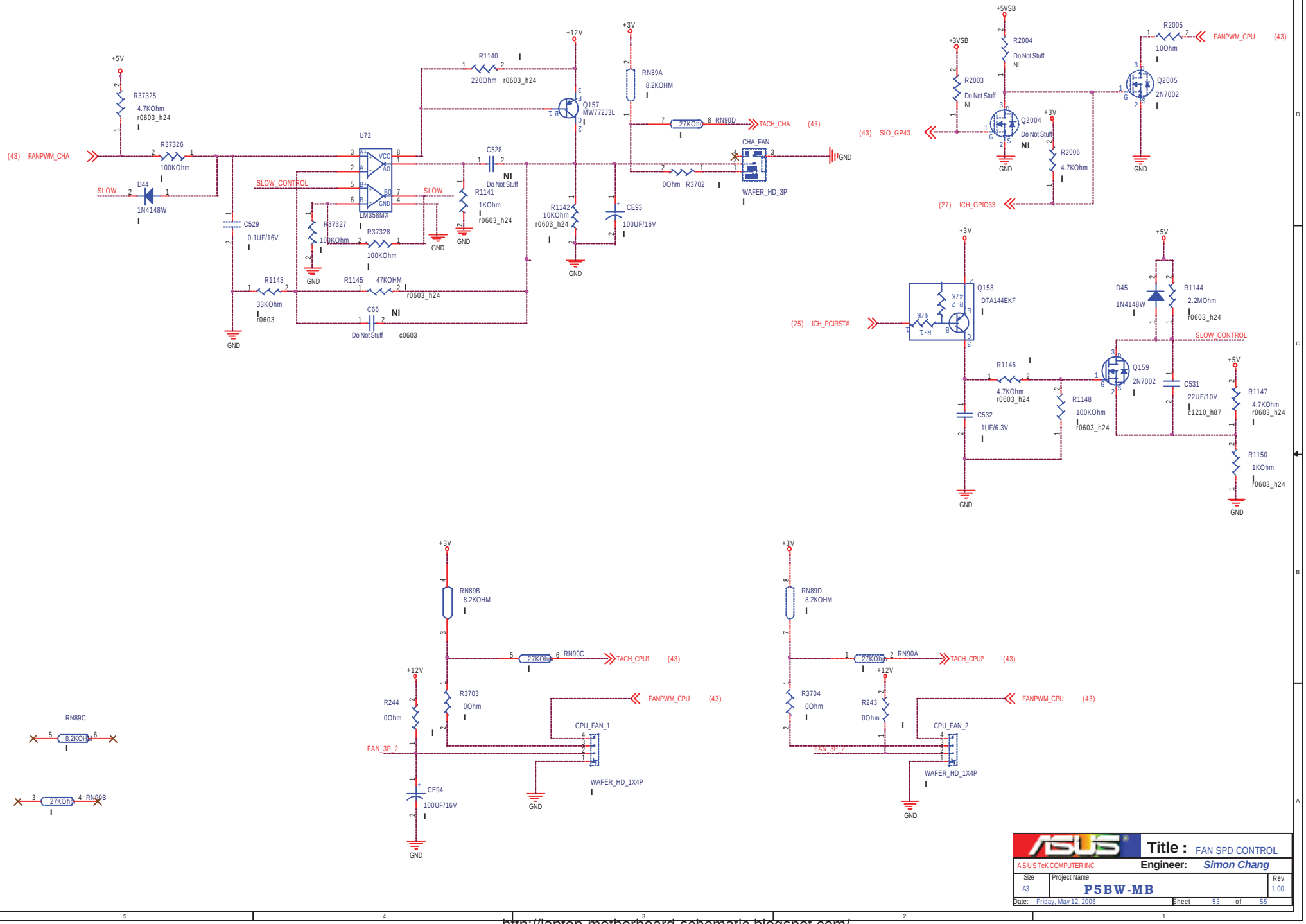
P5BW-MB R100

VRM POWER SUPPLY CONNECTOR

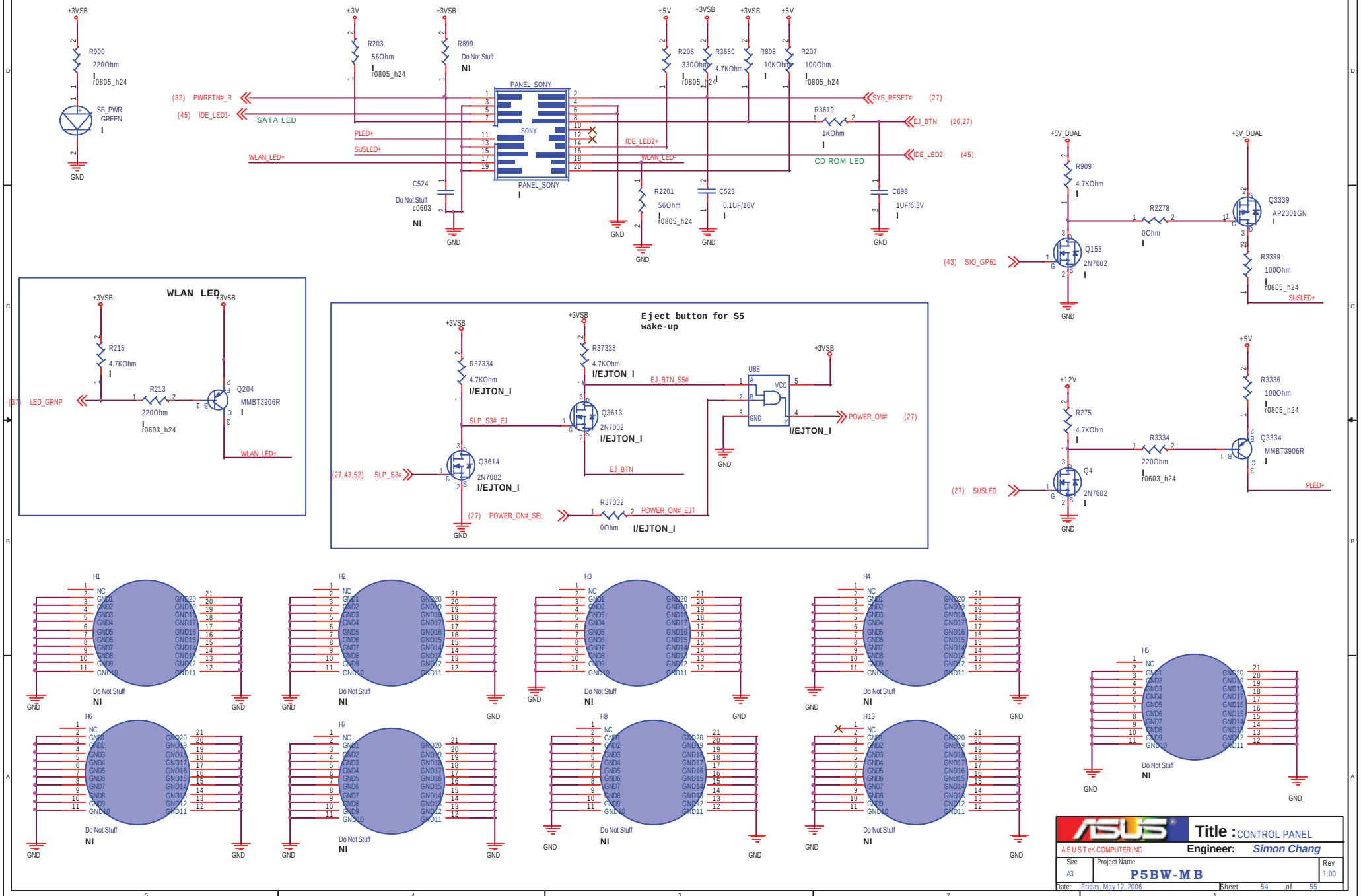




ASUSTeK COMPUTER INC	Title : ATX POWER CONN.		
	Engineer: Simon Chang		
Size: A3	Project Name: P5BW-MB		Rev: 1.00
Date: Friday, May 12, 2006	Sheet 52 of 55		



CONTROL PANEL / LED CIRCUITRY



ASUSTeK COMPUTER INC

Title : CONTROL PANEL

Engineer: Simon Chang

Size	Project Name	Rev
A3	P5BW-MB	1.00

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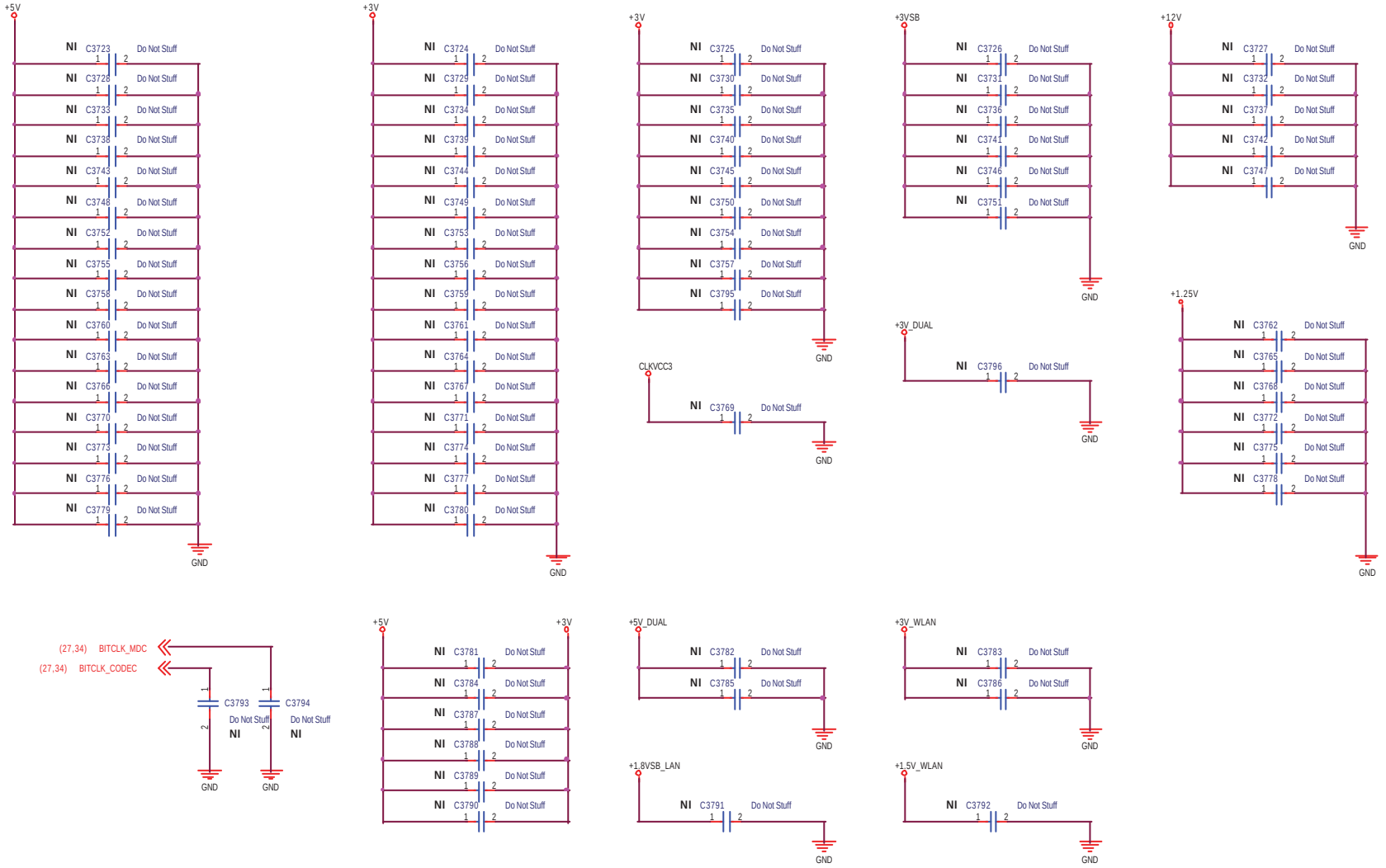

ASUS	Title : EMI CAP.	
A S U S TeK COMPUTER INC	Engineer: Simon Chang	
Size: A3	Project Name: P5BW-MB	Rev: 1.00
Date: Friday, May 12, 2006	Sheet 55 of 55	