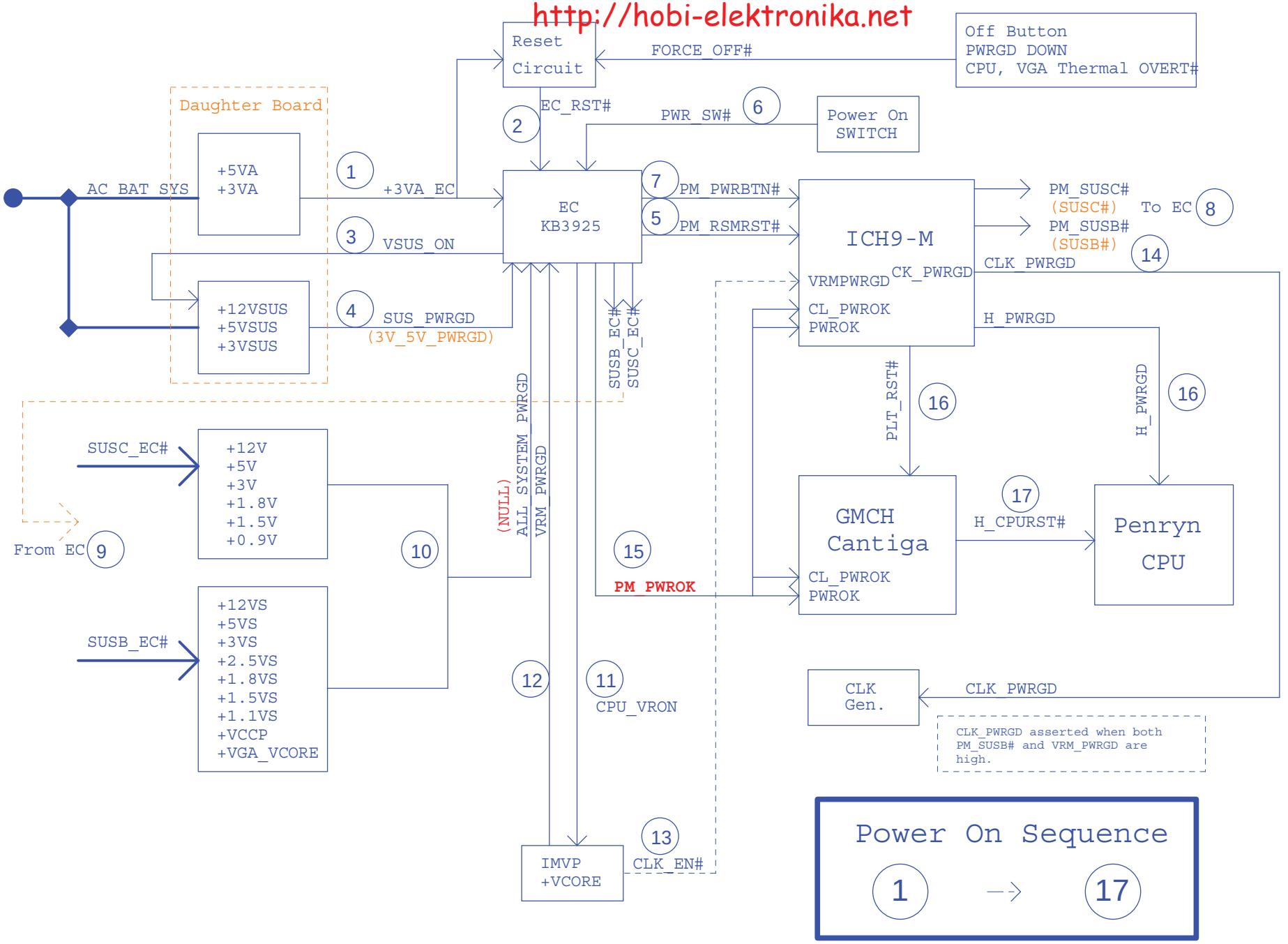
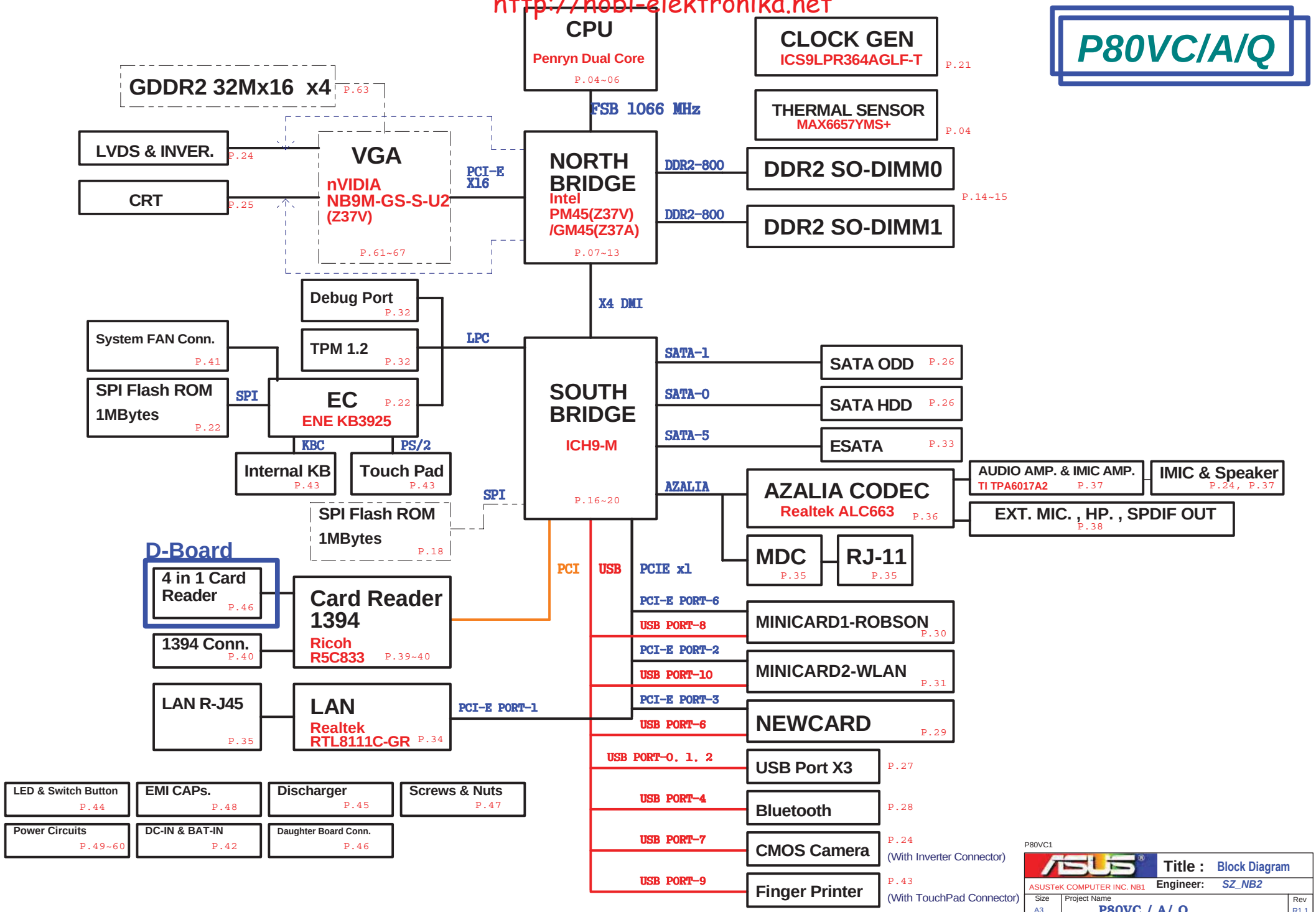


P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Power-On Sequence	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 1 of 52	

P80VC/A/Q



P80VC1

ASUSTeK COMPUTER INC. NB1

Title : Block Diagram

Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 2 of 52

Z37V/A Schematic Index

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32	POWER-ON SEQUENCE
33	Realtek RTL8111C
34	RJ45 + RJ11
35	MDC
36	ALC663 Codec
37	AUDIO_G1431 & HP
38	MICROPHONE & Array MIC
~~39~~	~~FM2010 DSP~~
40	CARDBUS R5C833(PCI I/F)
41	CARDBUS R5C833(1394 & SD)
42	IEEE1394A & 4 IN1 CON
43	NewCard PWR SW & CON
44	Debug
45	LVDS & INVERTER CONNECTOR
46	CRT
48	HDMI
50	THER SENSOR & FAN
51	HDD & CDROM
52	USB Port x 4
53	MINICARD(Ebron/Robson/3G/TV)
~~54~~	~~PORT Docking~~
~~55~~	~~Super I/O & FIR~~
56	LED/TP/SW
57	DISCHARGE
58	UMB
60	DC power jack, Batter conn.
61	Blue Tooth
62	TPM
63	Finger Print
65	MDC NUT & Hinksink NUT
66	E-SATA
68	XDP
70-77	VGA (nVidia NB9P-GE)
80	POWER_VCORE
81	POWER_SYSTEM
82	POWER_I/O_1.5V & 1.05VM
83	POWER_I/O_DDR & VTT
84	NONE
85	POWER_VGA_VCORE & 1.1VO
88	POWER_CHARGER
90	POWER_DETECT
91	POWER_LOAD SWITCH
92	POWER_PROTECT
93	POWER_SIGNAL
94	POWER_FLOWCHART

GPIO33 Internal Pull High, Go Low= Flash
Descriptor Security will be overriden

ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	Native	PMSYNC#	+3VS
GPIO 01	GPI	- EXT PU to +3VS	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	+5VS
GPIO 06	GPI	**WLBT_SW#** EXT PU	+3VS
GPIO 07	GPI	-	+3VS
GPIO 08	GPI	EXT_SMI# EXT PU	+3VSUS
GPIO 09	Native	WOL_EN EXT PD	+3VSUS
GPIO 10	GPI	**RTLAN_DSM#** EXT PU	+3VSUS
GPIO 11	Native	SMBALERT# EXT PU	+3VSUS
GPIO 12	GPI	EXT_SCI# EXT PU	+3VSUS
GPIO 13	GPI	-	+3VSUS
GPIO 14	Native	AC_PRESENT EXT PU	+3VSUS
GPIO 15	Native	STP_PCI#	+3VSUS
GPIO 16	Native	PM_DPRSLPVR INT PD*	+3VS
GPIO 17	GPI	-	+3VS
GPIO 18	GPO	**GPU_PWR_SB** EXT PU NS	+3VS
GPIO 19	GPO	BT_LED EXT PU NS	+3VS
GPIO 20	GPO	**GPU_RST_SB#** EXT PU NS	+3VS
GPIO 21	GPO	WLAN_LED EXT PU NS	+3VS
GPIO 22	GPI	**ODC#** EXT PU	+3VS
GPIO 23	Native	LPC_LDRQ1# INT PU*	+3VS
GPIO 24	GPO	-	+3VSUS
GPIO 25	Native	STP_CPU#	+3VSUS
GPIO 26	Native	PM_S4_STATE#	+3VSUS
GPIO 27	GPO	-	+3VSUS
GPIO 28	GPO	-	+3VSUS
GPIO 29	Native	USB_OC5# EXT PU	+3VSUS
GPIO 30	Native	USB_OC6#	+3VSUS
GPIO 31	Native	USB_OC7# EXT PU	+3VSUS
GPIO 32	GPO	PM_CLKRUN# EXT PU	+3VS
GPIO 33	GPO	- INT PU*	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	-	+3VS
GPIO 36	GPO	WLAN_ON EXT PU NS	+3VS
GPIO 37	GPO	BT_ON EXT PU NS	+3VS
GPIO 38	GPI	-	+3VS
GPIO 39	GPO	**CLK_PWRSAVE#** EXT PU	+3VS
GPIO 40	Native	USB_CON_OC01#	+3VSUS
GPIO 41	Native	USB_CON_OC2#	+3VSUS
GPIO 42	Native	USB_OC3# EXT PU	+3VSUS
GPIO 43	Native	USB_OC4# EXT PU	+3VSUS
GPIO 44	Native	USB_OC8# EXT PU	+3VSUS
GPIO 45	Native	USB_OC9# EXT PU	+3VSUS
GPIO 46	Native	USB_OC10# EXT PU	+3VSUS
GPIO 47	Native	USB_OC11# EXT PU	+3VSUS
GPIO 48	GPI	-	+3VS
GPIO 49	GPO	- INT PU* EXT PU to +3VS	+3VS
GPIO 50	Native	PCI_REQ#1	+5VS
GPIO 51	Native	PCI_GNT#1 INT PU* EXT PU to +3VS	+3VS
GPIO 52	Native	PCI_REQ#2	+5VS
GPIO 53	Native	PCI_GNT#2 INT PU* EXT PU to +3VS	+3VS
GPIO 54	Native	PCI_REQ#3	+5VS
GPIO 55	Native	PCI_GNT#3 INT PU*	+3VS
GPIO 56	GPI	- EXT PU	+3VSUS
GPIO 57	GPI	- EXT PU	+3VSUS
GPIO 58	GPI	SPI_CS#1 INT PU*	+3VSUS
GPIO 59	Native	USB_CON_OC01#	+3VSUS
GPIO 60	Native	PM_LINKALERT# EXT PU	+3VSUS

INT PU*: PU or PD in special time

EC GPIO	Use As	Signal Name	Power
GPIO02	GPO	PM_RSMRST#	
GPIO03	GPO	LCD_BACKOFF#	
GPIO04	GPI	EMAIL_SW#	
GPIO06	-	-	
GPIO07	-	-	
GPIO08	GPO	EXT_SMI#	
GPIO09	-	-	
GPIO0A	GPI	LID_EC#	
GPIO0B			
GPIO0C			
GPIO0D	GPI	DISTP_SW#	
GPIO11	GPO		
GPIO18			
GPIO19			

EC GPIO	Use As	Signal Name	Power

P80VC1

ASUSTeK COMPUTER INC. NB1

Title : System Information

Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 3 of 52

R1.1 KL99 FOR P80Q
R1.1 KL1 FOR P80VC/A

+3V KL99 120Ohm/100Mhz /AMT
+3VM /AMT KL1 120Ohm/100Mhz
+3VS_CLK KC7 Do Not Stuff /X; KC8 10UF/6.3V; KC9 0.1UF/10V; KC10 0.1UF/10V; KC11 0.1UF/10V; KC12 0.1UF/10V; KC30 0.1UF/10V; KC31 0.1UF/10V
KL3 120Ohm/100Mhz
+3VS_CLKA KC2 0.1UF/10V
GND

+1.5VS KL2 120Ohm/100Mhz
+1.5VS_CLK KC1 Do Not Stuff /X; KC3 10UF/6.3V; KC4 0.1UF/10V; KC6 0.1UF/10V
R1.1
GND

KR1 Do Not Stuff
KX1 14.318Mhz +/-30ppm/20PF H = 1.2mm
XIN_CLK KC13 30PF/50V
XOUT_CLK KC14 30PF/50V
GND

Tuning Cap. @ device sides

CLK_27M_GPU KC24 Do Not Stuff/X
CLK_27M_GPU_SS KC25 Do Not Stuff/X
CLK_48M_SB KC18 Do Not Stuff/X
CLK_33M_TPM KC22 Do Not Stuff/X
CLK_33M_EC KC23 Do Not Stuff/X
CLK_33M_SB KC19 Do Not Stuff/X
CLK_33M_DBG2 KC20 Do Not Stuff/X
CLK_14M_ICH KC17 Do Not Stuff/X
GND

Close the end of devices

Close to CLK GEN

SMB_CLK_M
SMB_DAT_M
KC15 Do Not Stuff /X
KC16 Do Not Stuff /X
GND

+3VS_CLKA +1.5VS_CLK +3VS_CLK

KU1
VDDSRC_1 VDDSRC_IO1 VDDSRC_IO2 VDDPCI_1 VDDPCI_2 VDD48 VDDREF
**FUC → To ICH9 GPIO45
VDDCPU VDDA GNDA
XIN_CLK X1
XOUT_CLK X2
CLK_100M_LVDS 33Ohm 2 KRN8A /GM
CLK_27M_GPU 33Ohm 2 KRN11A /PM
CLK_27M_FIX → 27MHZ/LCD_SSCG/SRC-0
CLK_100M_LVDS# 33Ohm 4 KRN8B /GM
CLK_27M_GPU_SS 33Ohm 4 KRN11B /PM
CLK_27M_SS → 27MHZSS/LCD_SSCG#/SRC-0#
CLK_48M_CR KR29 33Ohm
CLK_48M_SB KR17 33Ohm CLK_48M → **FSLA/USB_48MHz
FSLA
CLK_48M_SB,CLK_48M_CR layout 時 trace 長度相等
FSLB → **FSLB/TEST_MODE
LCDCK_SEL → *SELSRC0_LCD#/PCI-3
CLK_33M_TPM KR32 33Ohm CLK_33M2 → PCI-2
PCI-1
CLK_33M_DBG2 KR26 33Ohm REQ_SEL# → **PCI-0/REQ_SEL
SEL_27M#
CLK_33M_SB KR27 33Ohm CLK_33M_F1 → *SELLCD_27#/PCIF-1
EN_ITPCLK
CLK_33M_EC KR28 33Ohm CLK_33M_F0 → **ITP_EN/PCIF-0
SMB_CLK_M → SCLK
SMB_DAT_M → SDATA
FOC → **FOC
To ICH9 GPIO44
GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7
RTM875T-336-GRT

R1.1
**PCI_SRC_STOP# → STP_PCI#
**CPU_STOP# → STP_CPU#
CPU-1 CPUCLK1 33OHM 2 KRN1A → CLK_MCH_BCLK
CPU-1# CPUCLK1# 33OHM 4 KRN1B → CLK_MCH_BCLK#
CPU-0 CPUCLK0 33OHM 2 KRN14A → CLK_CPU_BCLK
CPU-0# CPUCLK0# 33OHM 4 KRN14B → CLK_CPU_BCLK#
CPUITP/SRC-8 CPUCLK2 33OHM 2 KRN3A → CLK_XDP_BCLK
CPUITP#/SRC-8# CPUCLK2# 33OHM 4 KRN3B /ITP → CLK_XDP_BCLK#
*SRC_REQ1#/SRC-7 → LAN_CLKREQ#
*SRC_REQ2#/SRC-7# → MCH_CLKREQ#
R1.1 Remove 0ohm
SRC-6 CLK_PCIE6 33OHM 2 KRN2A → CLK_PCIE_LAN
SRC-6# CLK_PCIE6# 33OHM 4 KRN2B → CLK_PCIE_LAN#
SRC-5 CLK_PCIE5 33OHM 2 KRN6A → CLK_100M_NEW
SRC-5# CLK_PCIE5# 33OHM 4 KRN6B → CLK_100M_NEW#
SRC-4 CLK_PCIE4 33OHM 4 KRN13B → CLK_100M_MIN1
SRC-4# CLK_PCIE4# 33OHM 2 KRN13A → CLK_100M_MIN1#
SRC-3 CLK_PCIE3 33OHM 4 KRN9B → CLK_PCIE_GPU
SRC-3# CLK_PCIE3# 33OHM 2 KRN9A /PM → CLK_PCIE_GPU#
SRC-2 CLK_PCIE2 33OHM 4 KRN15B → CLK_PCIE_ICH
SRC-2# CLK_PCIE2# 33OHM 2 KRN15A → CLK_PCIE_ICH#
SRC-1 CLK_PCIE1 33OHM 4 KRN7B → CLK_PCIE_NB
SRC-1# CLK_PCIE1# 33OHM 2 KRN7A → CLK_PCIE_NB#
SATA CLK_SATA 33OHM 4 KRN16B → CLK_SATA_SB
SATA# CLK_SATA# 33OHM 2 KRN16A → CLK_SATA_SB#
SRC-9/DOT96 CLK_96M 33OHM 4 KRN10B → CLK_96M_NB
SRC-9#/DOT96# CLK_96M# 33OHM 2 KRN10A /GM → CLK_96M_NB#
R1.1
*SRC_REQ3# → WLAN_CLKREQ#
*SRC_REQ4# → NEW_CLKREQ#
**VtlPWR_GD/PD# CLK_PWRGD KR35 0Ohm → SB_CLKPWRGD
KR36 Do Not Stuff /X → EC_CLKPWRGD
**REF-1/FSLC/TEST_SEL FSLC REF-0 KR24 33Ohm → CLK_14M_ICH

*INT-PU 120K ohm
**INT-PD 120K ohm.

PEREQ1# for SATA,SRC-0, SRC-6(LAN:PCIE6)
PEREQ2# for SRC-1, SRC-8(NC)
PEREQ3# for SRC-2,SRC-4(WLAN PCIE4)
PEREQ4# for SRC-3,SRC-5, SRC-7(NEWCARD PCIE5)

FSB Freq. Strap

FSC	FSB	FSA	CPU
0	0	0	266
0	0	1	133
0	1	0	200
0	1	1	166
1	0	0	333
1	0	1	100
1	1	0	400
1	1	1	200

FSLA KR5 10KOhm CPU_BSEL0
FSLB KR6 10KOhm CPU_BSEL1
FSLC KR7 10KOhm CPU_BSEL2

LCDCK_SEL	SEL_27M#				
PIN 5 (IPU)	PIN 9 (IPU)	PIN14, 15	PIN17	PIN18	
0	0	SRC-9	27FIX	27SS	
0	1	DOT96	DOT96SS	DOT96SS	
1	0	DOT96	27FIX	27SS	/PM
1	1	DOT96	SRC-0	SRC-0	/GM

R1.1 +3VS_CLK KR33 10KOhm /GM; KR8 10KOhm /PM SEL_27M# GND
R1.1 +3VS_CLK KR34 10KOhm; KR9 Do Not Stuff LCDCK_SEL GND

PIN 8 ITP_EN/PCIF-0
Select PIN43, 44 as CPUITP or SRC8
R1.1 +3VS_CLK KR20 10KOhm; KR10 Do Not Stuff EN_ITPCLK GND
0 :SRC8
1 :CPUITP

PIN 64 (IPD)PCI-0/REQ_SEL
Select PIN40, 41 as SRC_REQ# or SRC7
R1.1 +3VS_CLK KR15 10KOhm REQ_SEL#
0 :SRC-7
1 :SRC_REQ#

P80VC1
ASUSTeK COMPUTER INC. NB6
Title : Main Clock-1
Engineer: SZ_NB2
Size A2 | Project Name P80VC / A/ Q | Rev R1.1
Date: Tuesday, December 16, 2008 | Sheet 4 of 52

CPU1A

SOCKET478B

12G010594786

CPU1B

SOCKET478B

12G010594786

Zo=55 Ohm, 0.5" max for GTL_REF

Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
Comp 1,3: Z0=55 Ohm, trace length < 0.5"

AC mode : check PWRLIMT#
DC mode : check battery OTP / OCP

R1.1
Remove THRO_CPU from EC

SM Bus Address fix at:
1001 100x (98, 99),
Resolution : +/- 1 degree

ITP

BTOB_CON_31P
/ITP

12G161300310

Stuff when use ITP : HR12, HR13, HR14, HR17, HR18, HR19, HR20, HR21, HR22, HR23, HR24, KRN3

HR12, HR13, HR30, HR31 Place close to CPU

CPU Thermal Sensor

HU1
MAX6657YMS+

Place close to CPU Pin
Max: 1mA

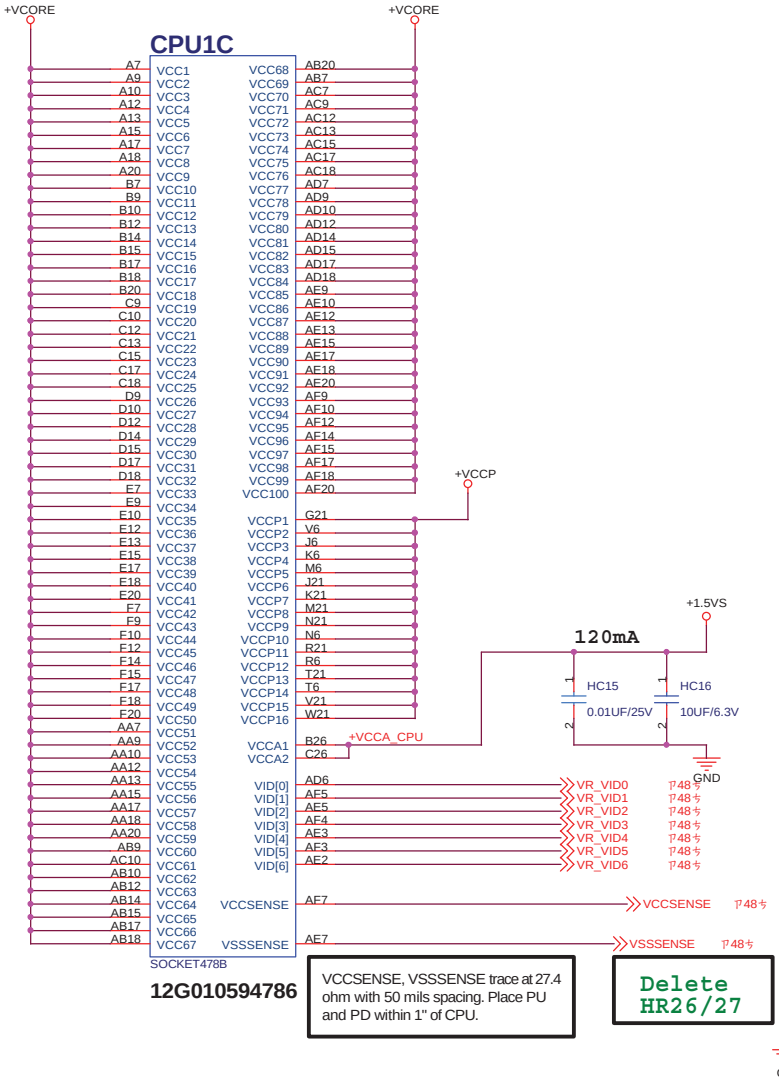
Route H_THERMDA and H_THERMDC in the same layer

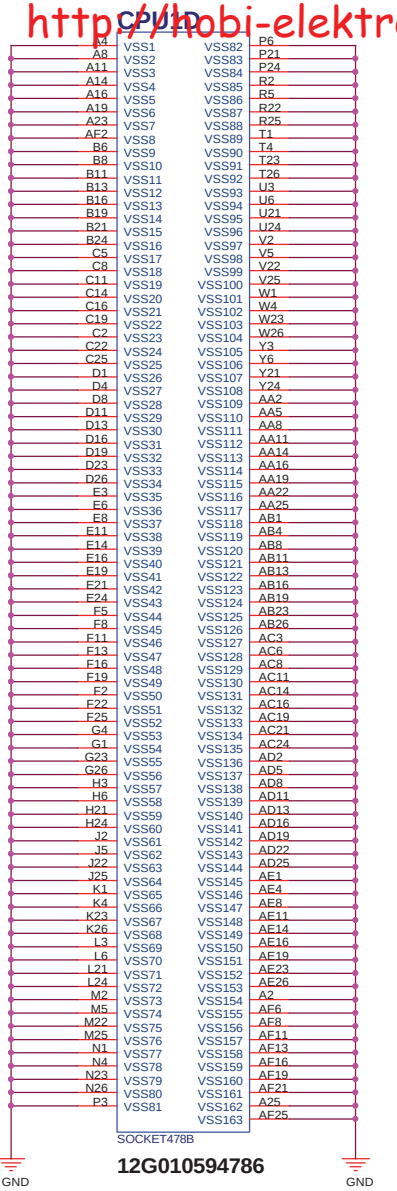
----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
==========GND
15 mils
----------OTHER SIGNALS

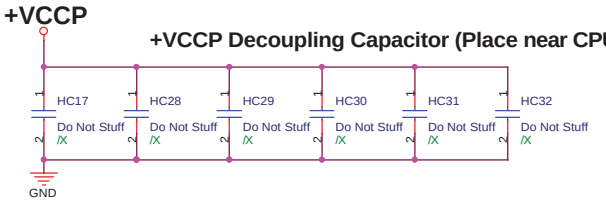
Avoid FSB,Power

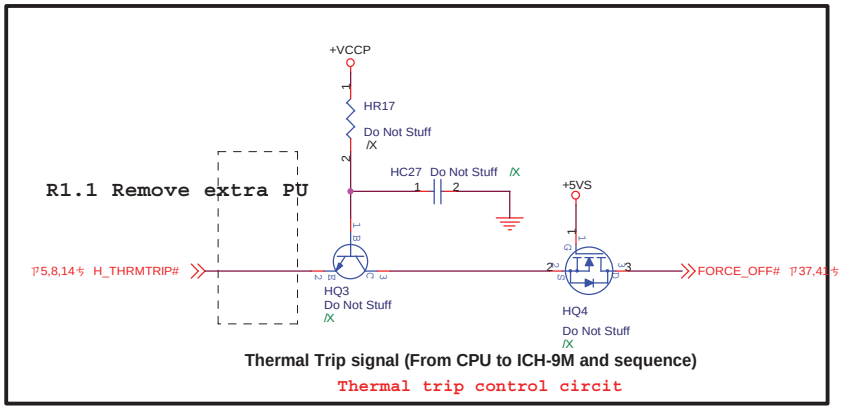
P80VC1

Title : CPU-Penryn (1)
ASUSTeK COMPUTER INC. NB1
Engineer: SZ_NB2
Size: A3
Project Name: P80VC / A/ Q
Rev: R1.1
Date: Tuesday, December 16, 2008
Sheet 5 of 52



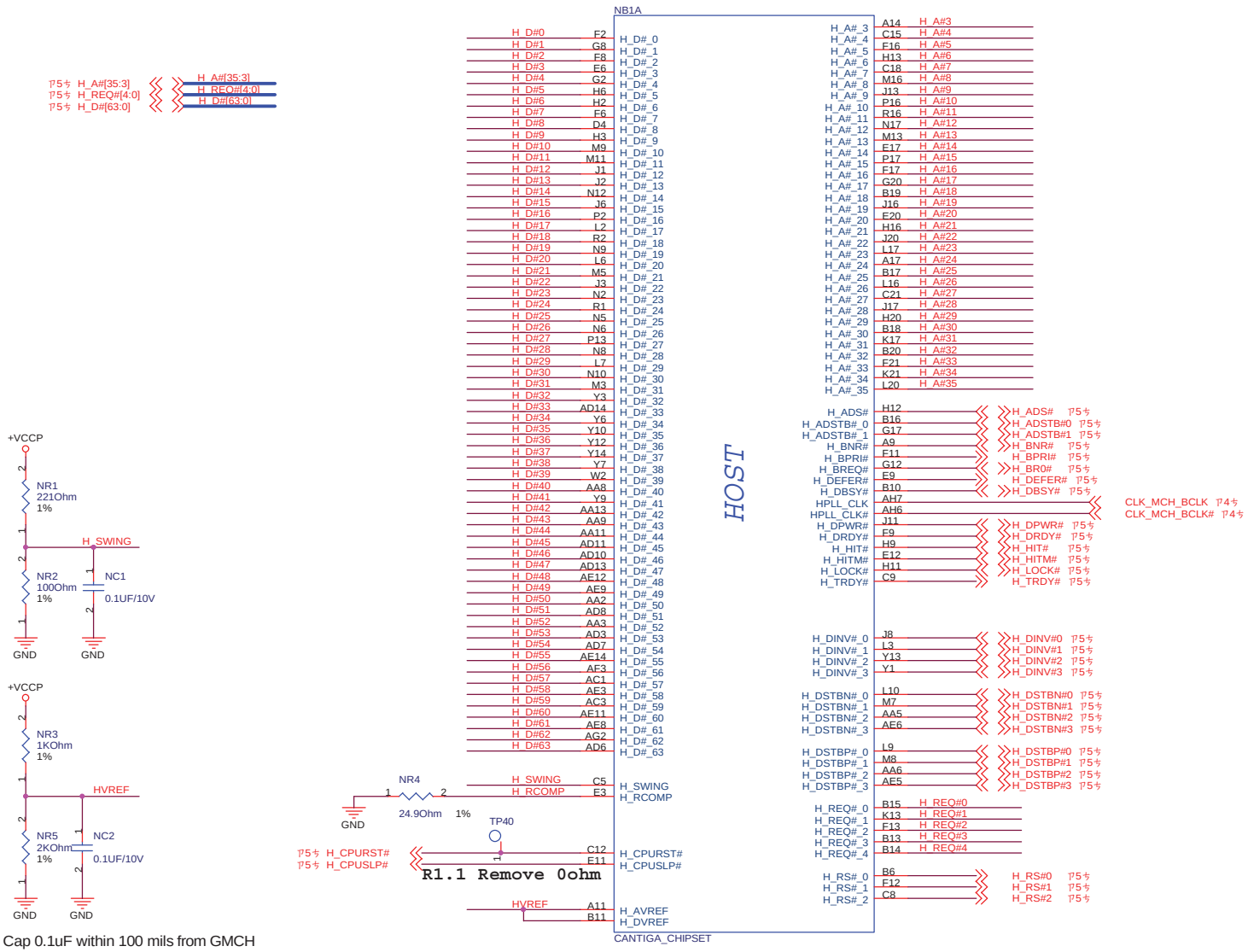






P80VC1

ASUSTeK COMPUTER INC. NB1	Title : CPU-Penryn (2)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 6 of 52	



Cap 0.1uF within 100 mils from GMCH

BOM:
GM45:02G010020030
PM45:02G010022520
GL40:02G010023900
or 02G010017532

P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Cantiga - CPU(1)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 7 of 52	

CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2
CFG6 : Integrated TPM Host Interface
HIGH = iTPM disable (Default)
LOW = iTPM enable
CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite
HIGH = With confidentiality (Default)
LOW = Without confidentiality
CFG9 : PCIE GRAPHIC LANE
HIGH = Normal Operation (Default)
LOW = Reverse Lanes
CFG10 : PCIe Loopback
HIGH = Disable (Default)
LOW = Enable
CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)
CFG16 : FSB Dynamic ODT
HIGH = Ensable (Default)
LOW = Disable
CFG19 : DMI Lane Reversal
LOW = NORMAL (default)
HIGH = Reverse Lanes
CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (Default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

NB1B

RSVD: M36 RSVD1, N36 RSVD2, R33 RSVD3, T33 RSVD4, AH9 RSVD5, AH10 RSVD6, AH12 RSVD7, AH13 RSVD8, K12 RSVD9, AL34 RSVD10, AK34 RSVD11, AN35 RSVD12, AM35 RSVD13, T24 RSVD14, B31 RSVD15, AJ6 RSVD16, M1 RSVD17, AY21 RSVD20, A47 RSVD21, BG23 RSVD22, BF23 RSVD23, BH18 RSVD24, BF18 RSVD25

DDR CONTROL/COMPENSATION: SA_CK_0 AP24 M_A_CLK_0 ↱25↳, SA_CK_1 AT21 M_A_CLK_1 ↱25↳, SB_CK_0 AV24 M_B_CLK_0 ↱25↳, SB_CK_1 AU20 M_B_CLK_1 ↱25↳; SA_CK#_0 AR24 M_A_CLK_#0 ↱25↳, SA_CK#_1 AR21 M_A_CLK_#1 ↱25↳, SB_CK#_0 AU24 M_B_CLK_#0 ↱25↳, SB_CK#_1 AV20 M_B_CLK_#1 ↱25↳; SA_CKE_0 BC28 M_A_CKE0 ↱25,26↳, SA_CKE_1 AY28 M_A_CKE1 ↱25,26↳, SB_CKE_0 AY36 M_B_CKE0 ↱25,26↳, SB_CKE_1 BB36 M_B_CKE1 ↱25,26↳; SA_CS#_0 BA17 M_A_CS#0 ↱25,26↳, SA_CS#_1 AY16 M_A_CS#1 ↱25,26↳, SB_CS#_0 AV16 M_B_CS#0 ↱25,26↳, SB_CS#_1 AR13 M_B_CS#1 ↱25,26↳; SA_ODT_0 BD17 M_A_ODT0 ↱25,26↳, SA_ODT_1 AY17 M_A_ODT1 ↱25,26↳, SB_ODT_0 BF15 M_B_ODT0 ↱25,26↳, SB_ODT_1 AY13 M_B_ODT1 ↱25,26↳; SM_RCOMP BG22 M_RCOMP, SM_RCOMP# BH21 M_RCOMP#; SM_RCOMP_VOH BF28 SM_RCOMP_VOH, SM_RCOMP_VOL BH28 SM_RCOMP_VOL; SM_VREF AV42, SM_PWROK AR36, SM_REXT BF17 NR11 1 2 499Ohm 1% GND, SM_DRAMRST# BC36 M_DRAMRST# 1 TP41

CLK: DPLL_REF_CLK B38 CLK_96M_NB, DPLL_REF_CLK# A38 CLK_96M_NB#, DPLL_REF_SSCLK E41 CLK_100M_LVDS, DPLL_REF_SSCLK# F41 CLK_100M_LVDS#; PEG_CLK F43 CLK_PCIE_NB ↱4↳, PEG_CLK# E43 CLK_PCIE_NB# ↱4↳

DMI: DMI_RXN_0 AE41 DMI_TXN0 ↱16↳, DMI_RXN_1 AE37 DMI_TXN1 ↱16↳, DMI_RXN_2 AE47 DMI_TXN2 ↱16↳, DMI_RXN_3 AH39 DMI_TXN3 ↱16↳; DMI_RXP_0 AE40 DMI_TXP0 ↱16↳, DMI_RXP_1 AE38 DMI_TXP1 ↱16↳, DMI_RXP_2 AE48 DMI_TXP2 ↱16↳, DMI_RXP_3 AH40 DMI_TXP3 ↱16↳; DMI_TXN_0 AE35 DMI_RXN0 ↱16↳, DMI_TXN_1 AE43 DMI_RXN1 ↱16↳, DMI_TXN_2 AE46 DMI_RXN2 ↱16↳, DMI_TXN_3 AH42 DMI_RXN3 ↱16↳; DMI_TXP_0 AD35 DMI_RXP0 ↱16↳, DMI_TXP_1 AE44 DMI_RXP1 ↱16↳, DMI_TXP_2 AE46 DMI_RXP2 ↱16↳, DMI_TXP_3 AH43 DMI_RXP3 ↱16↳

GRAPHICS VID: GFX_VID_0 B33, GFX_VID_1 B32, GFX_VID_2 G33, GFX_VID_3 F33, GFX_VID_4 E33; GFX_VR_EN C34 NR66 1 2 100KOHM /GM GND

ME: CL_CLK AH37 CL_CLK0 ↱17↳, CL_DATA AH36 CL_DATA0 ↱17↳, CL_PWROK AN36 CLPWROK ↱17↳, CL_RST# AJ35 CL_RST#0 ↱17↳, CL_VREF AH34 NB_CL_VREF

MISC: DDPC_CTRLCLK N28 NT1, DDPC_CTRLDATA M28 NT2, SDVO_CTRLCLK G36 NT3, SDVO_CTRLDATA E36 NT4; CLKREQ# K36 MCH_CLKREQ# ↱4↳, ICH_SYNC# H36 MCH_ICH_SYNC# ↱17↳; TSATN# B12 TSATN# NR37 1 2 56OHM +VCCP

HDA: HDA_BCLK B28, HDA_RST# B30, HDA_SDI B29, HDA_SDO C29, HDA_SYNC A28

CFG: CFG_0 T25 ↱4,5↳ CPU_BSEL0, CFG_1 R25 ↱4,5↳ CPU_BSEL1, CFG_2 P25 ↱4,5↳ CPU_BSEL2, CFG_3 TP42 P20, CFG_4 TP43 P24, CFG_5 NR18 MCH_CFG_5 C25, CFG_6 NR19 MCH_CFG_6 N24, CFG_7 NR20 MCH_CFG_7 M24, CFG_8 TP44 F21, CFG_9 NR21 MCH_CFG_9 C23, CFG_10 NR22 MCH_CFG_10 C24, CFG_11 TP45 N21, CFG_12 NR23 MCH_CFG_12 P21, CFG_13 NR24 MCH_CFG_13 T21, CFG_14 TP46 R20, CFG_15 NR25 MCH_CFG_16 L21, CFG_16 TP47 M20, CFG_17 TP48 H21, CFG_18 TP49 P29, CFG_19 NR26 MCH_CFG_19 R28, CFG_20 NR27 MCH_CFG_20 T28 (Do Not Stuff 1% /X; GND, +3VS)

PM: PM_SYNC# R29 ↱17↳ PM_SYNC# ↱5,14,48↳ H_DPRSTP#, PM_DPRSTP# B7, PM_EXT_TS#_0 PM_EXTTS#0 N33, PM_EXT_TS#_1 PM_EXTTS#1 P32, PWROK AT40 ↱17,37↳ PM_PWROK, RSTIN# AT11 ↱15,19,29,31,36,37,42↳ BUF_PLT_RST#, THERMTRIP# T20 ↱5,6,14↳ H_THRMTRIP#, DPRSLPVR R32 ↱17,48↳ PM_DPRSLPVR

NC: NC_1 BG48, NC_2 BF48, NC_3 BD48, NC_4 BC48, NC_5 BH47, NC_6 BG47, NC_7 BE47, NC_8 BH46, NC_9 BF46, NC_10 BG45, NC_11 BH44, NC_12 BH43, NC_13 BH6, NC_14 BH5, NC_15 BG4, NC_16 BH3, NC_17 BF3, NC_18 BH2, NC_19 BG2, NC_20 BE2, NC_21 BG1, NC_22 BF1, NC_23 BD1, NC_24 BC1, NC_25 F1

CANTIGA_CHIPSET

+3VS → 10KOhm ×4: 1 2 NRN6A PM_EXTTS#0 PM_EXTTS#1; 3 4 NRN6B; 5 6 NRN6C; 7 8 NRN6D

M_RCOMP NR12 1 2 80.6Ohm 1%, NR13 1 2 Do Not Stuff 1% /X; M_RCOMP# NR14 1 2 Do Not Stuff 1% /X, NR15 1 2 80.6Ohm 1% → +1.8V, GND

M_VREF_MCH → NC7 0.1UF/10V GND; +1.8V → NR81 1KOhm 1%, NR82 1KOhm 1% GND

3.01K OHM -> 3K OHM

+1.8V → NR7 1KOhm 1%, NR8 3KOhm 1%, NR9 1KOhm 1%; SM_RCOMP_VOH → NC3 1UF/10V, NC4 0.01UF/25V; SM_RCOMP_VOL → NC5 1UF/10V, NC6 0.01UF/25V; R1.1 GND

2.2UF -> 1UF

CLK_96M_NB# CLK_96M_NB CLK_100M_LVDS# CLK_100M_LVDS → 0OHM ×4: NRN1A /PM, NRN1B /PM, NRN2A /PM, NRN2B /PM → GND

+1.05VM → NR34 1KOhm; NB_CL_VREF → NC8 0.1UF/10V GND, NR36 499Ohm 1% GND

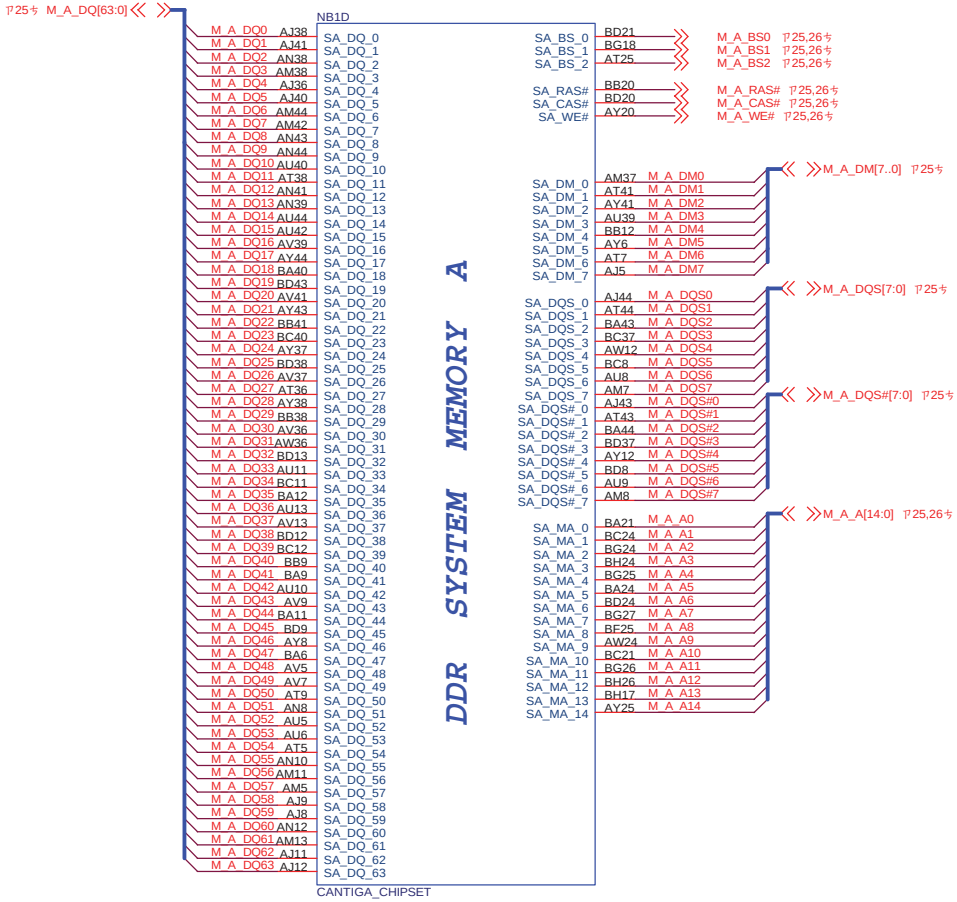
P80VC1

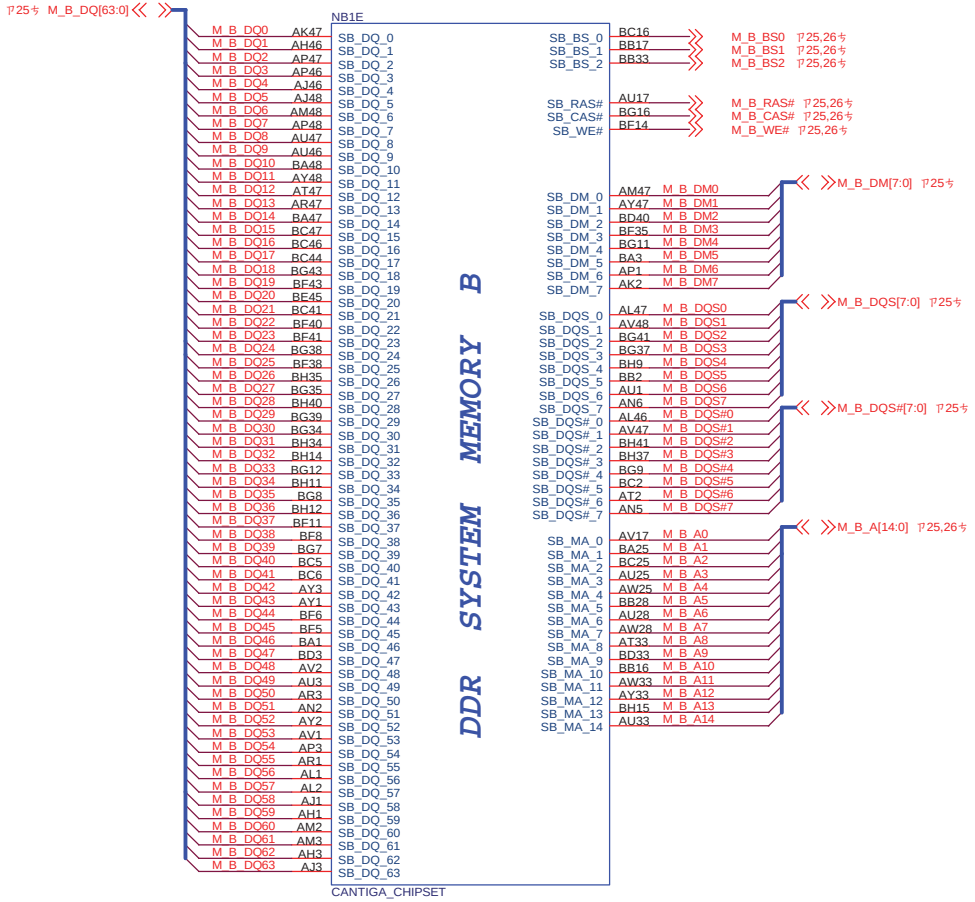
ASUSTeK COMPUTER INC. NB1 — Engineer: SZ_NB2

Title : Cantiga - DDR2/DMI(2)

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

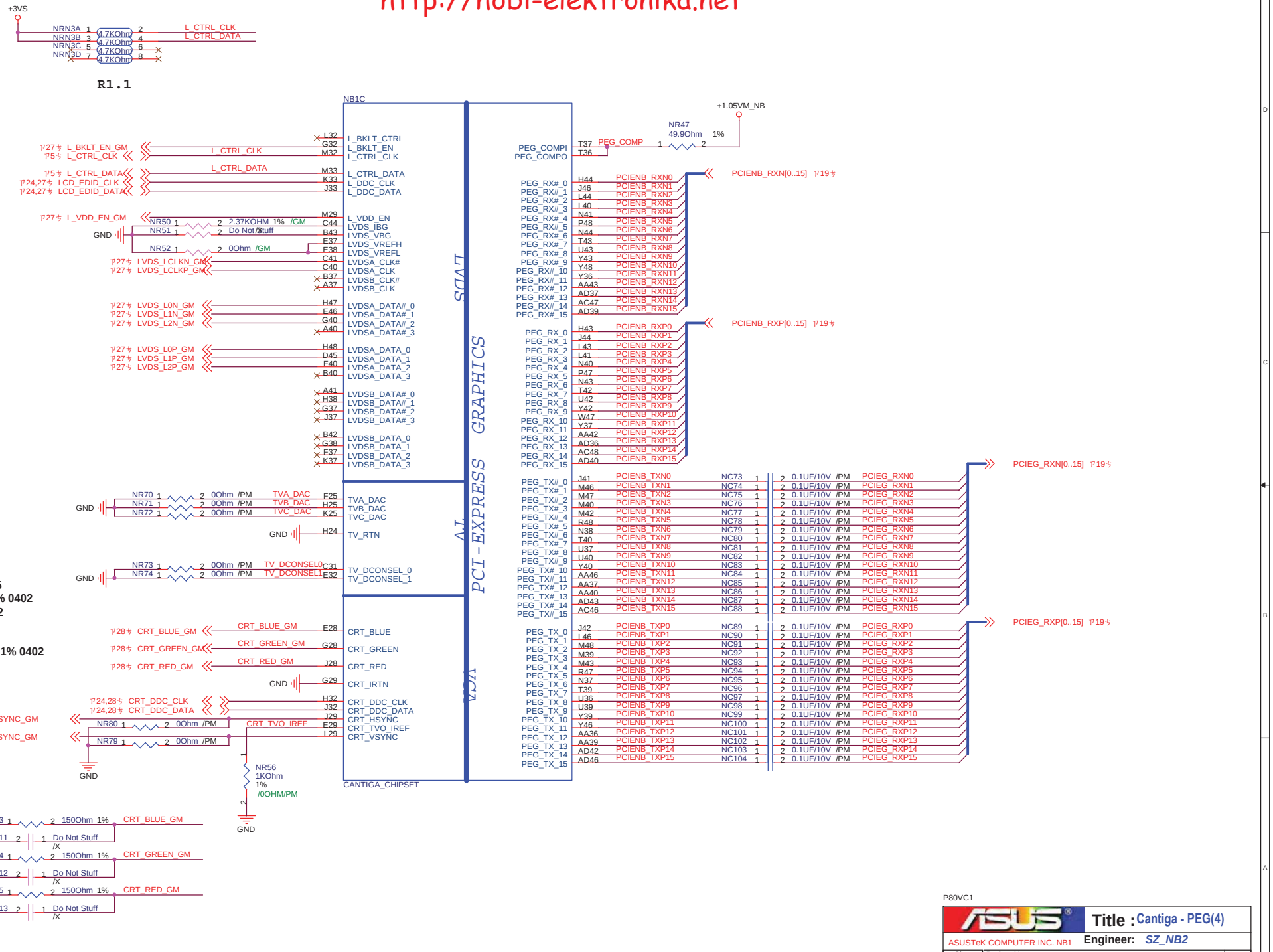
Date: Tuesday, December 16, 2008 Sheet 8 of 52





P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Cantiga - DDR2(3)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 9 of 52	

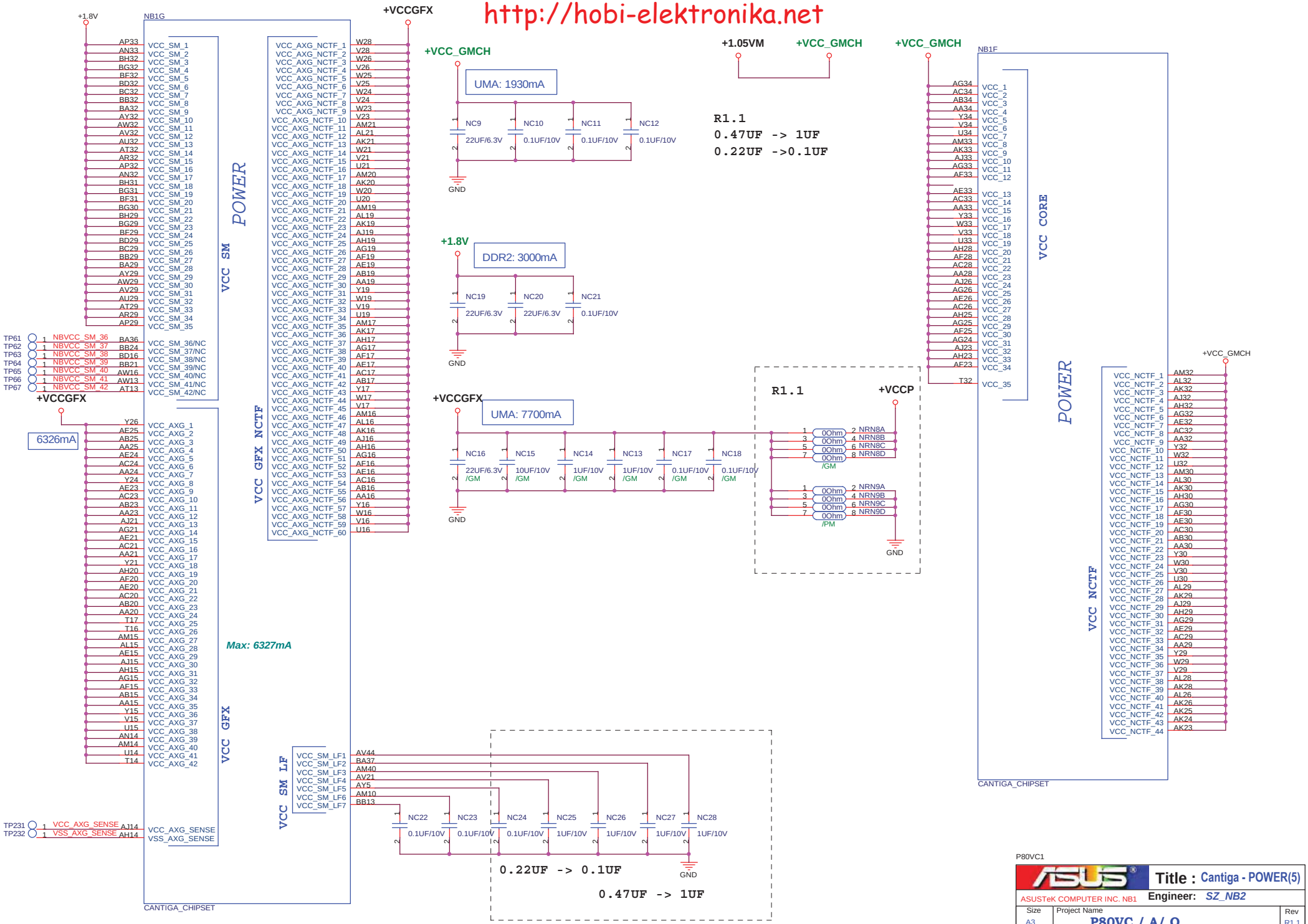


NR53, NR54, NR55
GM45: 150 ohm 1% 0402
PM45 : 0 ohm 0402

NR56
GM45: 1.02K ohm 1% 0402
PM45: 0 ohm 0402

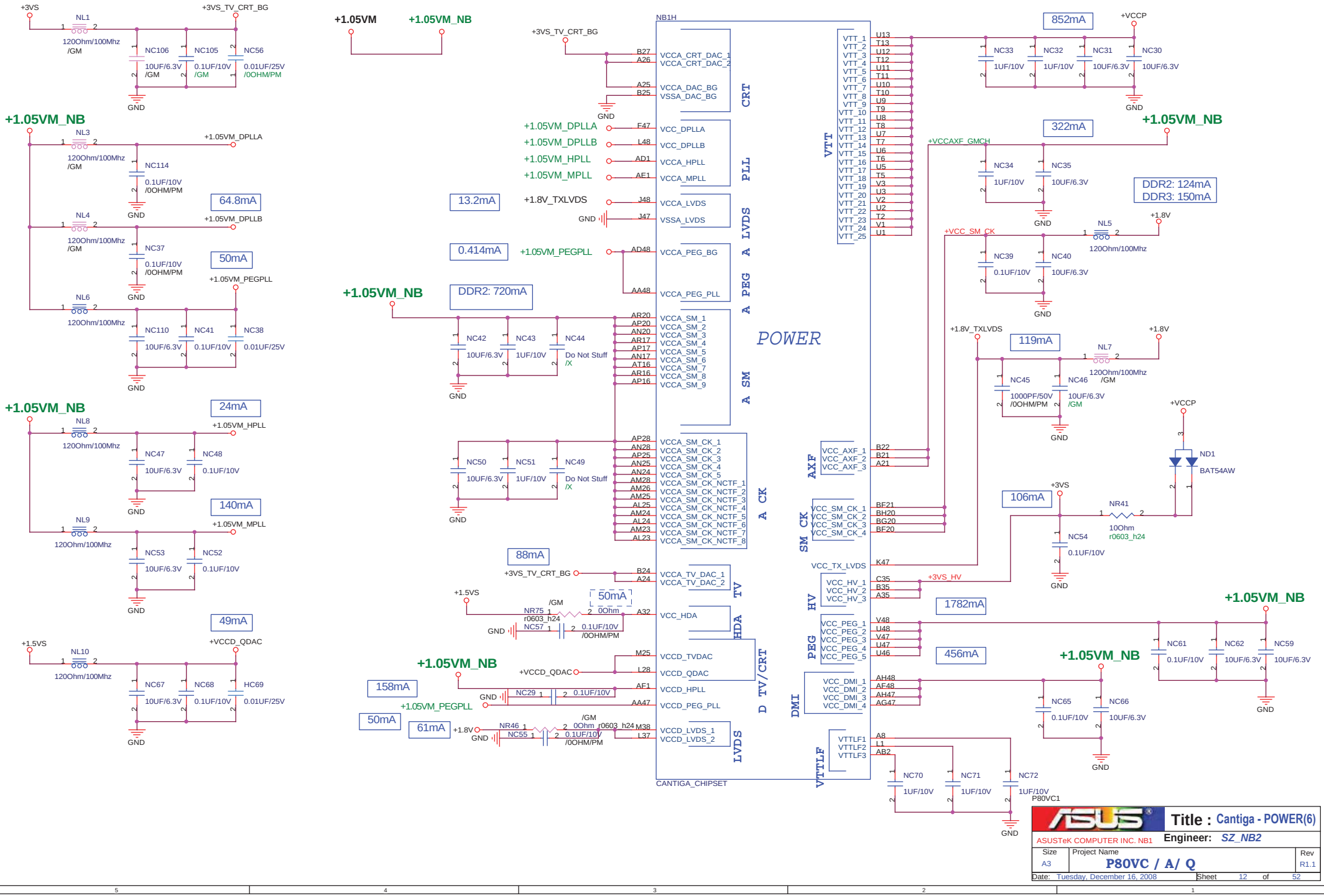
P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Cantiga - PEG(4)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 10 of 52	



P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Cantiga - POWER(5)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 11 of 52	



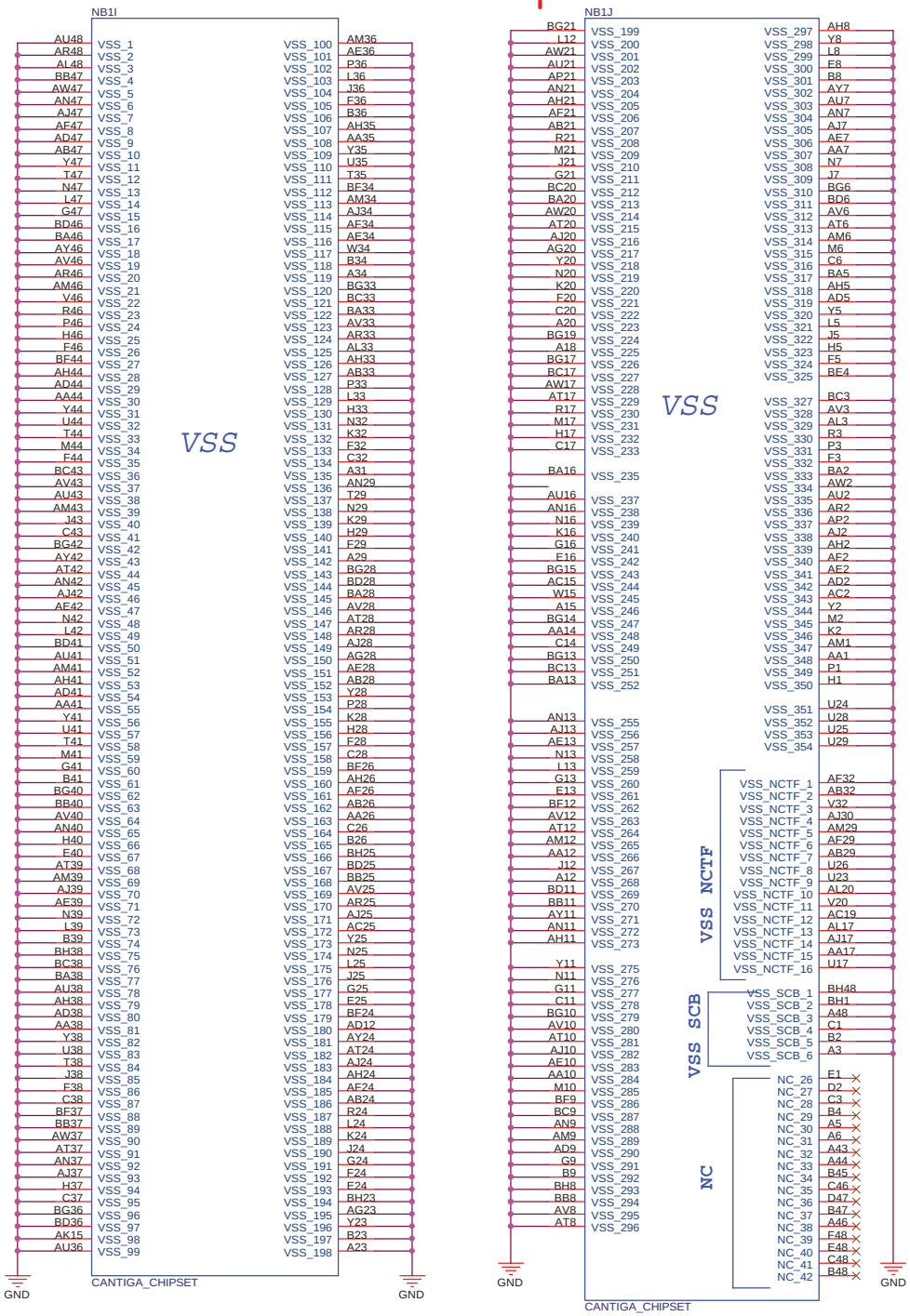
ASUSTeK COMPUTER INC. NB1

Title : Cantiga - POWER(6)

Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 12 of 52



Change NC-26/42 to NC from GND

P80VC1

ASUSTeK COMPUTER INC. NB1	Title : Cantiga - GND(7)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 13 of 52	

Place Near the Open Door

RTCRST#
SC1 1UF/10V
JRST1 Do Not Stuff r0603_h24 /X
GND GND

R1.1
+VCC_RTC
100KOHM SRN6A
100KOHM SRN6B
100KOHM SRN6C
100KOHM SRN6D

VccSus1_05, VccSus1_5, & VccCL1_5 Internal VR

VccLAN1_05 & VccCL1_05 Internal VR

High = Enable (Default)

Low = Disable

BOM: 02G010015342

SB Heatsink Screwhole
SH1 SH2
13GNJ510M190-1 13GNJ510M190-1
GND GND

SB1A
RTC_X1 C23 RTCX1
RTC_X2 C24 RTCX2
RTCRST# A25 RTCRST#
INTRUDER# E20 SRTCRST#
C22 INTRUDER#
ICH_INTVRMEN B22 INTVRMEN
ICH_LAN100_SLP A22 LAN100_SLP
E25 GLAN_CLK
C13 LAN_RSTSYNC
F14 LAN_RXD0
G13 LAN_RXD1
D14 LAN_RXD2
D13 LAN_TXD0
D12 LAN_TXD1
E13 LAN_TXD2
GPIO56 B10 GLAN_DOCK#/GPIO56
B28 GLAN_COMPI
B27 GLAN_COMPO
ACZ_BCLK AF6 HDA_BIT_CLK
ACZ_SYNC AH4 HDA_SYNC
ACZ_RST# AE7 HDA_RST#
AF4 HDA_SDIN0
AG4 HDA_SDIN1
AH3 HDA_SDIN2
AE5 HDA_SDIN3
ACZ_SDOUT AG5 HDA_SDOUT
SB_GPIO33 AG7 HDA_DOCK_EN#/GPIO33
AE8 HDA_DOCK_RST#/GPIO34
AG8 SATALED#
AJ16 SATA0RXN
AH16 SATA0RXP
AF17 SATA0TXN
AG17 SATA0TXP
AH13 SATA1RXN
AJ13 SATA1RXP
AG14 SATA1TXN
AF14 SATA1TXP
ICH9M

RTC
LPC
LAN / GLAN
CPU
IHDA
SATA

FWH0/LAD0 K5 LPC_AD0
FWH1/LAD1 K4 LPC_AD1
FWH2/LAD2 L6 LPC_AD2
FWH3/LAD3 K2 LPC_AD3
FWH4/LFRAME# K3 LPC_FRAME#
LDRQ0# J3 LPC_DRQ0# 1 ST68
LDRQ1#/GPIO23 J1 LPC_DRQ1#
A20GATE N7 A20GATE
A20M# AJ27 H_A20M#
DPRSTP# AJ25 H_DPRSTP#
DPSLP# AE23 H_DPSLP#
FERR# AJ26 1 56OHM 2 SRN4A H_FERR#
CPUPWRGD AD22 H_PWRGD
IGNNE# AE25 H_IGNNE#
INIT# AE22 H_INIT#
INTR AG25 H_INTR
RCIN# L3 RC_IN# H_RC_IN#
NMI AF23 H_NMI
SMI# AF24 H_SMI#
STPCLK# AH27 H_STPCLK#
THRMTRIP# AG26 PM_THRMTRIP#
PECI AG27 1 ST80
SATA4RXN AH11
SATA4RXP AJ11
SATA4TXN AG12
SATA4TXP AE12
SATA5RXN AH9 ESATA_RXN_SB
SATA5RXP AJ9 ESATA_RXP_SB
SATA5TXN AE10 ESATA_TXN_SB
SATA5TXP AE10 ESATA_TXP_SB
SATA_CLKN AH18 CLK_SATA_SB#
SATA_CLKP AJ18 CLK_SATA_SB
SATARBIAS# AJ7
SATARBIAS AH7 SATARBIAS# SR38 1 2 27.4Ohm 1% GND

Pass EA measurement

+3VSUS SR35 10KOhm
+1.5VS_PCIE_ICH SR36 1 2 24.9Ohm 1%

ACZ_BCLK_AUD 42 ACZ_SYNC_AUD 42 ACZ_RST#_AUD 42 ACZ_SDOUT_AUD 42 ACZ_BCLK_MDC 32 ACZ_SYNC_MDC 32 ACZ_RST#_MDC 32 ACZ_SDOUT_MDC 32
33OHM SRN1A SRN1D SRN1B SRN1C SRN2D SRN2B SRN2C SRN2A
ACZ_BCLK ACZ_SYNC ACZ_RST# ACZ_SDOUT

ACZ_SDIN0_AUD 42 ACZ_SDIN1_MDC 32

ST82

HDD_LED# 40
HDD
SATA_RXN0 35 SATA_RXP0 35 SATA_TXN0 35 SATA_TXP0 35
ODD
SATA_RXN1 35 SATA_RXP1 35 SATA_TXN1 35 SATA_TXP1 35

SC5 12PF/50V RTC_X1
SX1 32.768kMhz +/-20ppm/12.5PF
SR40 10MOhm
SC6 12PF/50V RTC_X2
GND

OD signal
H_FERR# 3 56OHM 4 SRN4B +VCCP
+VCCP SRN4D 56OHM
PM_THRMTRIP# 5 56OHM 6 SRN4C H_THRMTRIP# 5,6,8
SC72 Do Not Stuff /X
GND

[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1

Flash Descriptor Security Override

High = Enable (Default)

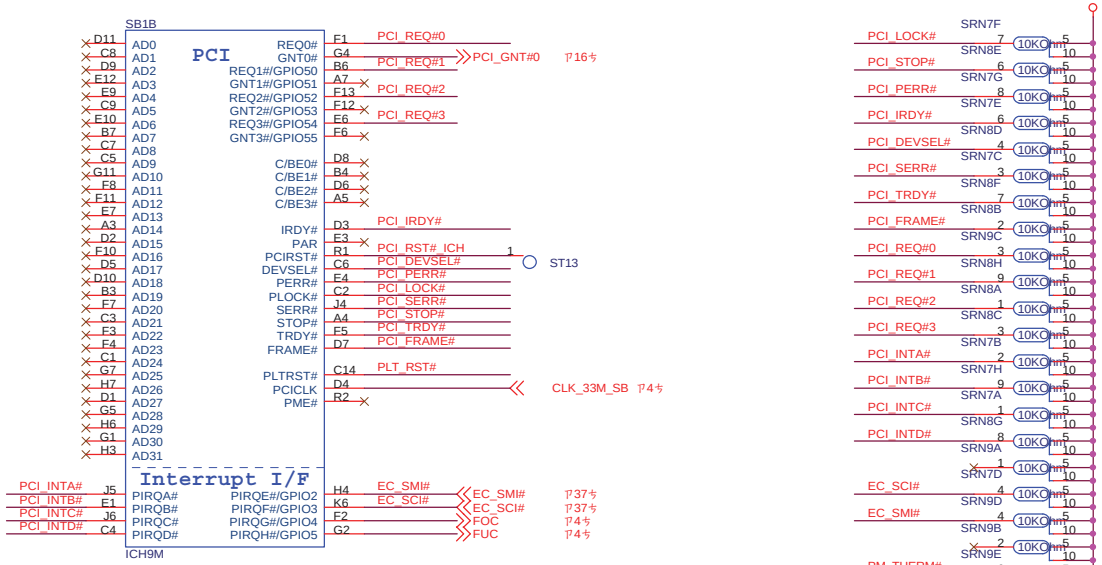
Low = Overridden

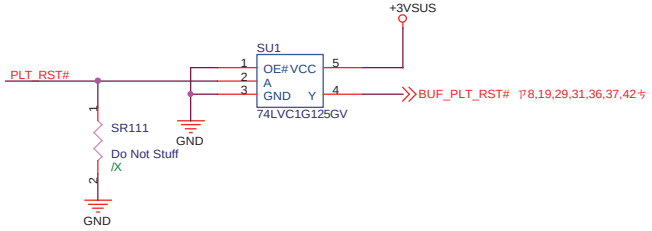
ACZ_SDOUT SR49 1 2 Do Not Stuff 1%
SR5 1 2 Do Not Stuff 1%
+3VS
ICH_TP3 17
GND

SR6 1 2 Do Not Stuff SB_GPIO33
GND

P80VC1

ASUSTeK COMPUTER INC. NB1	Title : SB-ICH9M(1)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 14 of 52	





UNUSED PCI temination

AD [31:0]	Can be left unconnected
C/BE [3:0]#	Can be left unconnected
DEVSEL#	8.2-k weak pull-up resistor to Vcc3_3
FRAME#	8.2-k weak pull-up resistor to Vcc3_3
IRDY#	8.2-k weak pull-up resistor to Vcc3_3
TRDY#	8.2-k weak pull-up resistor to Vcc3_3
STOP#	8.2-k weak pull-up resistor to Vcc3_3
PAR	Can be left unconnected
PERR#	8.2-k weak pull-up resistor to Vcc3_3
REQ0# REQ1#/GPIO50 REQ2#/GPIO52 REQ3#/GPIO54	Requires a 8.2-k weak pull-up resistor to Vcc3_3. REQ [3:1] can be configured as GPIO instead.
GNT0# GNT1#/GPIO51 GNT2#/GPIO53 GNT3#/GPIO55	Can be left unconnected. GNT [3:1]# can be configured as GPIO instead. GNT [3:0] is sampled as a functional strapping;
PCICLK	Should remain connected to 33-MHz clock source
PCIRST#	Can be left unconnected
PLOCK#	8.2-k weak pull-up resistor to Vcc3_3
SERR#	8.2-k weak pull-up resistor to Vcc3_3
PIRQ [D:A]# PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5	Requires a 8.2-k weak pull-up resistor to Vcc3_3 PIRQ [H:E]# Can be configured as GPIO instead
SERIRQ	8.2-k pull-up to Vcc3_3
PME#	Can be left unconnected. Internally pull-up
CLKRUN#	8.2-k weak pull-up resistor to Vcc3_3

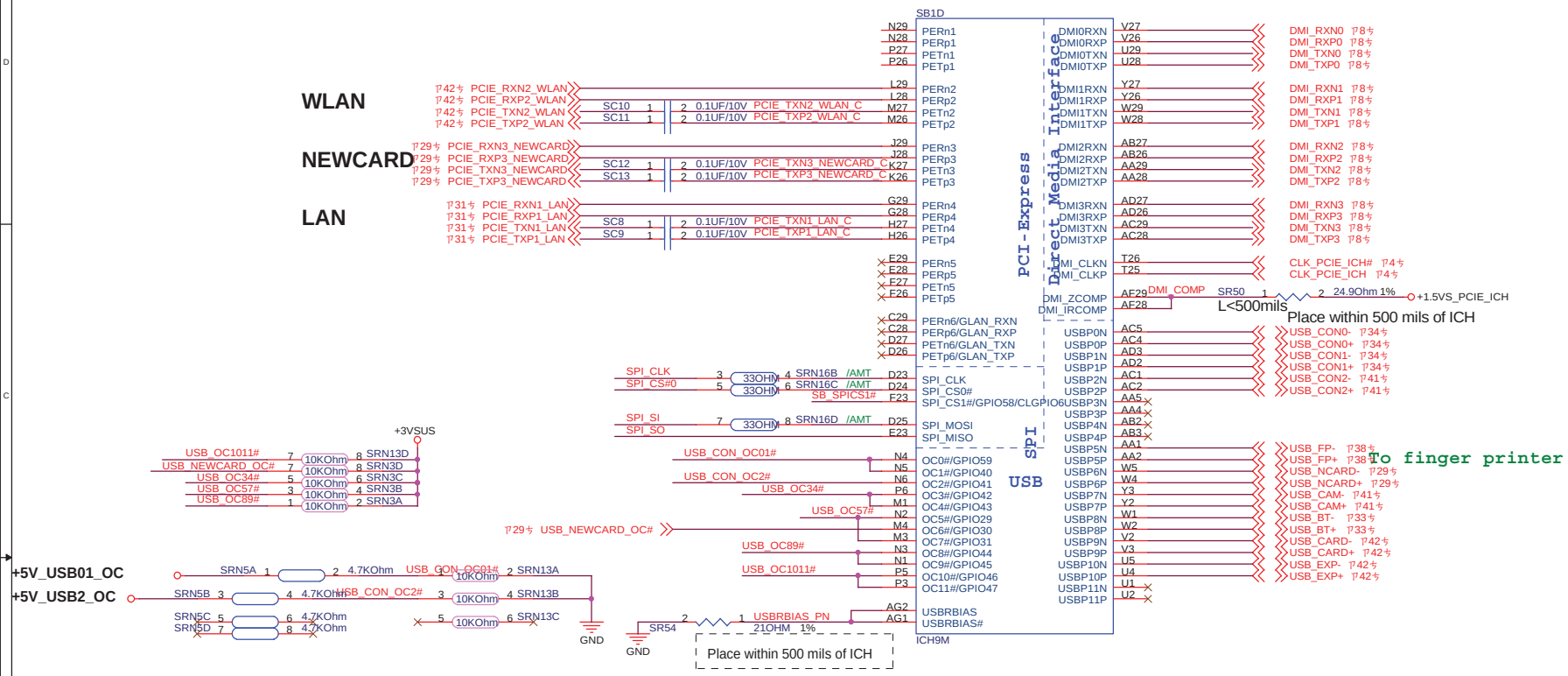
P80VC1

Title : SB-ICH9M(2)

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

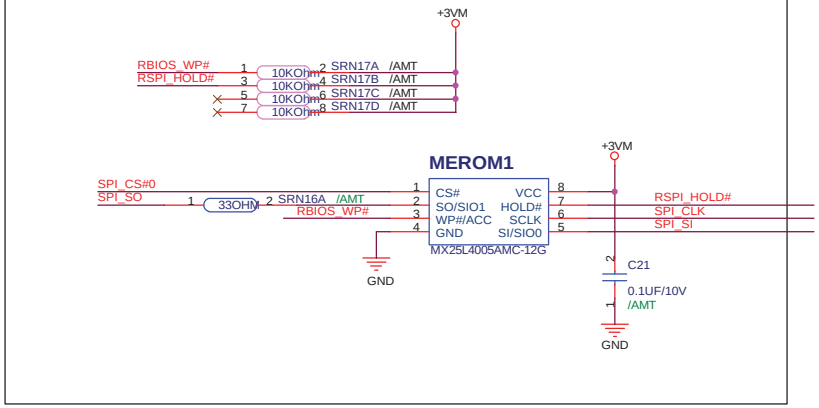
Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 15 of 52



USB0	CON
USB1	CON
USB2	CON
USB3	N/A
USB4	N/A
USB5	FingerPrint
USB6	NewCard
USB7	Camera
USB8	BT
USB9	Cardreader
USB10	MC (WLAN)
USB11	N/A

SB Flash for ME



ICH9 Boot BIOS select

		GNT#0	CS#1	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

PCI_GNT#0 SR216 Do Not Stuff /X
SB_SPICS1# SR217 Do Not Stuff /X

R1.1

SPI_MOSI
iTPM
Enable
High = Enable
Low = Disable(Default)

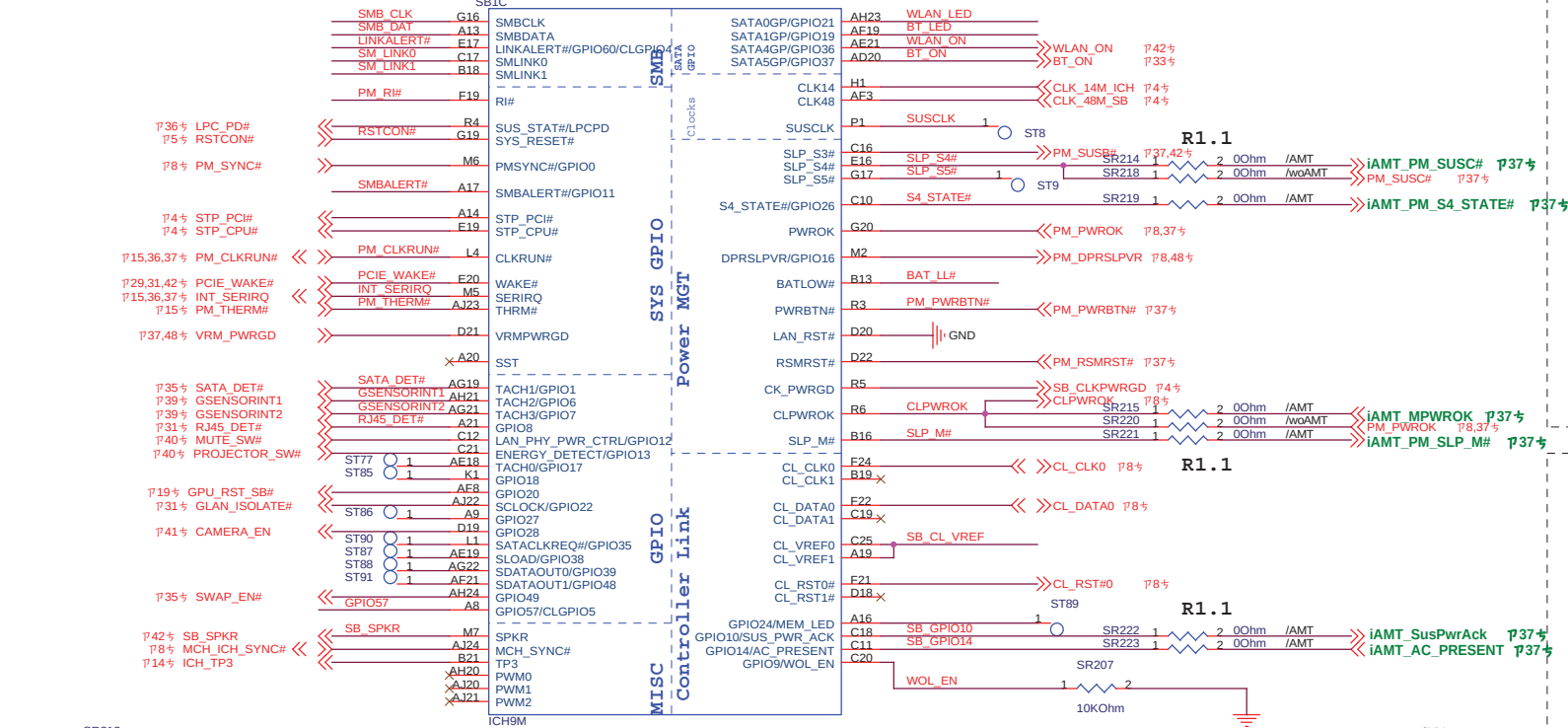
P80VC1

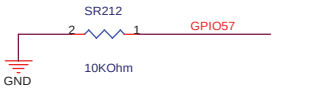
Title : SB-ICH9M(3)

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

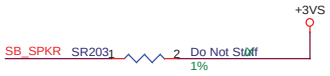
Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

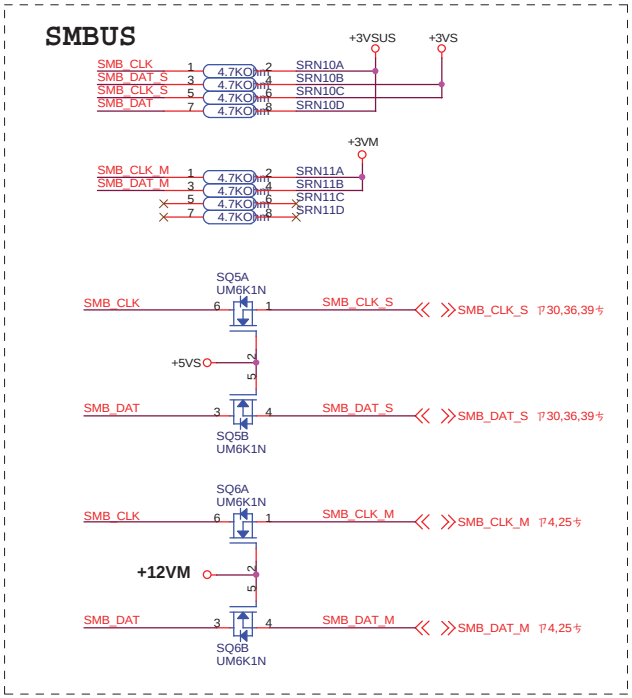
Date: Tuesday, December 16, 2008 Sheet 16 of 52

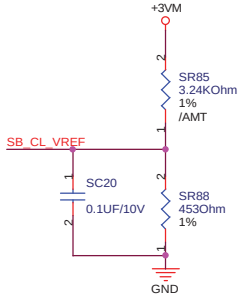


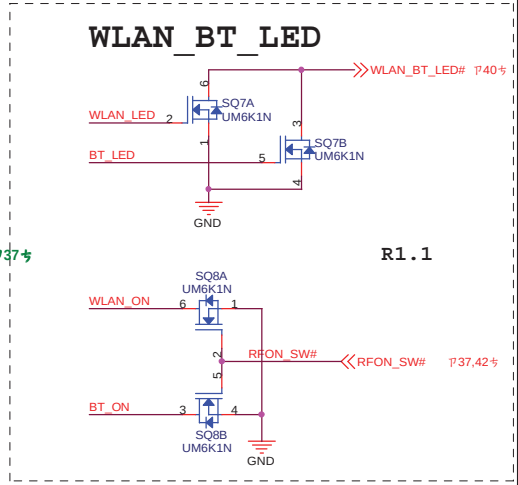


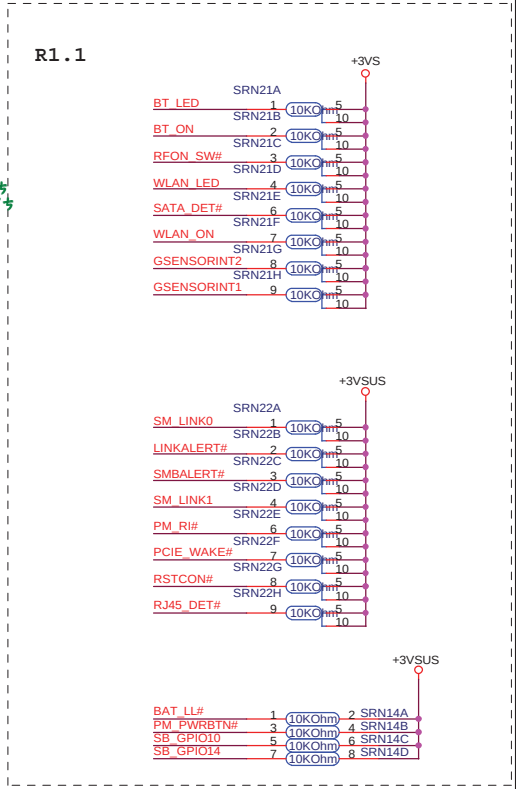
GPIO57:
PU:iTPM Physical presence
PD:100Kohm





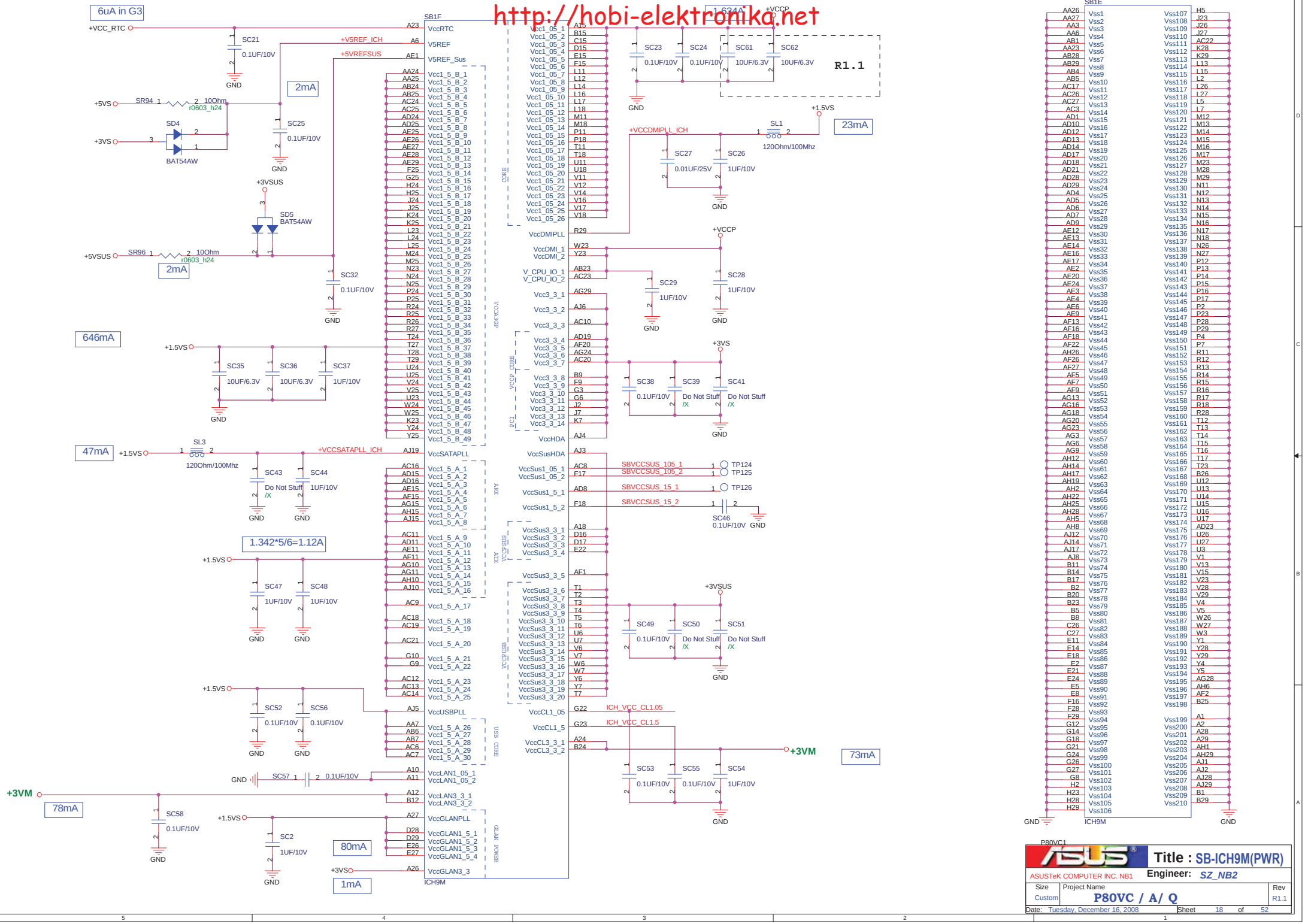






P80VC1

ASUSTeK COMPUTER INC. NB1	Title : SB-ICH9M(4)	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 17 of 52	



PCIEG_RXP[0..15] 於10分
PCIEG_RXN[0..15] 於10分
PCIENB_RXP[0..15] 於10分
PCIENB_RXN[0..15] 於10分

PCIENB_RXN15	GC4	1	2 0.1UF/10V /PM	PCIEG_TXN15
PCIENB_RXP15	GC5	1	2 0.1UF/10V /PM	PCIEG_TXP15
PCIENB_RXN14	GC6	1	2 0.1UF/10V /PM	PCIEG_TXN14
PCIENB_RXP14	GC7	1	2 0.1UF/10V /PM	PCIEG_TXP14
PCIENB_RXN13	GC8	1	2 0.1UF/10V /PM	PCIEG_TXN13
PCIENB_RXP13	GC9	1	2 0.1UF/10V /PM	PCIEG_TXP13
PCIENB_RXN12	GC10	1	2 0.1UF/10V /PM	PCIEG_TXN12
PCIENB_RXP12	GC11	1	2 0.1UF/10V /PM	PCIEG_TXP12
PCIENB_RXN11	GC12	1	2 0.1UF/10V /PM	PCIEG_TXN11
PCIENB_RXP11	GC17	1	2 0.1UF/10V /PM	PCIEG_TXP11
PCIENB_RXN10	GC18	1	2 0.1UF/10V /PM	PCIEG_TXN10
PCIENB_RXP10	GC19	1	2 0.1UF/10V /PM	PCIEG_TXP10
PCIENB_RXN9	GC20	1	2 0.1UF/10V /PM	PCIEG_TXN9
PCIENB_RXP9	GC21	1	2 0.1UF/10V /PM	PCIEG_TXP9
PCIENB_RXN8	GC22	1	2 0.1UF/10V /PM	PCIEG_TXN8
PCIENB_RXP8	GC23	1	2 0.1UF/10V /PM	PCIEG_TXP8
PCIENB_RXN7	GC24	1	2 0.1UF/10V /PM	PCIEG_TXN7
PCIENB_RXP7	GC25	1	2 0.1UF/10V /PM	PCIEG_TXP7
PCIENB_RXN6	GC26	1	2 0.1UF/10V /PM	PCIEG_TXN6
PCIENB_RXP6	GC27	1	2 0.1UF/10V /PM	PCIEG_TXP6
PCIENB_RXN5	GC28	1	2 0.1UF/10V /PM	PCIEG_TXN5
PCIENB_RXP5	GC29	1	2 0.1UF/10V /PM	PCIEG_TXP5
PCIENB_RXN4	GC30	1	2 0.1UF/10V /PM	PCIEG_TXN4
PCIENB_RXP4	GC31	1	2 0.1UF/10V /PM	PCIEG_TXP4
PCIENB_RXN3	GC32	1	2 0.1UF/10V /PM	PCIEG_TXN3
PCIENB_RXP3	GC33	1	2 0.1UF/10V /PM	PCIEG_TXP3
PCIENB_RXN2	GC34	1	2 0.1UF/10V /PM	PCIEG_TXN2
PCIENB_RXP2	GC35	1	2 0.1UF/10V /PM	PCIEG_TXP2
PCIENB_RXN1	GC42	1	2 0.1UF/10V /PM	PCIEG_TXN1
PCIENB_RXP1	GC43	1	2 0.1UF/10V /PM	PCIEG_TXP1
PCIENB_RXN0	GC44	1	2 0.1UF/10V /PM	PCIEG_TXN0
PCIENB_RXP0	GC45	1	2 0.1UF/10V /PM	PCIEG_TXP0

+3VSG
GR106 10KOhm /PM
GD1 BAT54AW /PM
於8,15,29,31,36,37,42分 BUF_PLT_RST#
於17分 GPU_RST_SB#
NB9M_RST#
於4分 CLK_PCIE_GPU
於4分 CLK_PCIE_GPU#
GT01 /X
GT02 /X

U9A
1/13 PCI_EXPRESS

	AF9	NC_10
PEX_RST_N	AD9	
PEX_REFCLK	AB10	CLK_PCIE_NB9M
PEX_REFCLK_N	AC10	CLK_PCIE_NB9M#
PEX_TX0	AD10	PCIEG_TXP0
PEX_TX0_N	AD11	PCIEG_TXN0
PEX_RX0	AE12	PCIEG_RXP0
PEX_RX0_N	AF12	PCIEG_RXN0
PEX_TX1	AD12	PCIEG_TXP1
PEX_TX1_N	AC12	PCIEG_TXN1
PEX_RX1	AG12	PCIEG_RXP1
PEX_RX1_N	AG13	PCIEG_RXN1
PEX_TX2	AB11	PCIEG_TXP2
PEX_TX2_N	AB12	PCIEG_TXN2
PEX_RX2	AF13	PCIEG_RXP2
PEX_RX2_N	AE13	PCIEG_RXN2
PEX_TX3	AD13	PCIEG_TXP3
PEX_TX3_N	AD14	PCIEG_TXN3
PEX_RX3	AE15	PCIEG_RXP3
PEX_RX3_N	AF15	PCIEG_RXN3
PEX_TX4	AD15	PCIEG_TXP4
PEX_TX4_N	AC15	PCIEG_TXN4
PEX_RX4	AG15	PCIEG_RXP4
PEX_RX4_N	AG16	PCIEG_RXN4
PEX_TX5	AB14	PCIEG_TXP5
PEX_TX5_N	AB15	PCIEG_TXN5
PEX_RX5	AF16	PCIEG_RXP5
PEX_RX5_N	AE16	PCIEG_RXN5
PEX_TX6	AC16	PCIEG_TXP6
PEX_TX6_N	AD16	PCIEG_TXN6
PEX_RX6	AE18	PCIEG_RXP6
PEX_RX6_N	AF18	PCIEG_RXN6
PEX_TX7	AD17	PCIEG_TXP7
PEX_TX7_N	AD18	PCIEG_TXN7
PEX_RX7	AG18	PCIEG_RXP7
PEX_RX7_N	AG19	PCIEG_RXN7
PEX_TX8	AC18	PCIEG_TXP8
PEX_TX8_N	AB18	PCIEG_TXN8
PEX_RX8	AF19	PCIEG_RXP8
PEX_RX8_N	AE19	PCIEG_RXN8
PEX_TX9	AB19	PCIEG_TXP9
PEX_TX9_N	AB20	PCIEG_TXN9
PEX_RX9	AE21	PCIEG_RXP9
PEX_RX9_N	AF21	PCIEG_RXN9
PEX_TX10	AD19	PCIEG_TXP10
PEX_TX10_N	AD20	PCIEG_TXN10
PEX_RX10	AG21	PCIEG_RXP10
PEX_RX10_N	AG22	PCIEG_RXN10
PEX_TX11	AD21	PCIEG_TXP11
PEX_TX11_N	AC21	PCIEG_TXN11
PEX_RX11	AF22	PCIEG_RXP11
PEX_RX11_N	AE22	PCIEG_RXN11
PEX_TX12	AB21	PCIEG_TXP12
PEX_TX12_N	AB22	PCIEG_TXN12
PEX_RX12	AE24	PCIEG_RXP12
PEX_RX12_N	AF24	PCIEG_RXN12
PEX_TX13	AC22	PCIEG_TXP13
PEX_TX13_N	AD22	PCIEG_TXN13
PEX_RX13	AG24	PCIEG_RXP13
PEX_RX13_N	AF25	PCIEG_RXN13
PEX_TX14	AD23	PCIEG_TXP14
PEX_TX14_N	AD24	PCIEG_TXN14
PEX_RX14	AG25	PCIEG_RXP14
PEX_RX14_N	AG26	PCIEG_RXN14
PEX_TX15	AE25	PCIEG_TXP15
PEX_TX15_N	AE26	PCIEG_TXN15
PEX_RX15	AF27	PCIEG_RXP15
PEX_RX15_N	AF27	PCIEG_RXN15

NB9M_GS /PM

+3VS +3VSG 200mA
+1.8VS +1.8VSG
+0.9VS +0.9VS_VGA
+1.1VS_GPU +VCCP 1.715A
JP4 1 2 Do Not Stuff /X
Use +1.05VS(+VCCP) for +1.1VS rail

BOM:02G190014113

+1.1VS_GPU 1.6A

PEX_IOVDD_01	AC9	
PEX_IOVDD_02	AD7	
PEX_IOVDD_03	AD8	
PEX_IOVDD_04	AE7	
PEX_IOVDD_05	AF7	
PEX_IOVDD_06	AG7	
PEX_IOVDDQ_01	AB13	
PEX_IOVDDQ_02	AB16	
PEX_IOVDDQ_03	AB17	
PEX_IOVDDQ_04	AB7	
PEX_IOVDDQ_05	AB8	
PEX_IOVDDQ_06	AB9	
PEX_IOVDDQ_07	AC13	
PEX_IOVDDQ_08	AC7	
PEX_IOVDDQ_09	AD6	
PEX_IOVDDQ_10	AE6	
PEX_IOVDDQ_11	AF6	
PEX_IOVDDQ_12	AG6	

GC13 10UF/10V X7R 10% /PM
GC14 1UF/10V /PM
GC15 1UF/10V /PM
GC16 1UF/10V /PM
GND

+VGA_CORE_VS

VDD_01	J10
VDD_02	J12
VDD_03	J13
VDD_04	J9
VDD_05	L9
VDD_06	M11
VDD_07	M17
VDD_08	M9
VDD_09	N11
VDD_10	N12
VDD_11	N13
VDD_12	N14
VDD_13	N15
VDD_14	N16
VDD_15	N17
VDD_16	N19
VDD_17	N9
VDD_18	P11
VDD_19	P12
VDD_20	P13
VDD_21	P14
VDD_22	P15
VDD_23	P16
VDD_24	P17
VDD_25	R11
VDD_26	R12
VDD_27	R13
VDD_28	R14
VDD_29	R15
VDD_30	R16
VDD_31	R17
VDD_32	R9
VDD_33	T11
VDD_34	T17
VDD_35	T9
VDD_36	U19
VDD_37	U9
VDD_38	W10
VDD_39	W12
VDD_40	W13
VDD_41	W18
VDD_42	W19
VDD_43	W9

GC46 10UF/6.3V /PM
GC47 1UF/10V /PM
GC48 1UF/10V /PM
GC49 1UF/10V /PM
GC50 1UF/10V /PM
GC51 1UF/10V /PM
GC41 1UF/10V /PM
GND

VDD_SENSE	W15	NVDD_SENSE 於53分
GND_SENSE	W16	

GND

+3VSG 80mA

VDD33_01	A12
VDD33_02	B12
VDD33_03	C12
VDD33_04	D12
VDD33_05	E12
VDD33_06	F12

GC53 1UF/10V /PM
GND

+1.1VS_GPU 65mA
PEX_PLLVDD AF9
GL1 10NH I0603 /PM
GC54 Do Not Stuff /X
GC56 1UF/10V /PM
GND

PEX_TSTCLK_OUT	AF10	PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N	AE10	PEX_TSTCLK_OUT_N

GR1 200Ohm 1% /PM

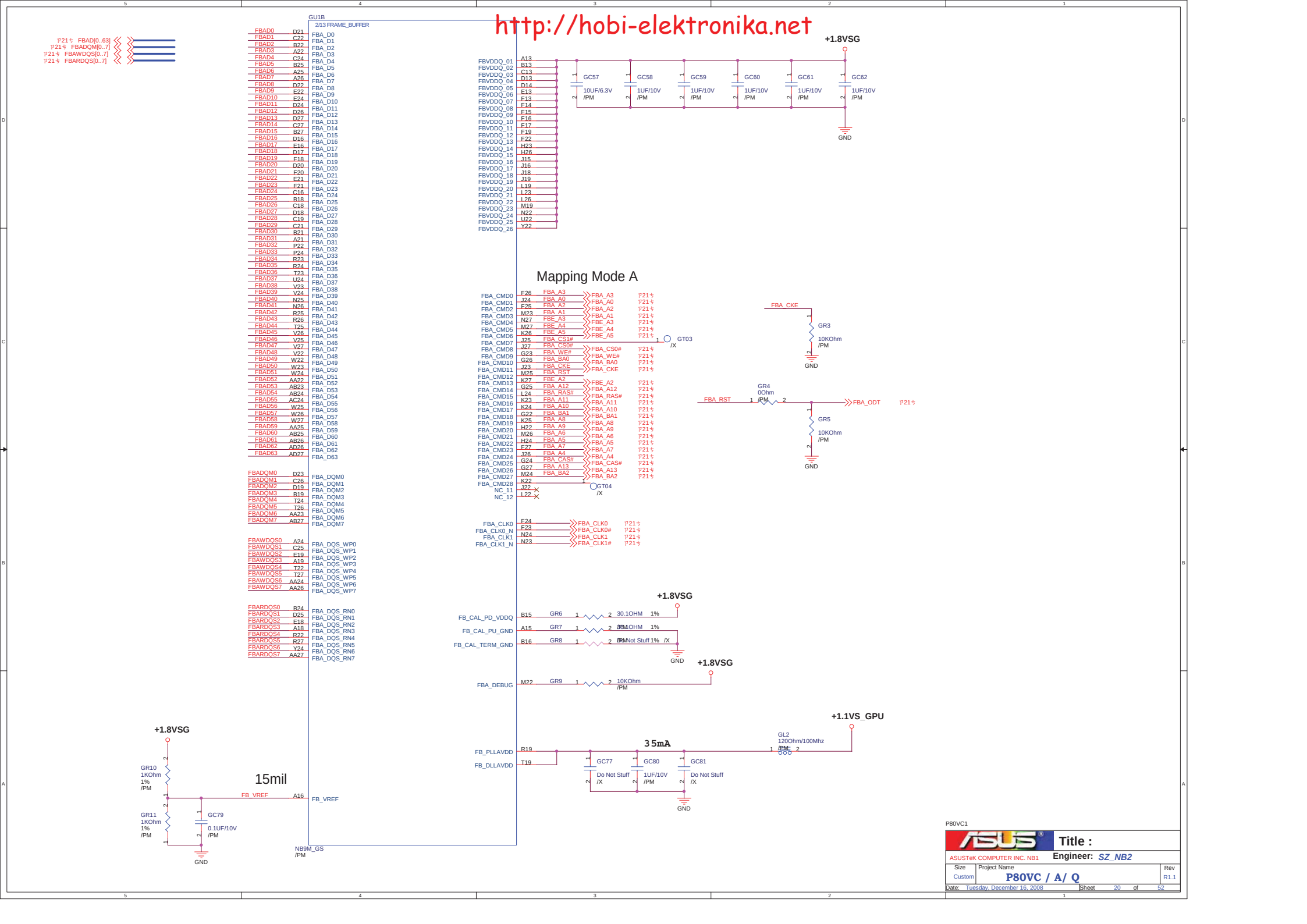
NC_09	AG9	
PEX_TERMP	AG10	

GR2 2.49KOhm 1% /PM
GND

PCI-E I/O Termination Calibration

P80VC1

ASUSTeK COMPUTER INC. NB1
Title :
Engineer: SZ_NB2
Size: Custom
Project Name: P80VC / A/ Q
Rev: R1.1
Date: Tuesday, December 16, 2008
Sheet 19 of 52



P80VC1

ASUSTeK COMPUTER INC. NB1

Title :

Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 20 of 52

FBAWDQS[0..7]
FBARDQS[0..7]
FBADQM[0..7]

03G15133F114:
03G15133F211

GU2 — K4N1G164QQ_HC25 /PM

GU3 — K4N1G164QQ_HC25 /PM

GU4 — K4N1G164QQ_HC25 /PM

GU5 — K4N1G164QQ_HC25 /PM

+1.8VSG

GND

FBA_ODT

FBA_CLK1 GR14 1 2 475Ohm 1% FBA_CLK1# /PM

FBA_CLK0 GR15 1 2 475Ohm 1% FBA_CLK0# /PM

+1.8VSG

GR12 1KOhm 1% /PM FBAVREF0

GR13 1KOhm 1% /PM FBAVREF1

15mil

GR16 1KOhm 1% /PM

GR17 1KOhm 1% /PM

GC83 0.1UF/10V /PM

GC84 0.1UF/10V /PM

GC85 GC86 GC87 1UF/10V /PM Do Not Stuff /X

GC88 GC89 GC90 1UF/10V /PM Do Not Stuff /X

GC91 GC92 GC93 1UF/10V /PM Do Not Stuff /X

GC94 GC95 GC96 1UF/10V /PM Do Not Stuff /X

+0.9VS_VGA

GC109 0.1UF/10V /PM

GC110 0.1UF/10V /PM

GC111 10UF/6.3V /PM

P80VC1

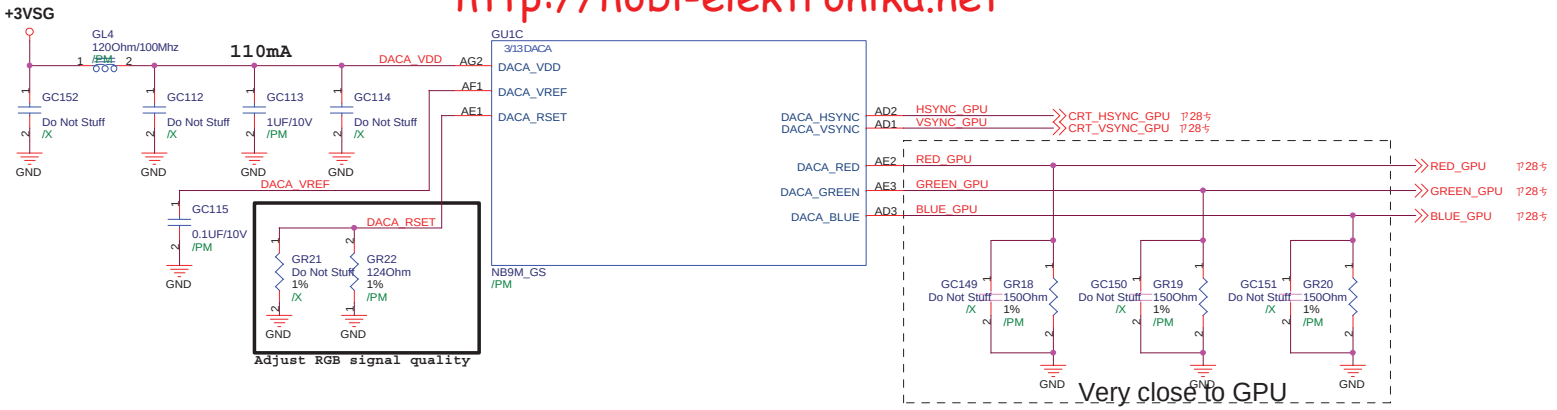
Title :

ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

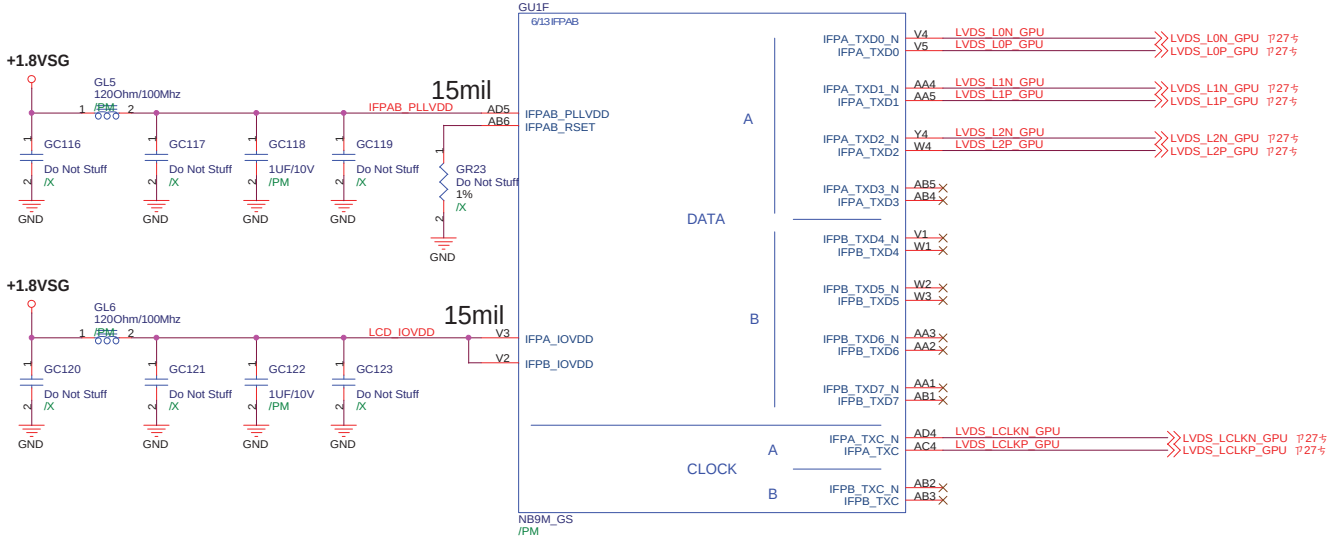
Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 21 of 52

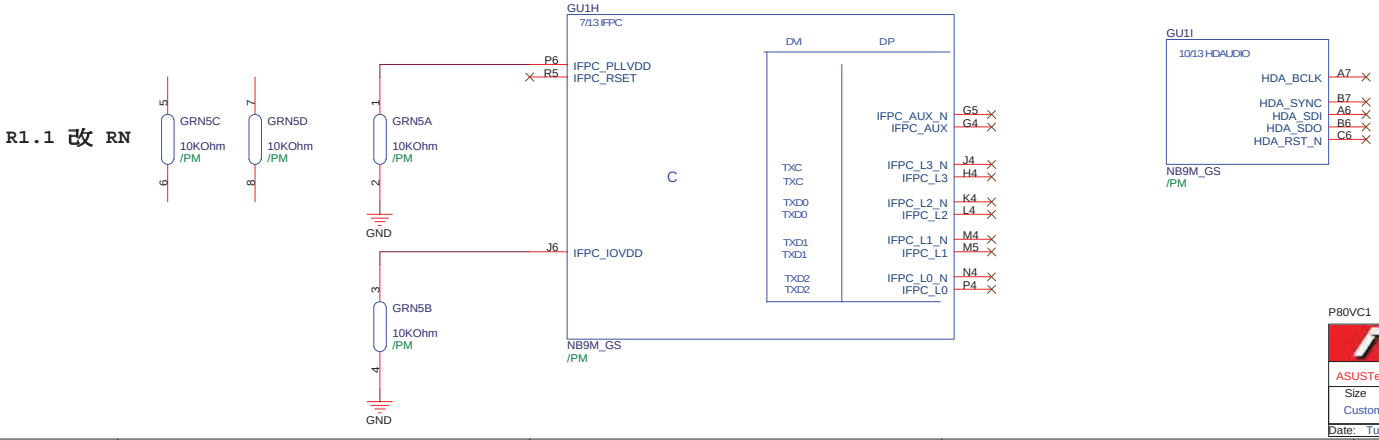
VGA



LVDS



HDMI



P80VC1

ASUSTeK COMPUTER INC. NB1

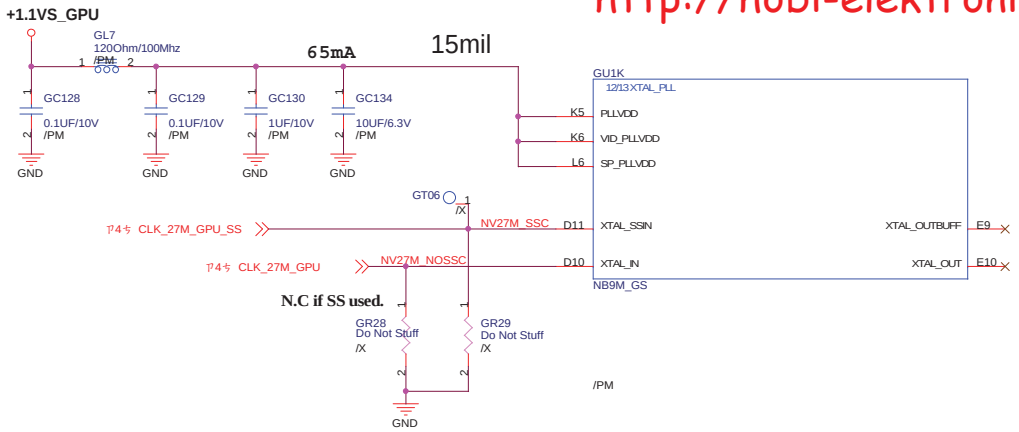
Title :

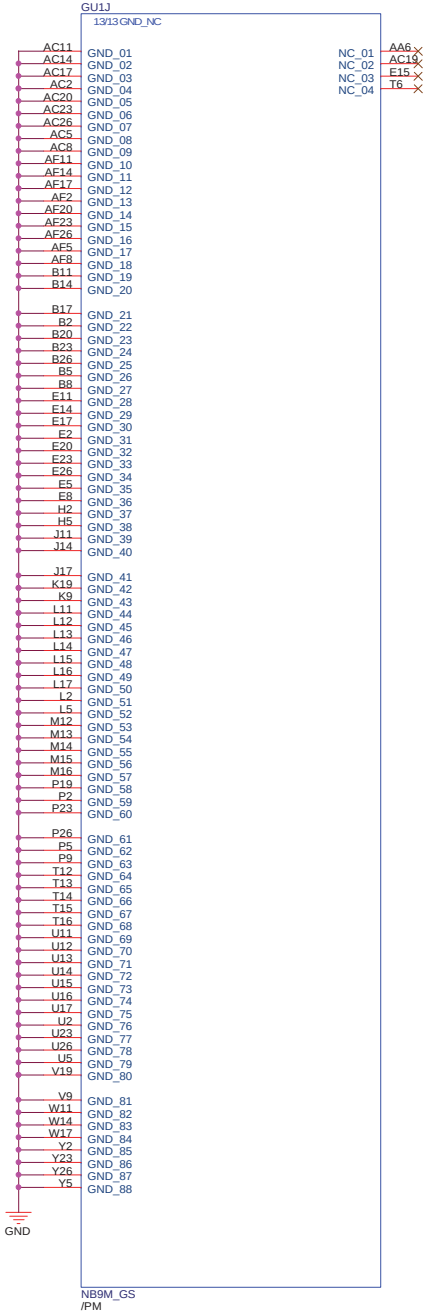
Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

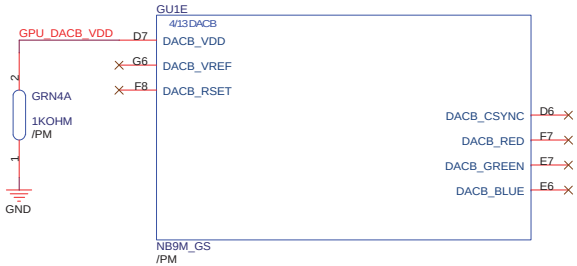
Date: Tuesday, December 16, 2008 Sheet 22 of 52

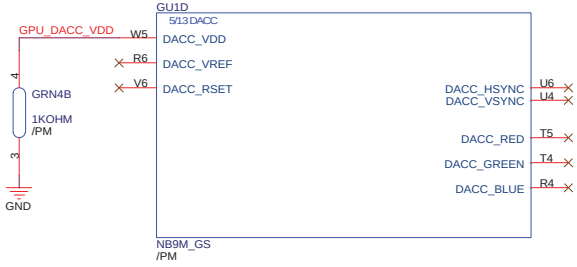
Xtal

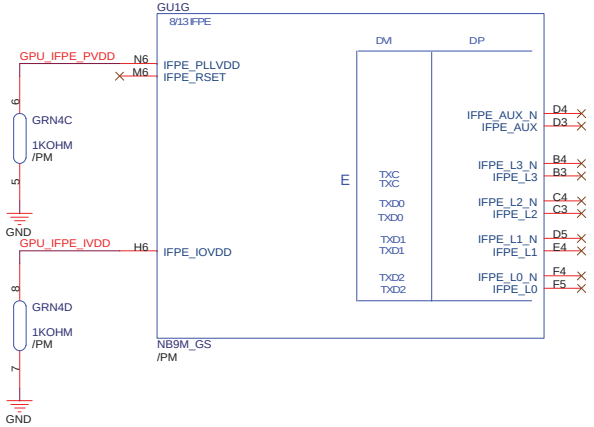




Other







P80VC1

ASUSTeK COMPUTER INC. NB1

Title :

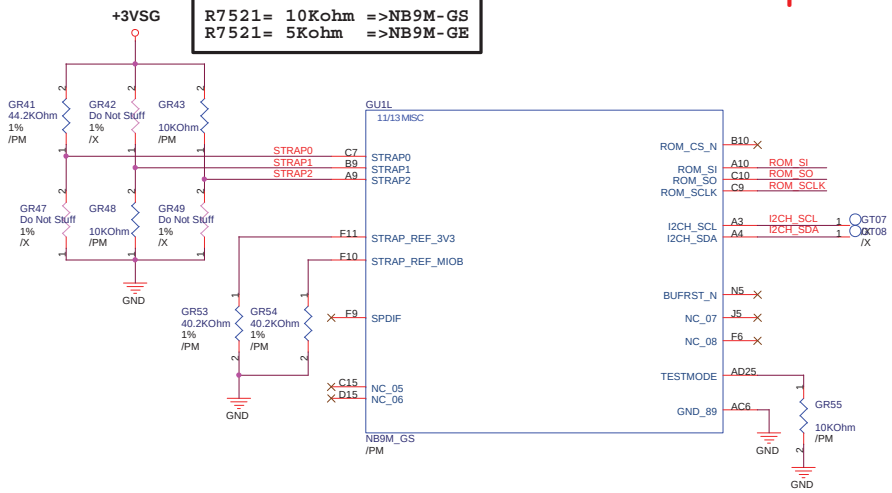
Engineer: SZ_NB2

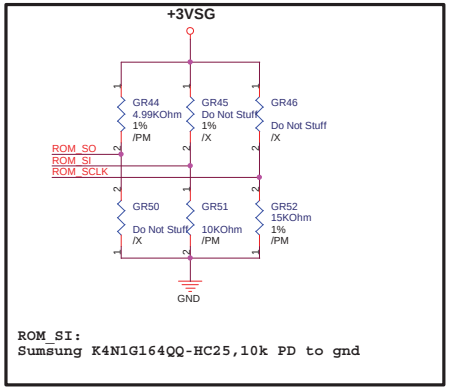
Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 23 of 52

ROM

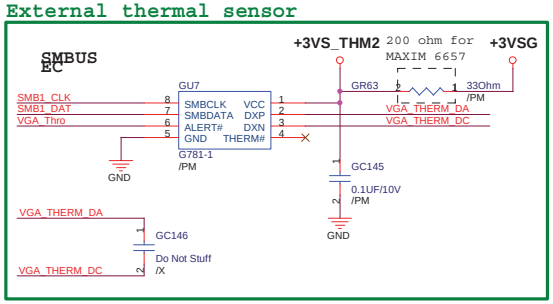
R7521= 10Kohm =>NB9M-GS
R7521= 5Kohm =>NB9M-GE

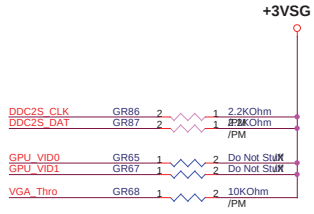


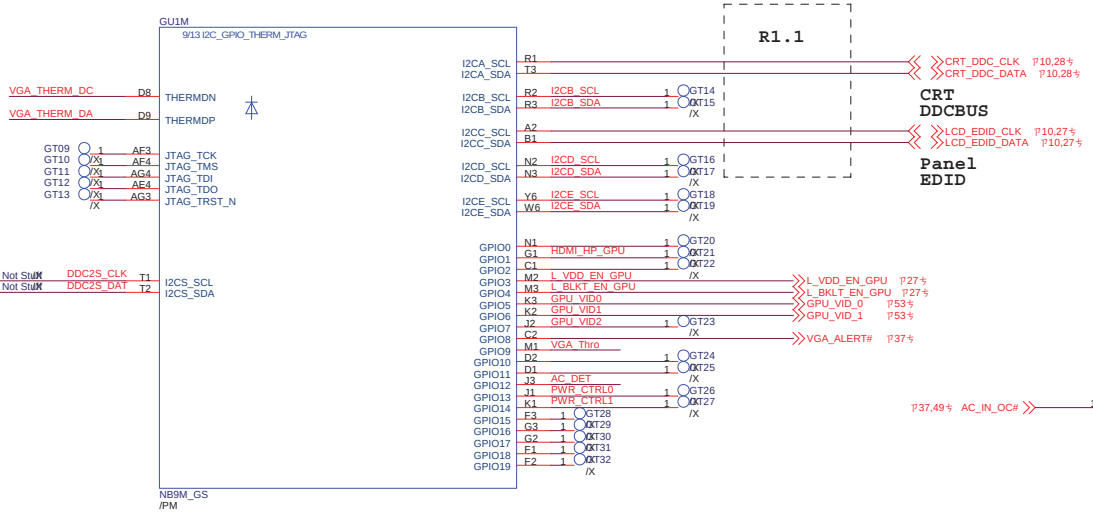


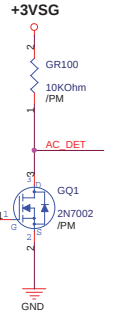
GPIO

External thermal sensor









GPIO ASSIGNMENTS

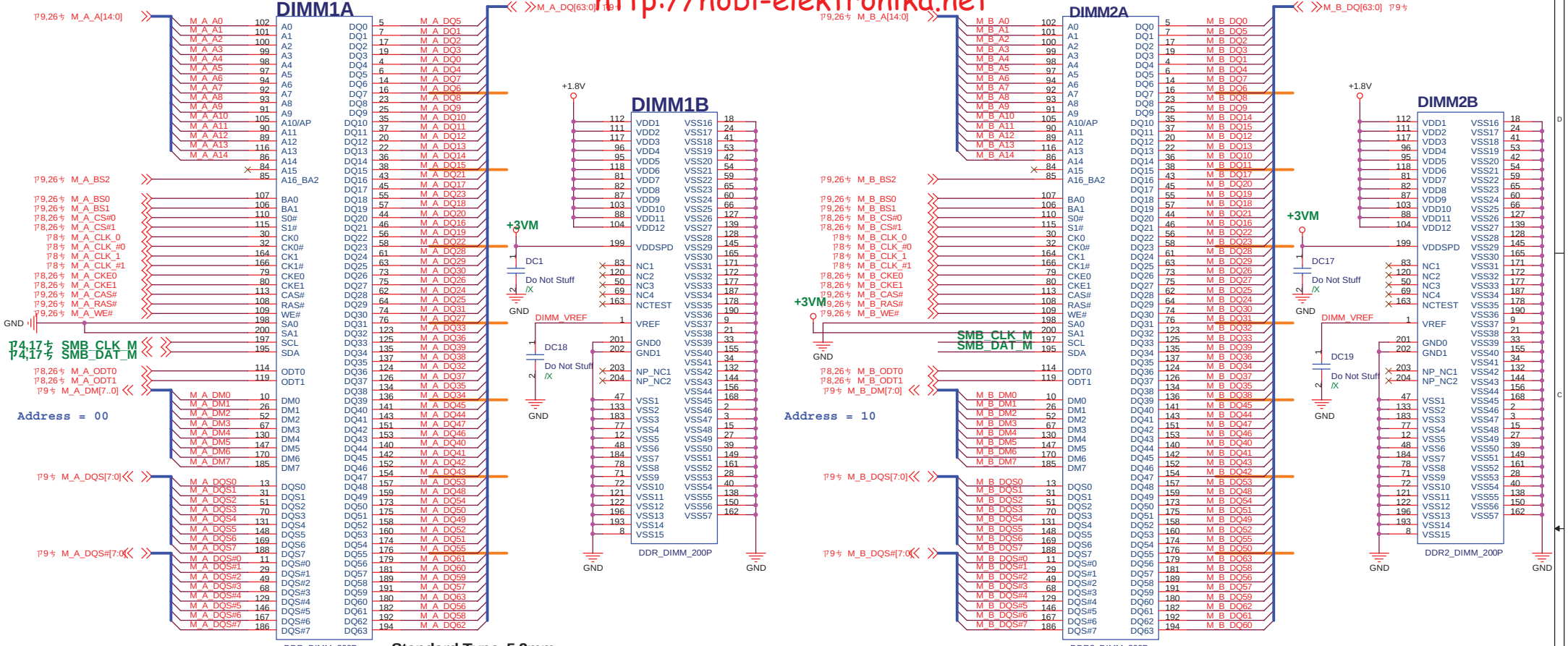
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	N/A
1	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID 0
6	OUT	N/A	NVVDD VID 1
7	OUT	N/A	FBVDD VID 0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	Low	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	N/A	PS CONTROL
14	OUT	N/A	PS CONTROL

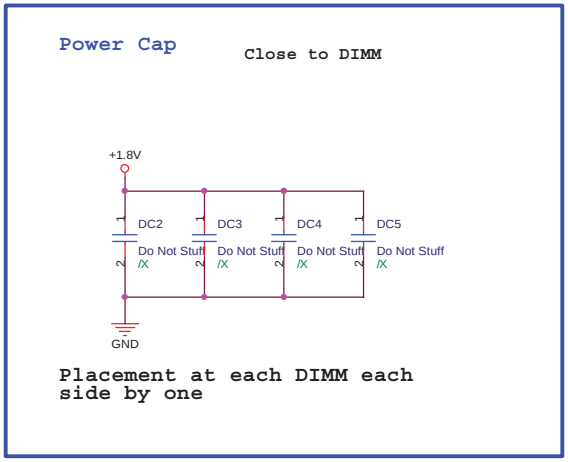
P80VC1

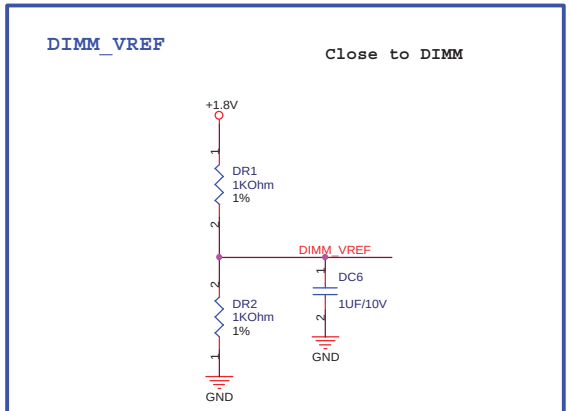
ASUSTeK COMPUTER INC. NB1 Engineer: SZ_NB2

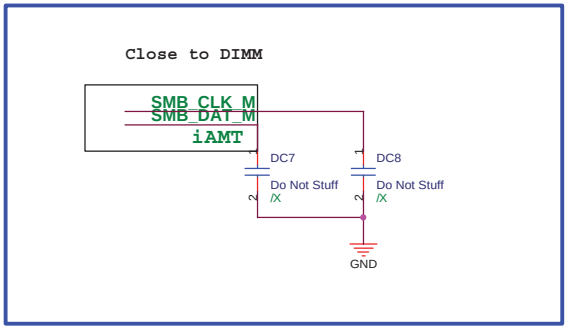
Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 24 of 52



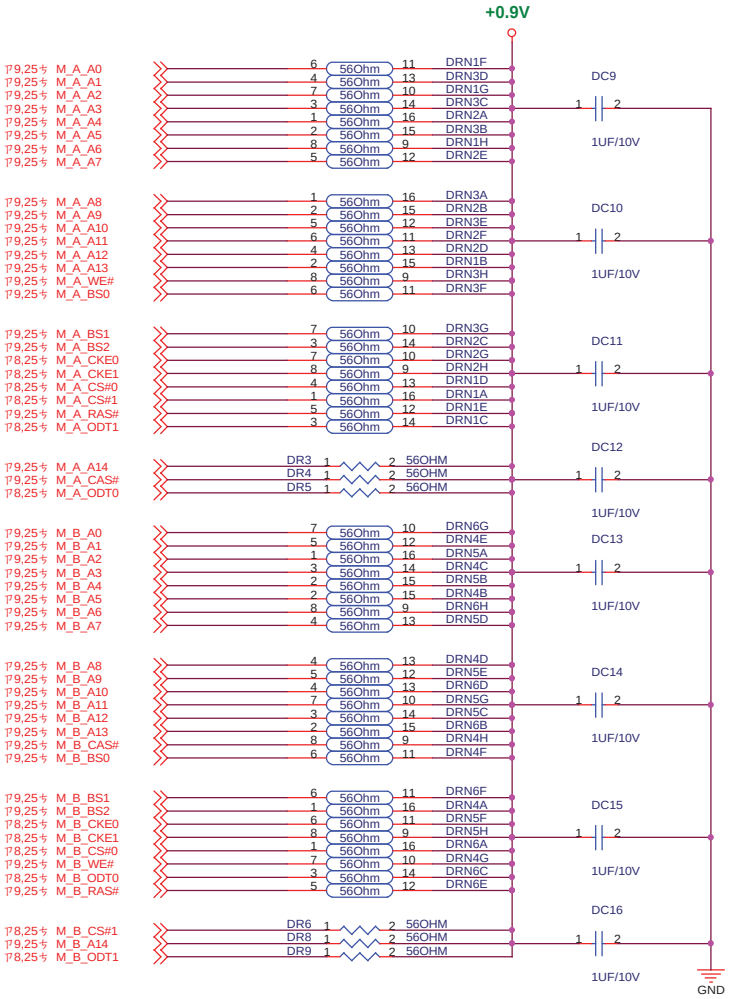






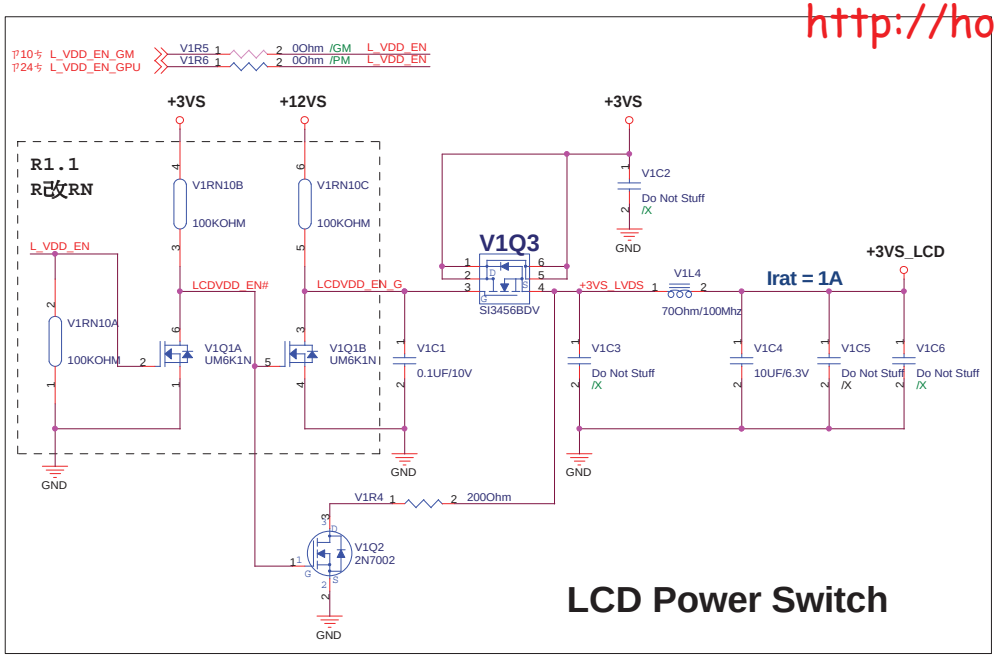
P80VC1

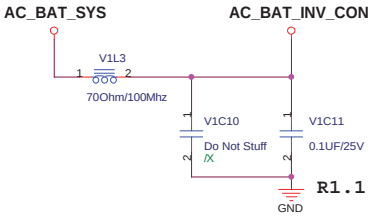
ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMMs	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 25 of 52	

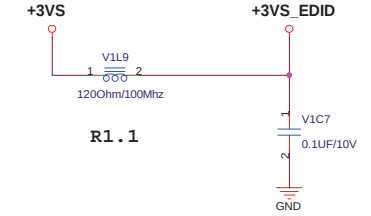


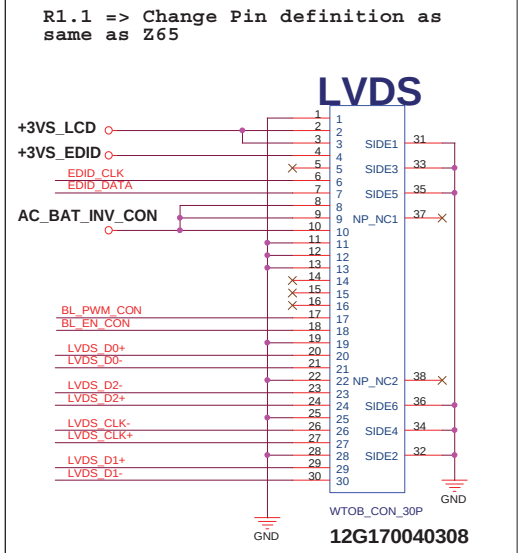
P80VC1

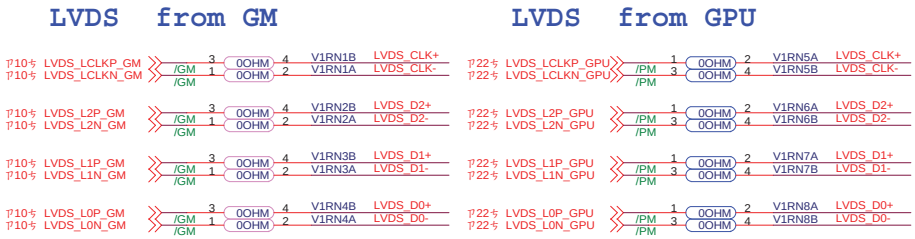
ASUSTeK COMPUTER INC. NB1	Title : DDR2 TERMINATION	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 26 of 52	

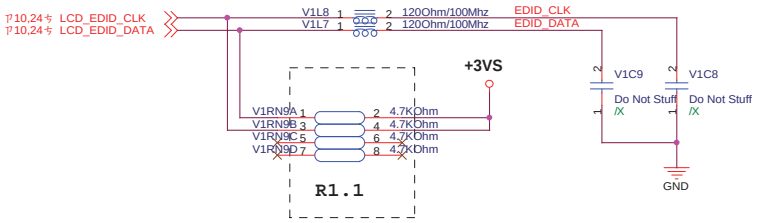


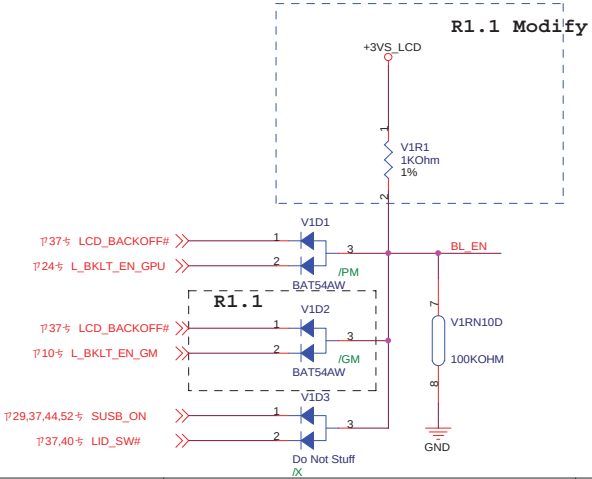


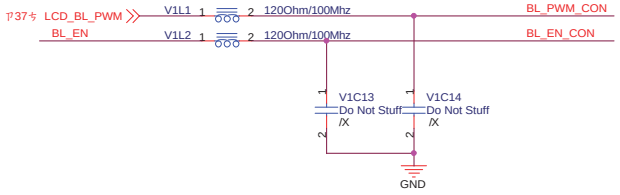










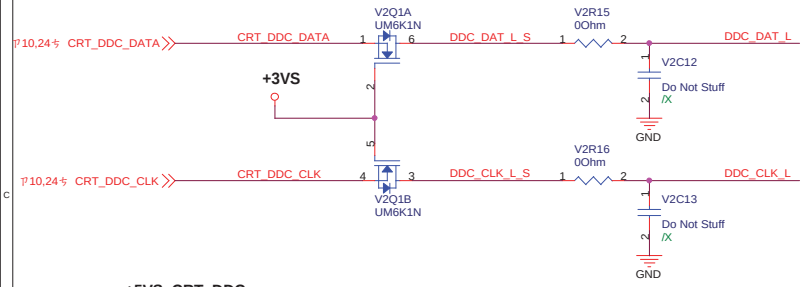


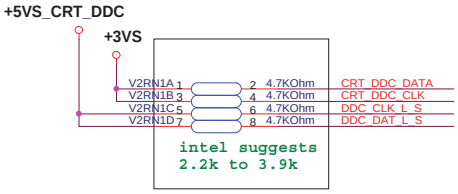
P80VC1

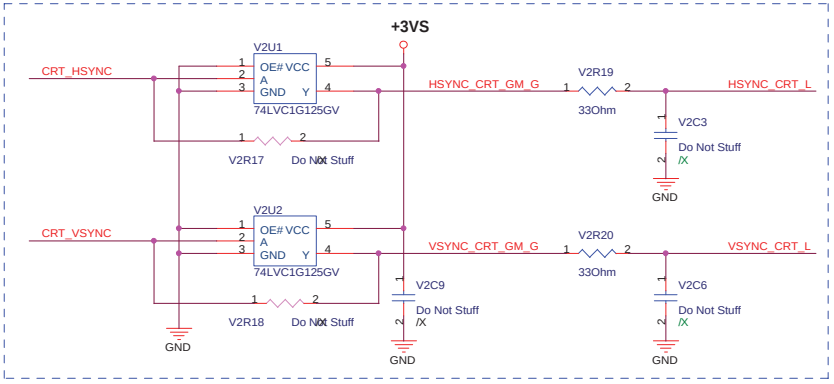
ASUSTeK COMPUTER INC. NB6	Title : LVDS conn	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A / Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 27 of 52	

From GMCH

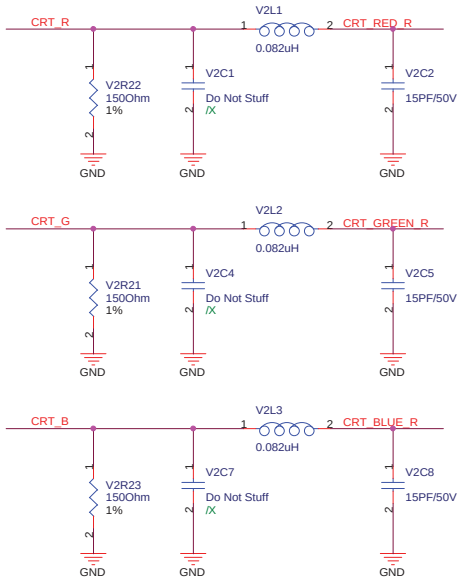
From GPU





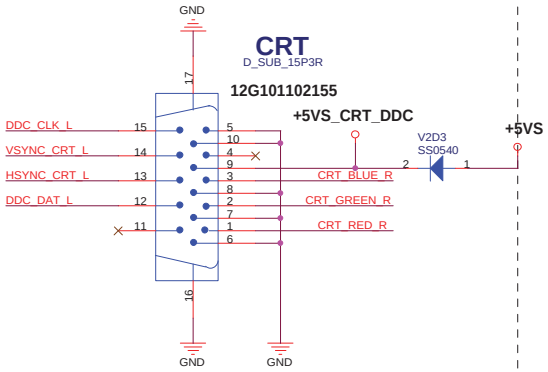


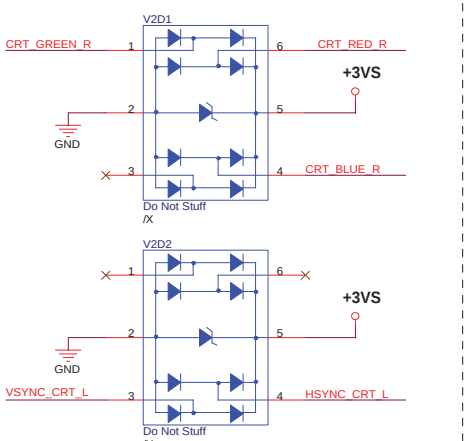
2008/12/4 : Pass EA measurement



R1.1 change P/N

CRT Connector





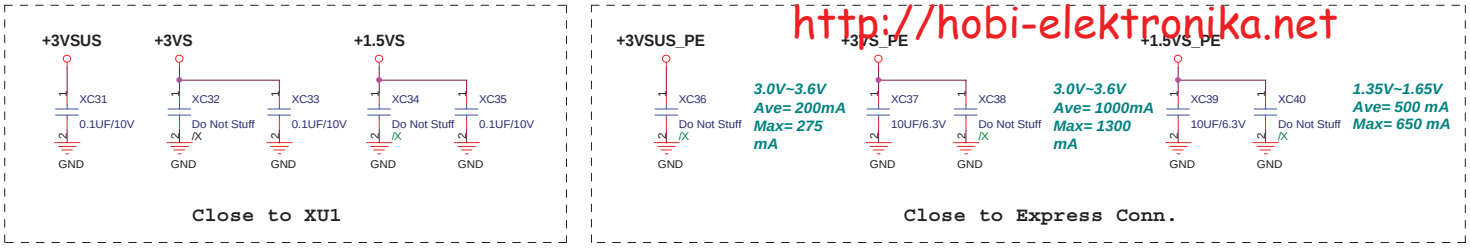
ESD Diodes

Place ESD Diodes near CRT Connector

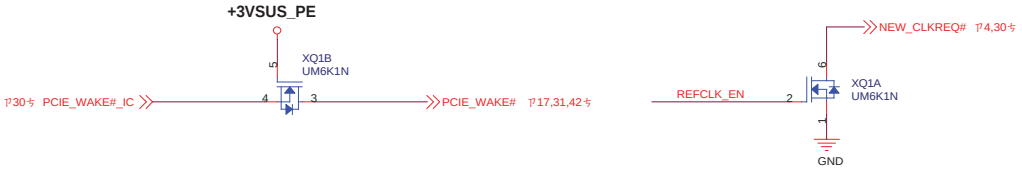
R1.1 /X

P80VC1

ASUSTeK COMPUTER INC. NB6	Title : CRT conn	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 28 of 52	

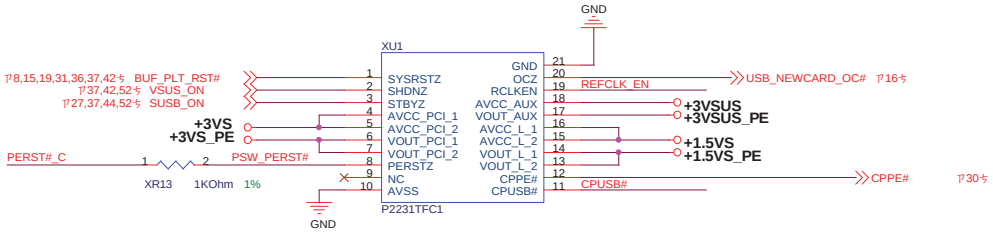


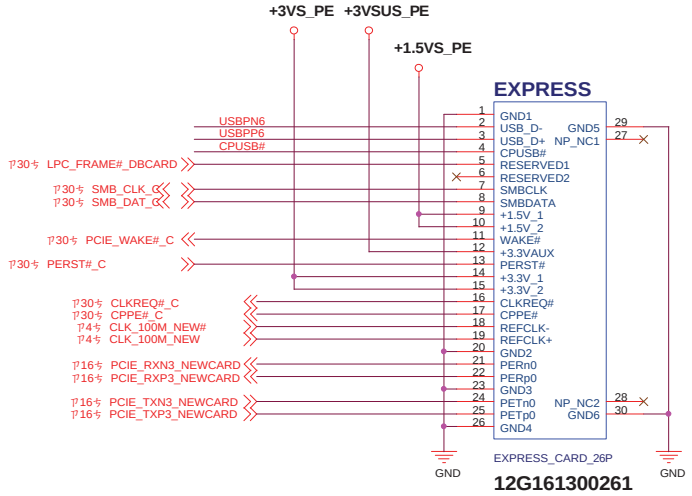
NewCard Header



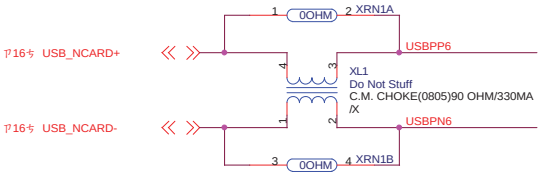
06G030057011 POWER SW. P2231TFC1 TSSOP-20 ENE P2231TFC1

06G030057012 POWER SW. P2231TFC2 TSSOP-20 ENE P2231TFC2

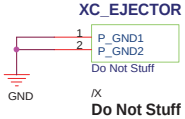




ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V



NewCard Ejector

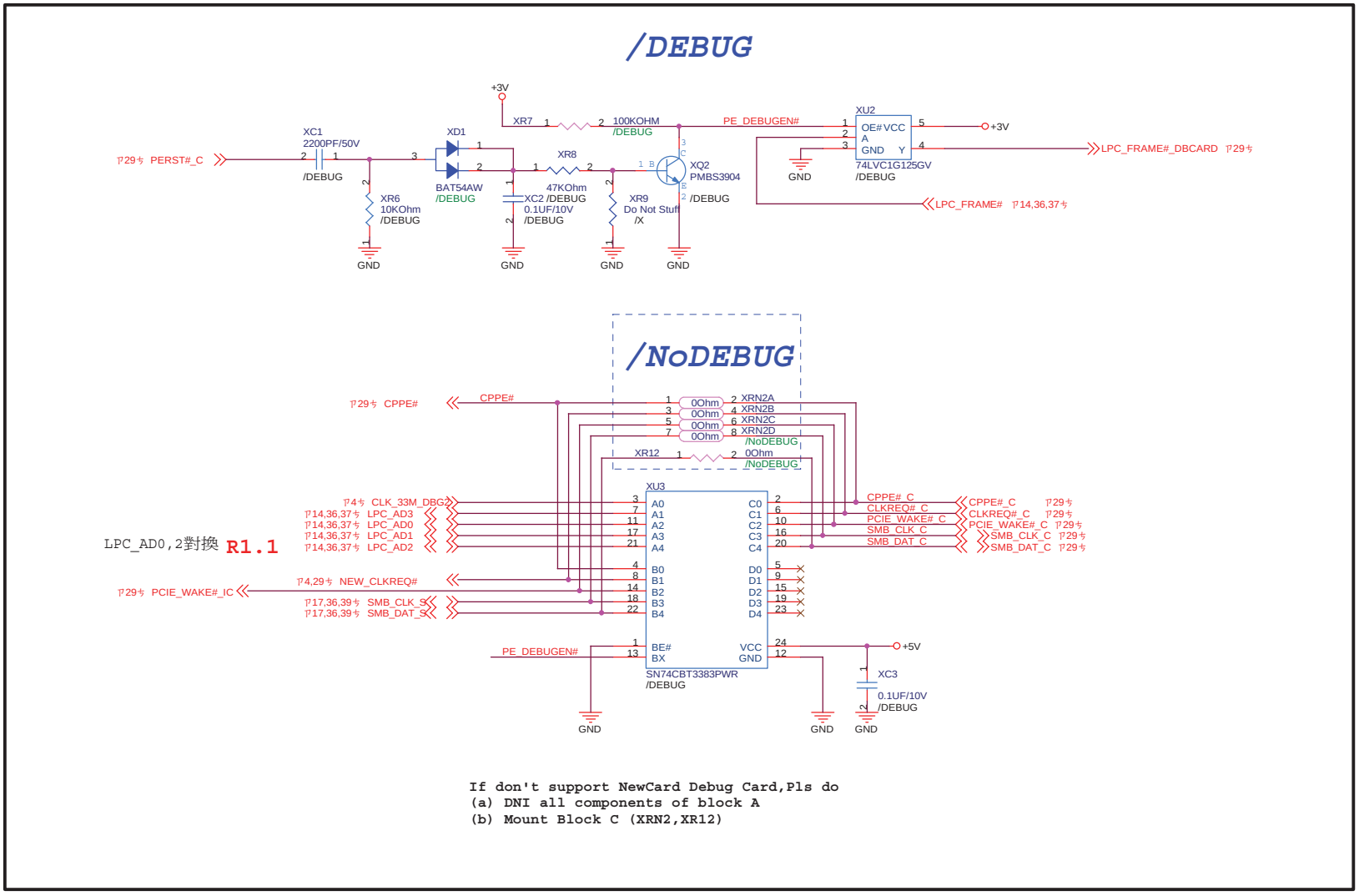


P80VC1

ASUSTeK COMPUTER INC. NB6 | Title : NEWCARD | Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

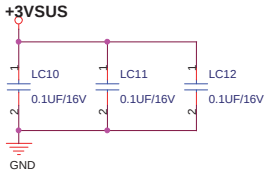
Date: Tuesday, December 16, 2008 Sheet 29 of 52



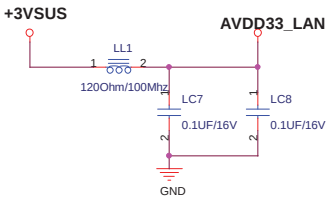
If don't support NewCard Debug Card,Pls do
(a) DNI all components of block A
(b) Mount Block C (XRN2,XR12)

P80VC1

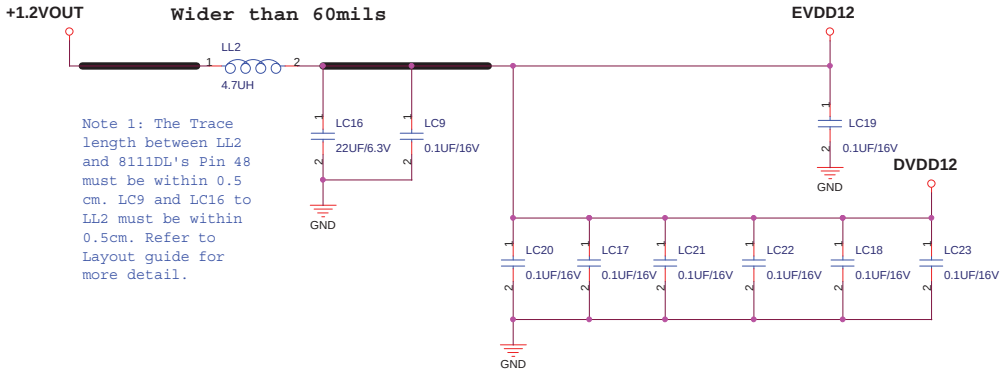
ASUSTeK COMPUTER INC. NB6	Engineer: SZ_NB2	Title : NEWCARD_DEBUG
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 30 of 52	



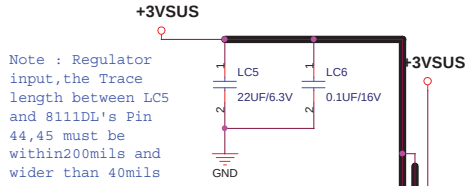
For VDD33 pin29, pin37



For AVDD33 pin1, pin40

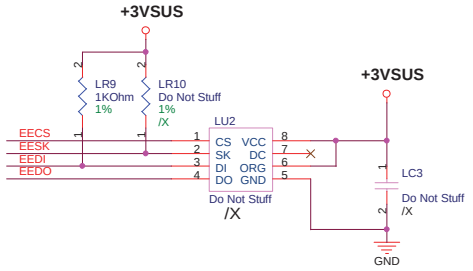


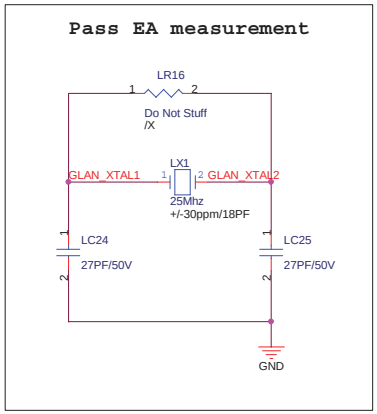
Note 1: The Trace length between LL2 and 8111DL's Pin 48 must be within 0.5 cm. LC9 and LC16 to LL2 must be within 0.5cm. Refer to Layout guide for more detail.

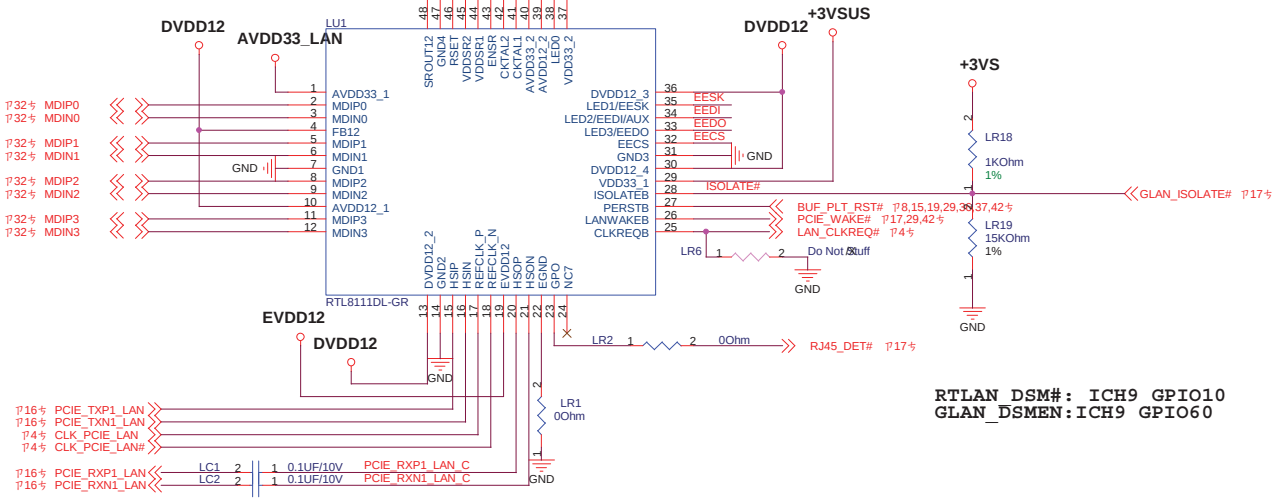


Note : Regulator input,the Trace length between LC5 and 8111DL's Pin 44,45 must be within200mils and wider than 40mils

Remove LR11 if switching regulator is enabled.
Remove LR14 if external power 1.2V is used.





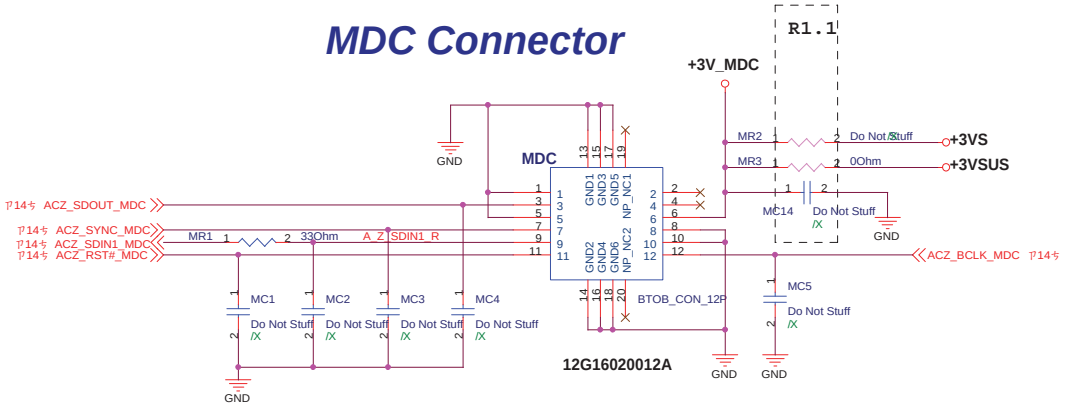


RTLAN_DSM#: ICH9 GPIO10
GLAN_DSMEN:ICH9 GPIO60

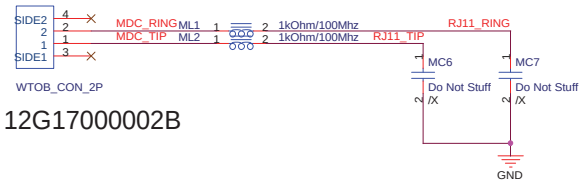
P80VC1

ASUSTeK COMPUTER INC. NB1	Title : SB-ICH9M(3)	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 31 of 52	

MDC Connector

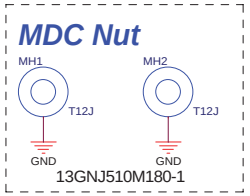


RING

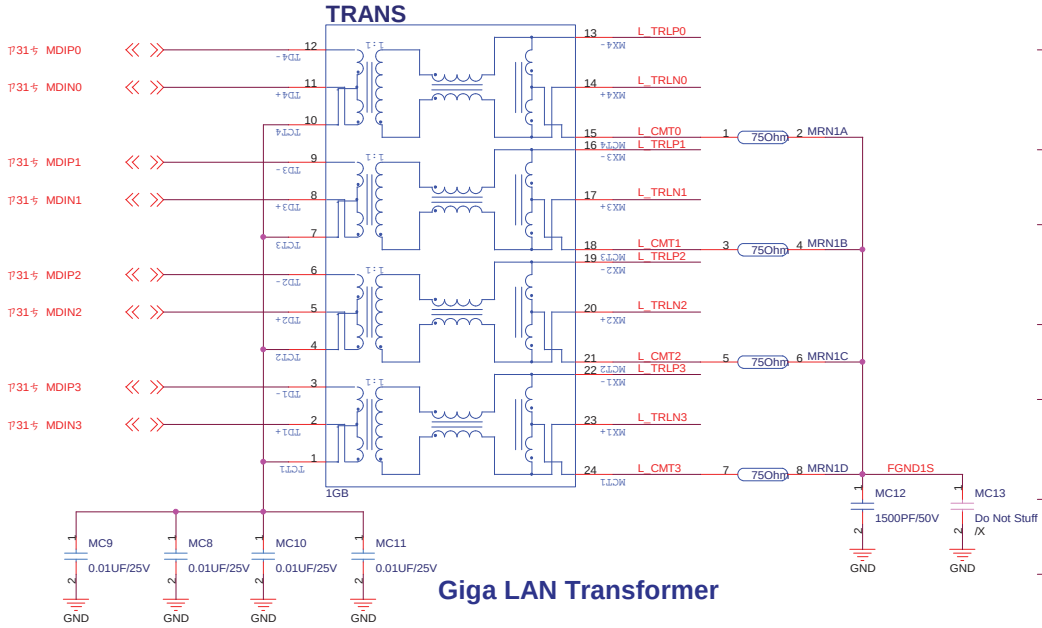


12G17000002B

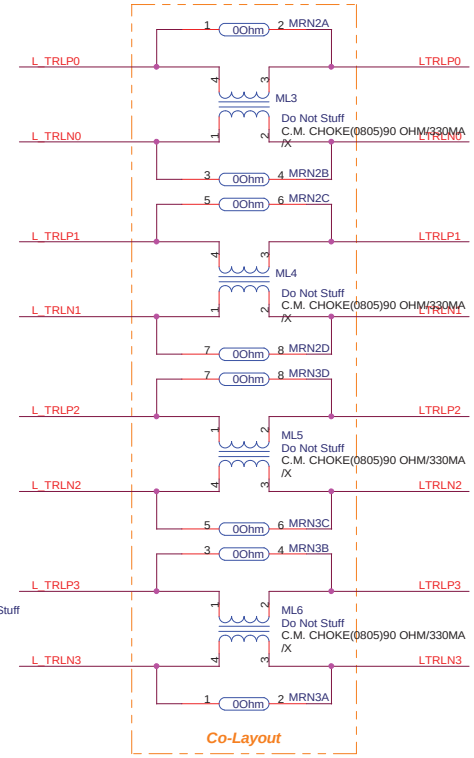
MDC Nut



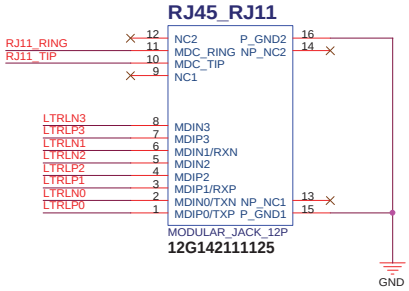
TRANS



Giga LAN Transformer



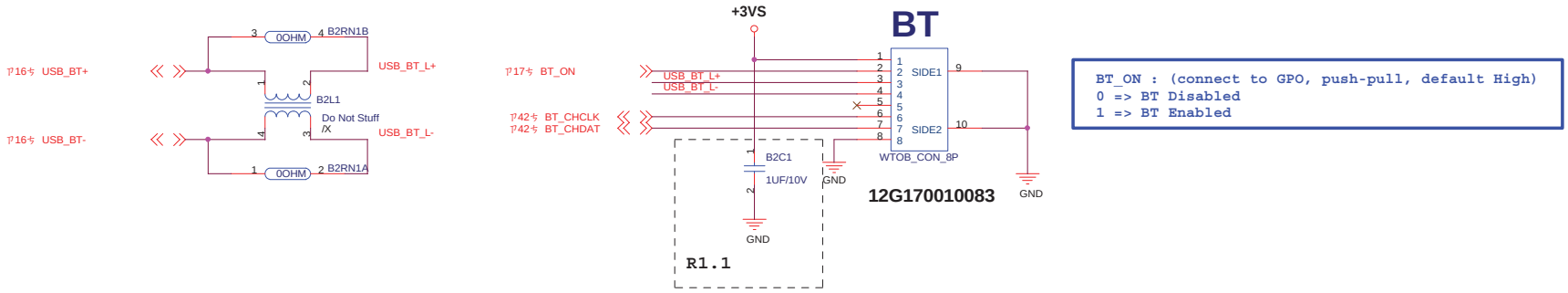
RJ45_RJ11



P80VC1

ASUSTeK COMPUTER INC. NB6	Title : RJ45-11&MDC	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 32 of 52	

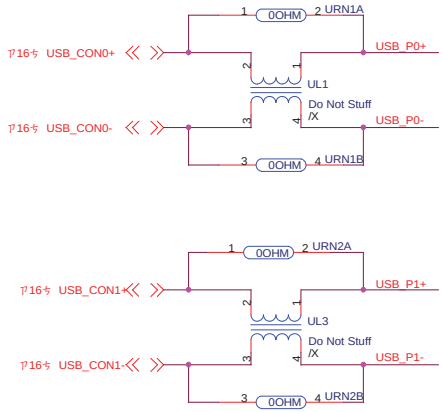
Bluetooth Connector

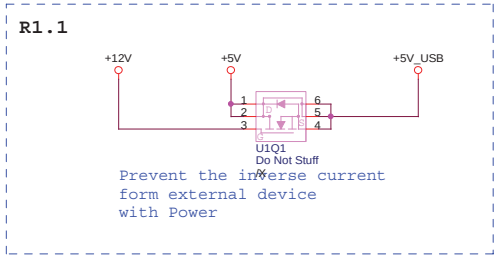


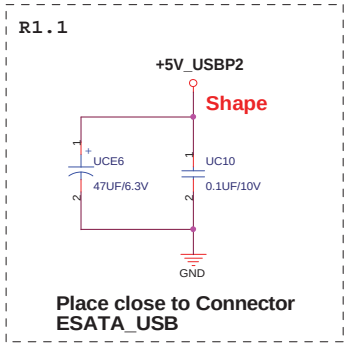
BT_ON : (connect to GPO, push-pull, default High)
0 => BT Disabled
1 => BT Enabled

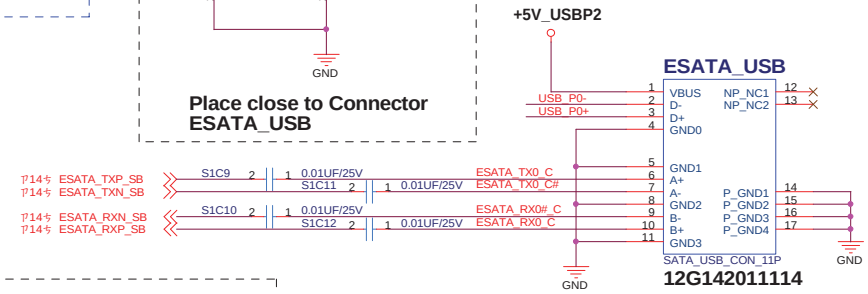
P80VC1

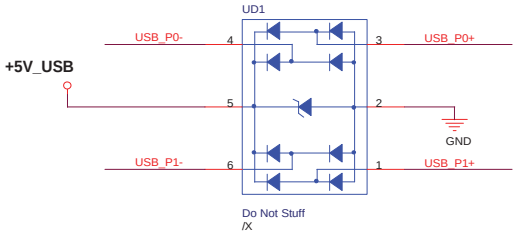
ASUSTeK COMPUTER INC. NB6	Title : BT&Launch	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 33 of 52	

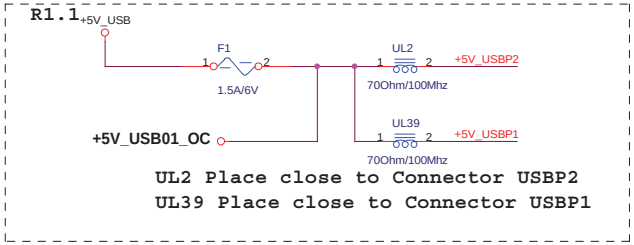


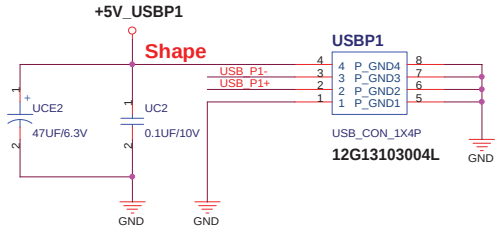








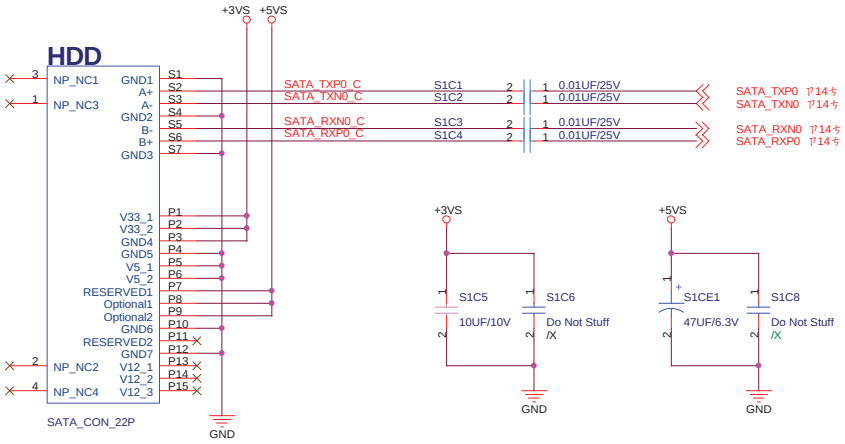




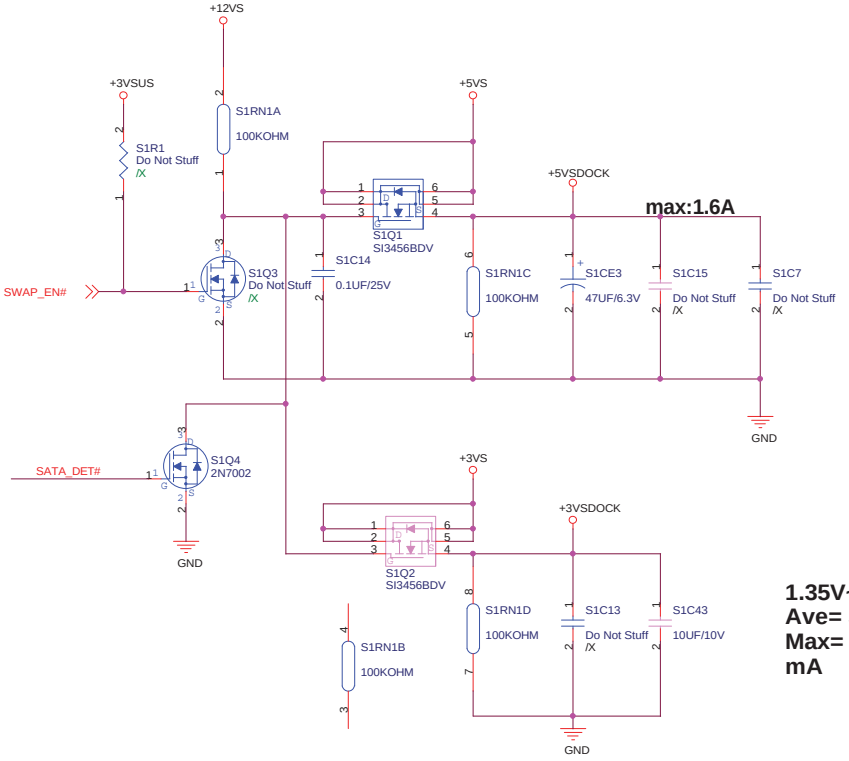
P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Audio Brd con&USB x2	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 34 of 52	

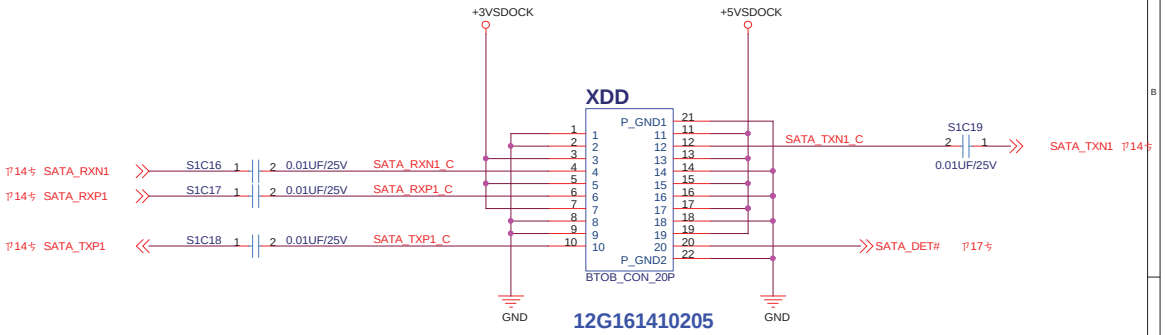
SATA HDD Connector



12G150200221



1.35V~1.65V
Ave= 500 mA
Max= 650
mA

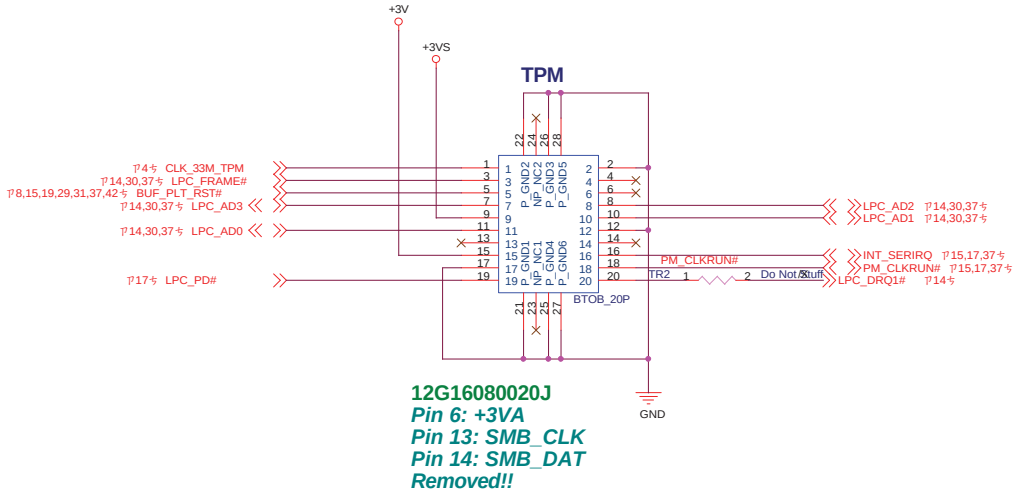


12G161410205

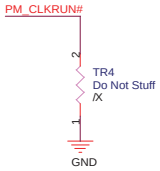
P80VC1

ASUSTeK COMPUTER INC. NB6	Title : SATA HDD	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 35 of 52	

TPM Connector



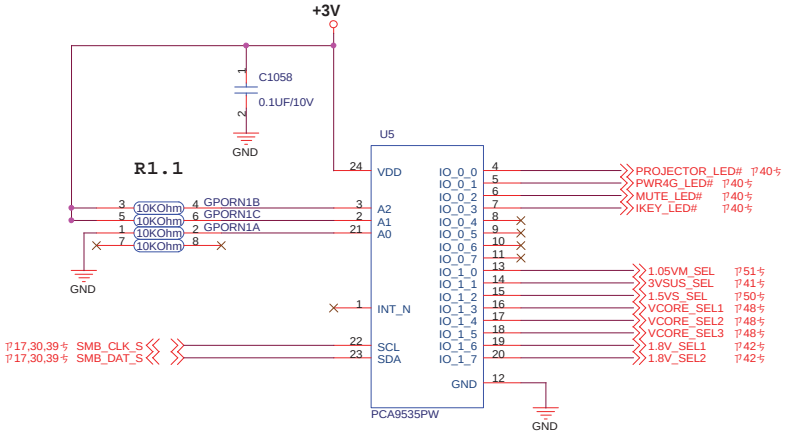
12G16080020J
Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
Removed!!



TPM Nut

13GNJ510M190-1

I2C GPIO Controller



P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Debug&TPM&GPIO	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 36 of 52	

For Discrete VGA

For IT8512 Power

R1.1 POWER GOOD DETECT

For EC Reset

close to the WRST# (IT8752E pin19)

Oringinal R = 160K OHM

For PU / PD

For X'tal

Note:
Cload=12.5PF
place close to EC

For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

Note: It can be programmable by EC fireware.

PP Enable

Note: Default Int. Pull-Low

For iAMT pin name

AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK

P80VC1

ASUSTeK COMPUTER INC. NB1

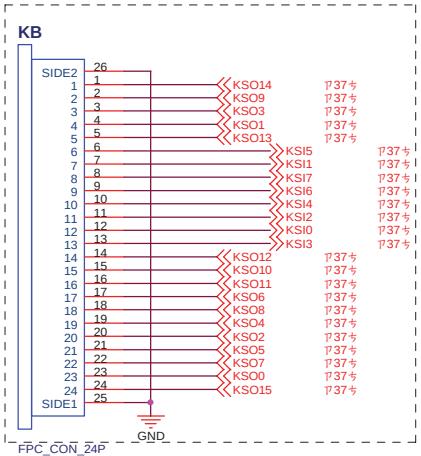
Title : EC ENE3925

Engineer: SZ_NB2

Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 37 of 52

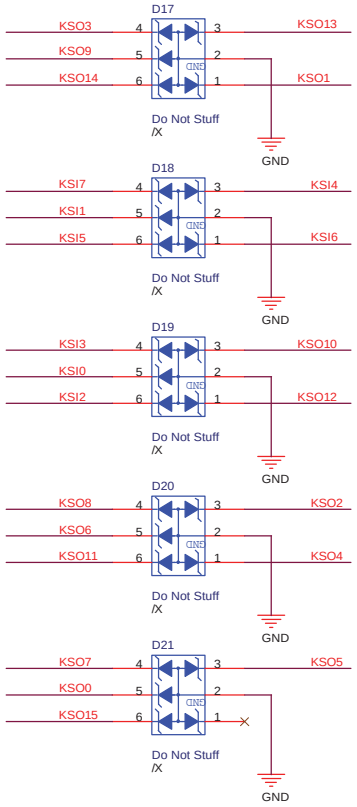
Keyboard Connector

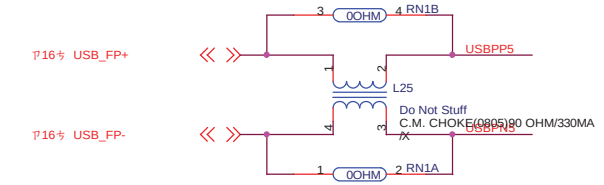


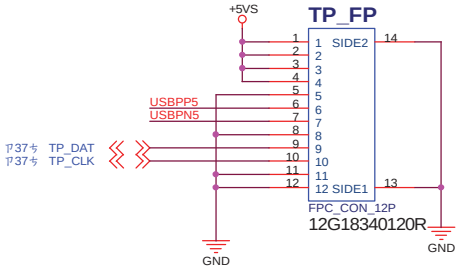
12G182102402

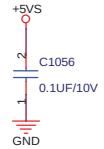
R1.1

FOR EMI/ESD

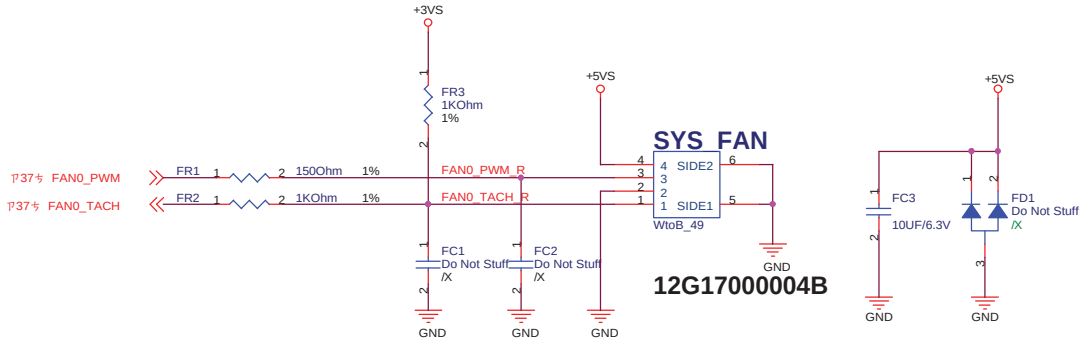








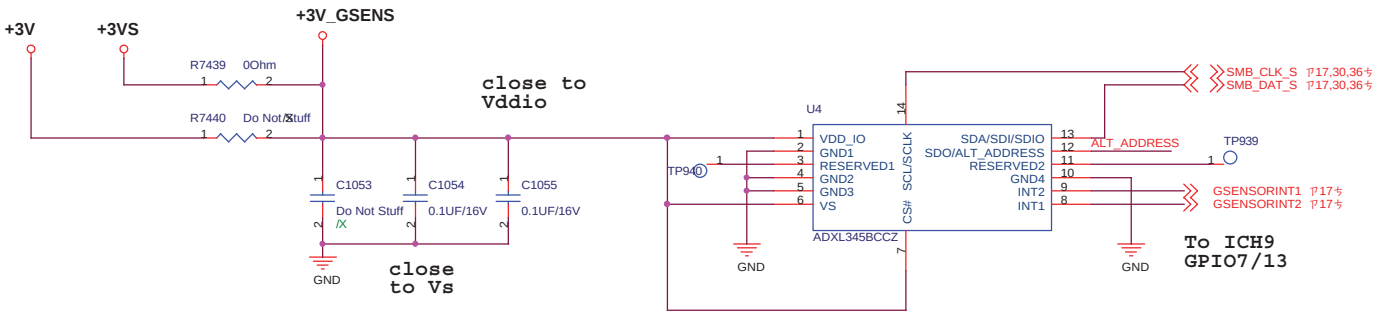
Place close to connector



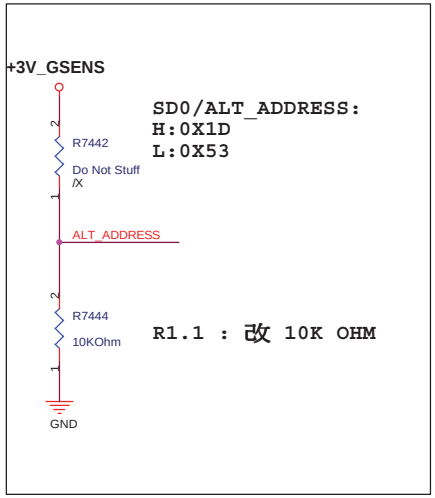
12G17000004B

P80VC1

ASUSTeK COMPUTER INC. NB6	Title : KB—TP	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 38 of 52	



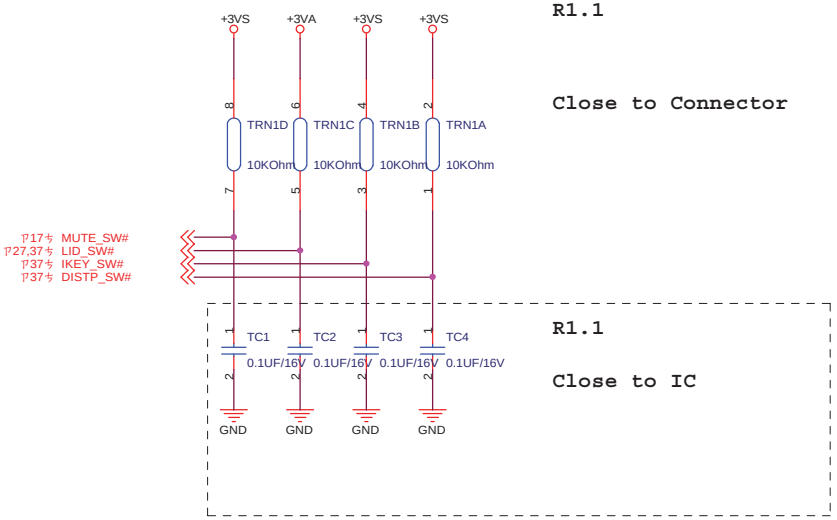
RESERVED
PIN3: connect to Vs or NC
PIN11: connect to GND or NC
CS#: Tie to Vddio to enable I2C mode.

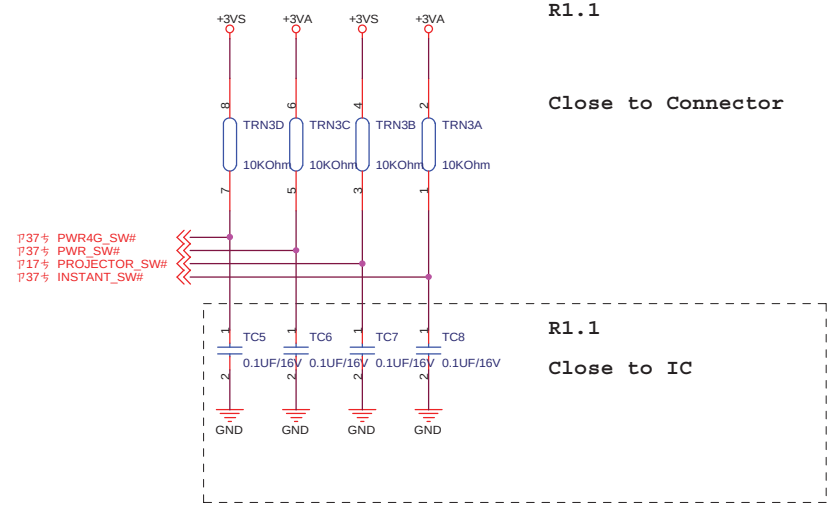


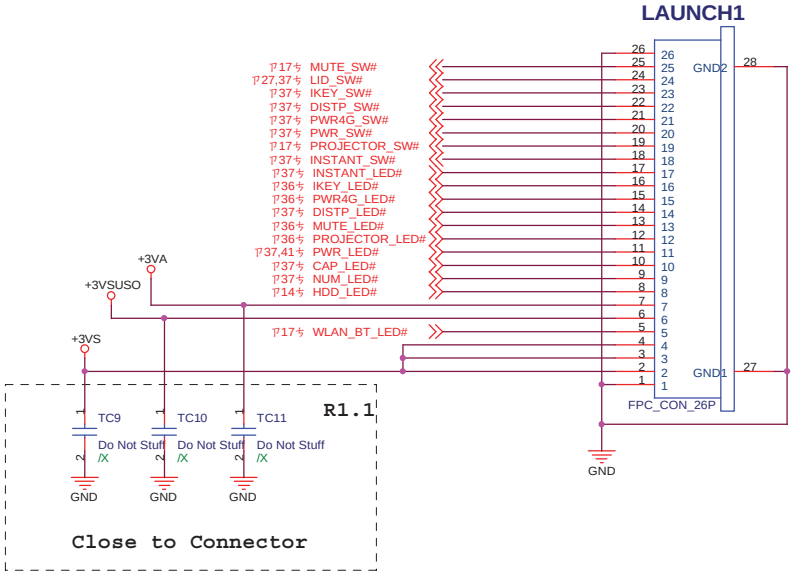
P80VC1

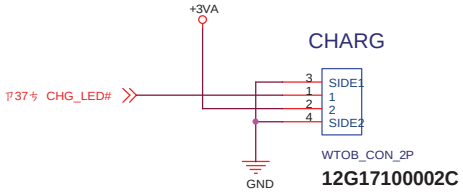
ASUSTeK COMPUTER INC. NB6	Title : Launch	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 39 of 52	

Debounced Circuits



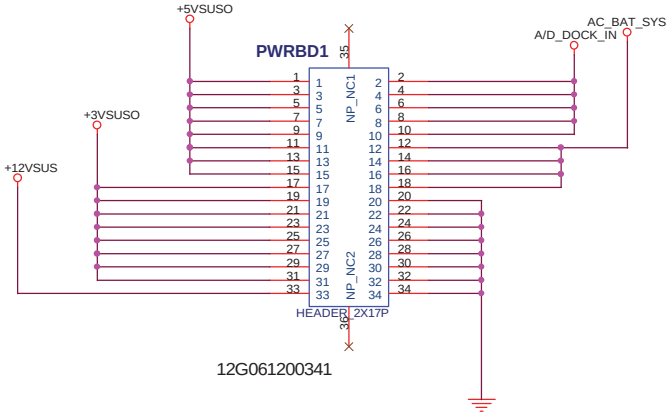




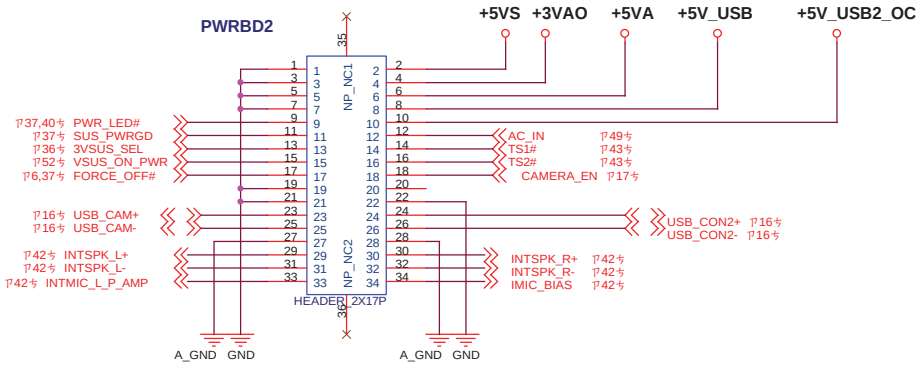


P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Launch	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 40 of 52	



12G061200341



12G061200341

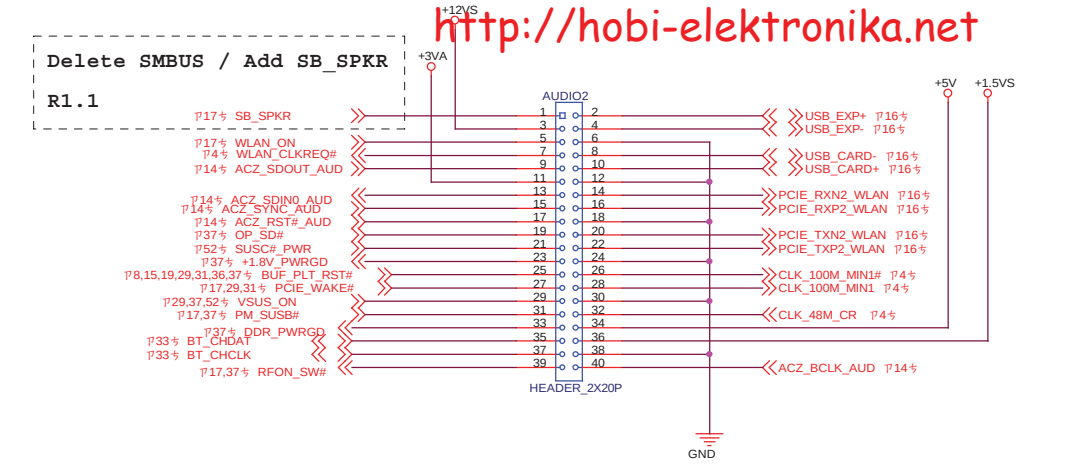
P80VC1

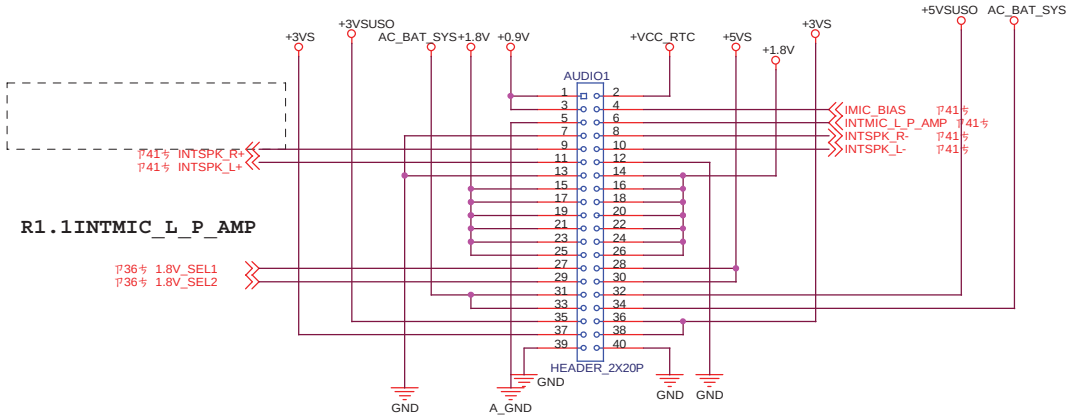
Title : other

ASUSTeK COMPUTER INC. NB6 Engineer: SZ_NB2

Size	Project Name	Rev
A3	P80VC / A/ Q	R1.1

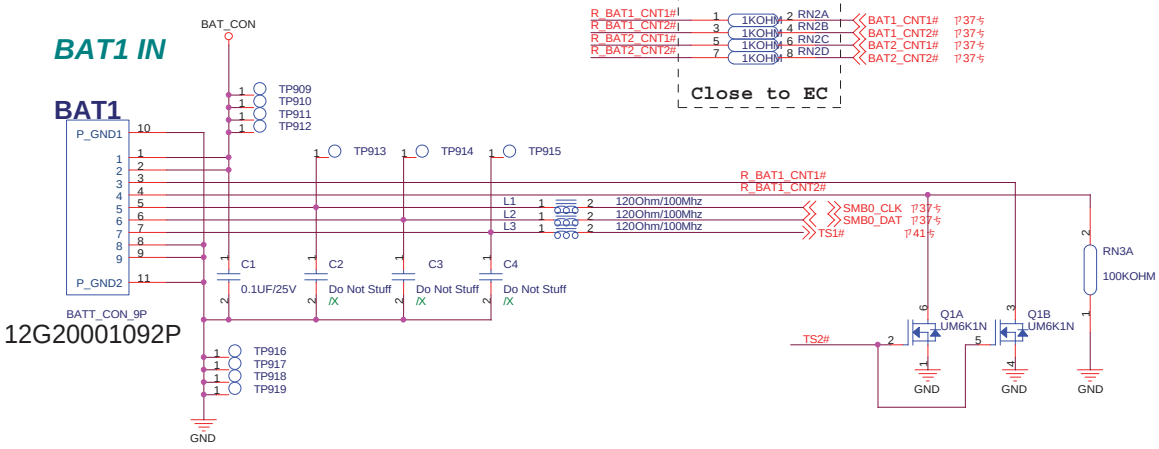
Date: Tuesday, December 16, 2008 Sheet 41 of 52

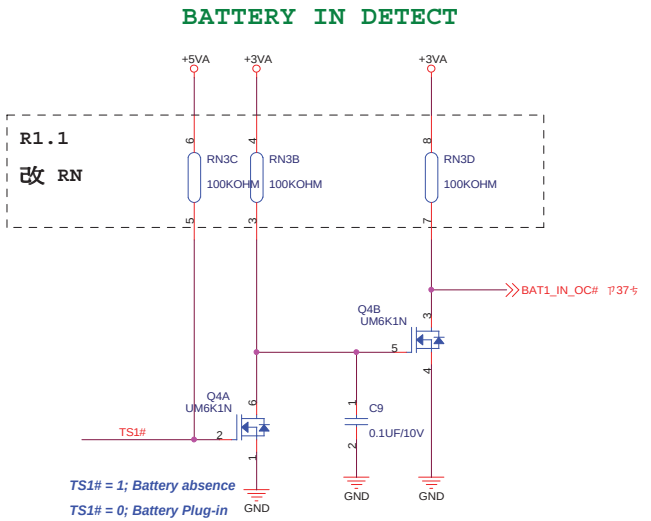


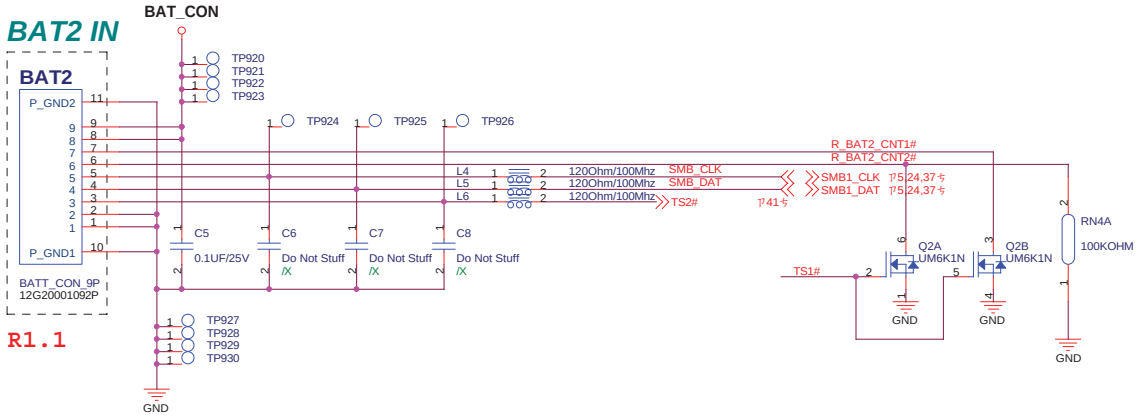


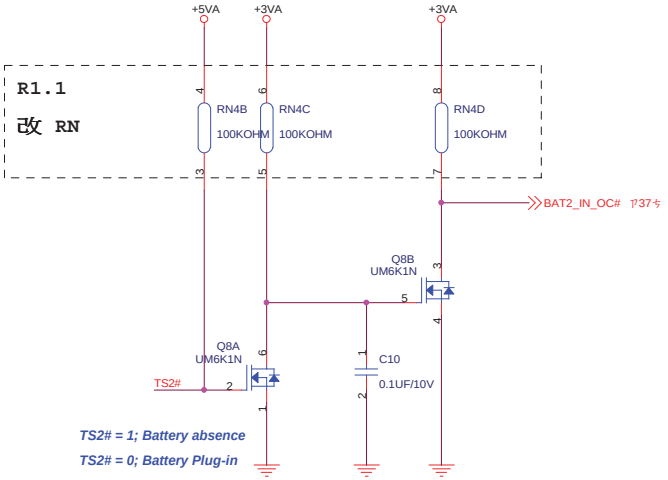
P80VC1

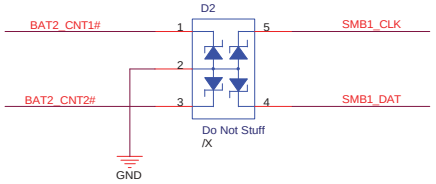
ASUSTeK COMPUTER INC. NB6	Title : other	
	Engineer: SZ_NB2	
Size: A3	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 42 of 52	

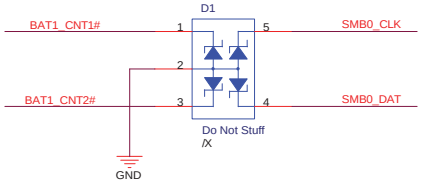






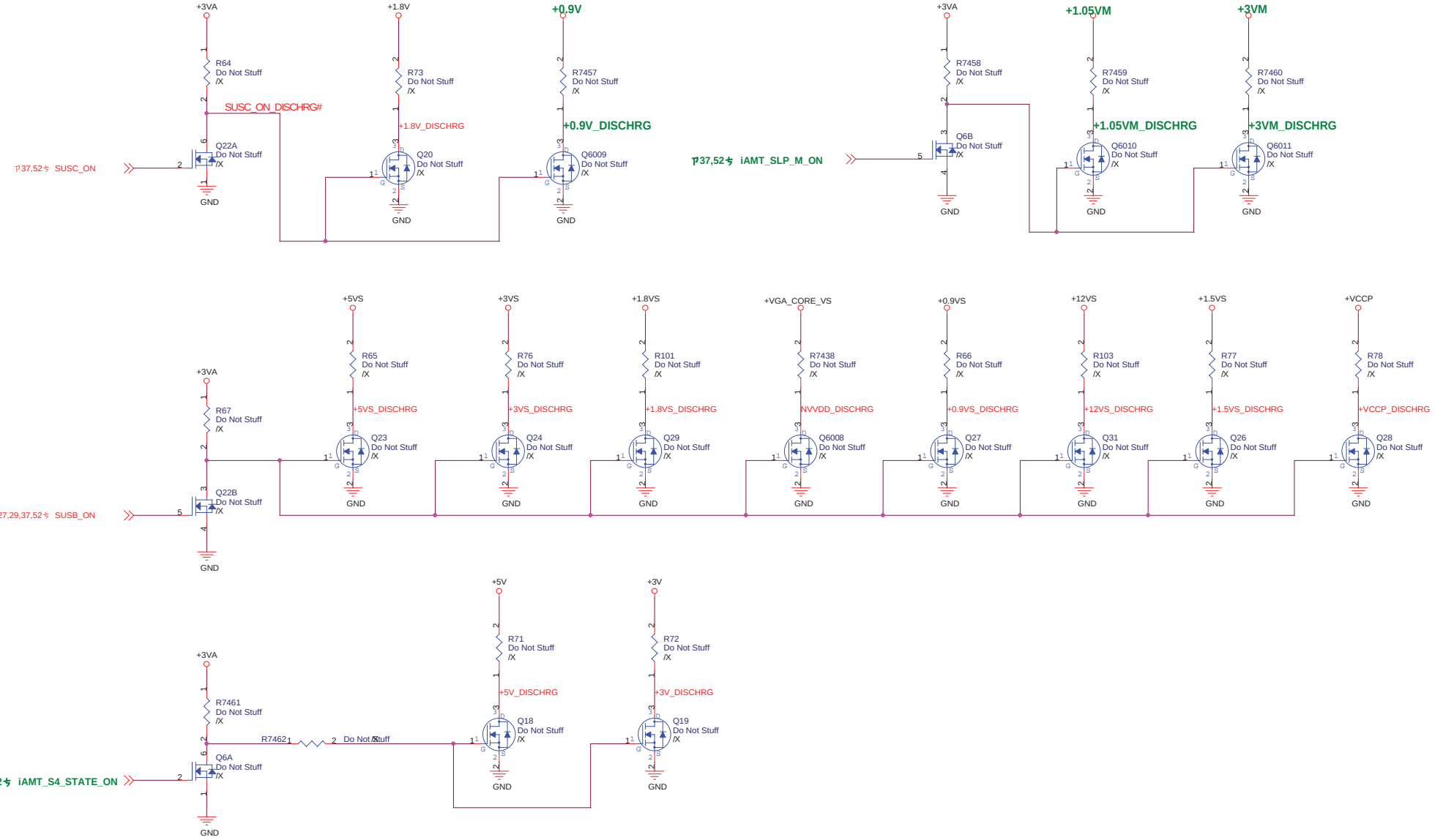






P80VC1

ASUSTeK COMPUTER INC. NB6	Title : DC-IN&BAT-IN	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 43 of 52	



P80VC1

Title : Discharger

ASUSTeK COMPUTER INC. NB6 **Engineer:** *SZ_NB2*

Size	Project Name	Rev
Custom	**P80VC / A/ Q**	R1.1

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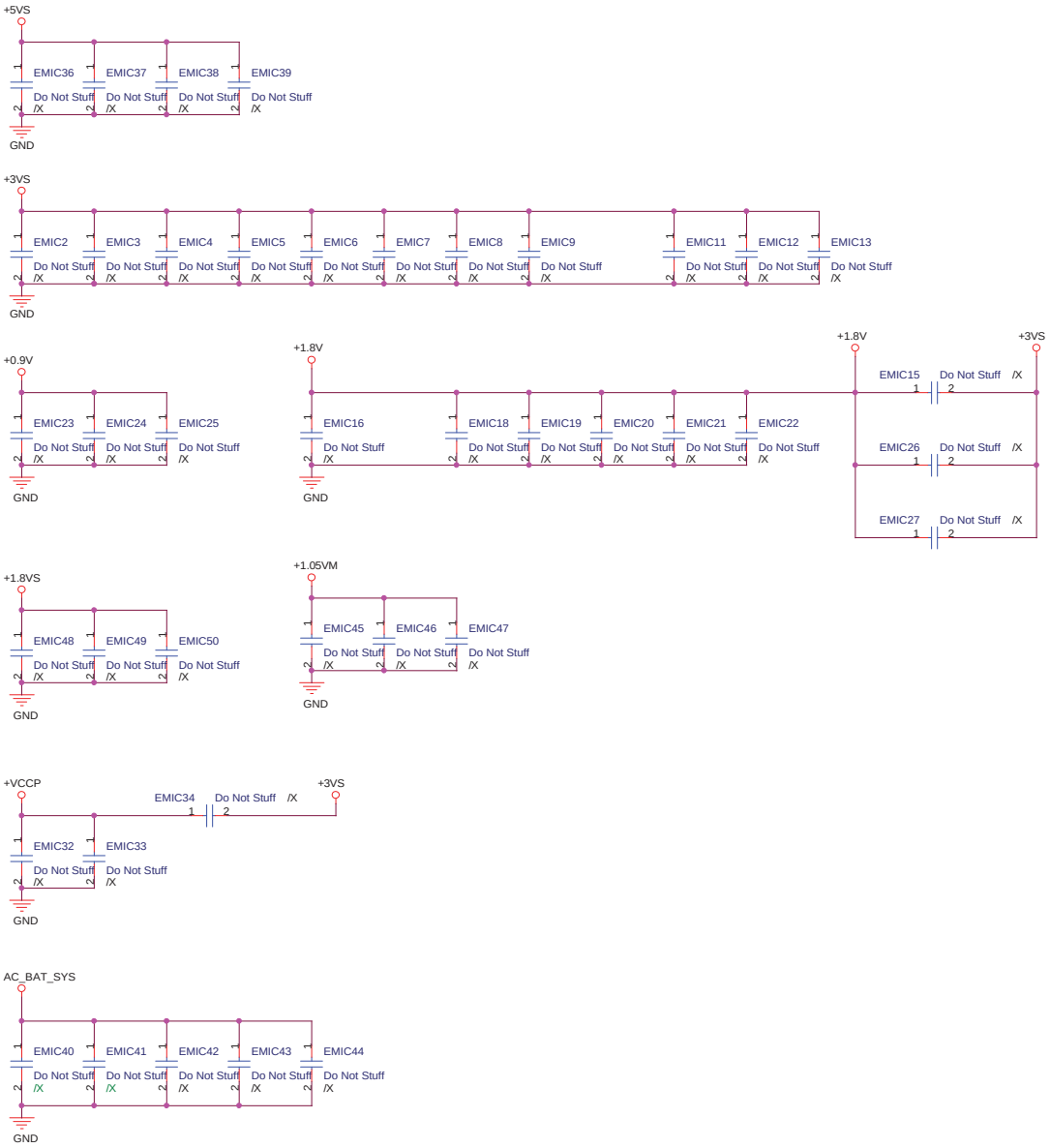


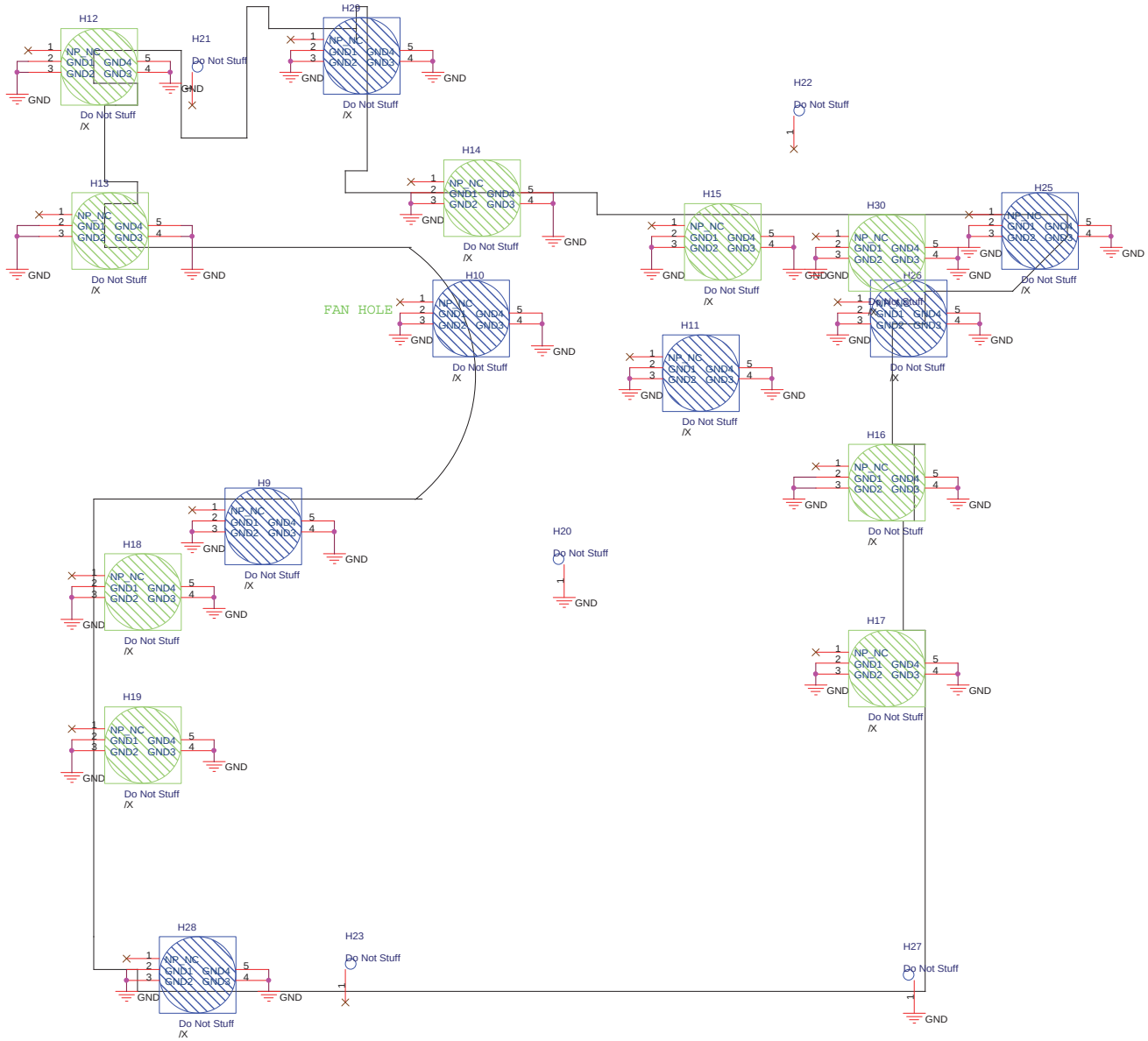
P80VC1

Title : EMI CAP

ASUSTeK COMPUTER INC. NB6 Engineer: SZ_NB2

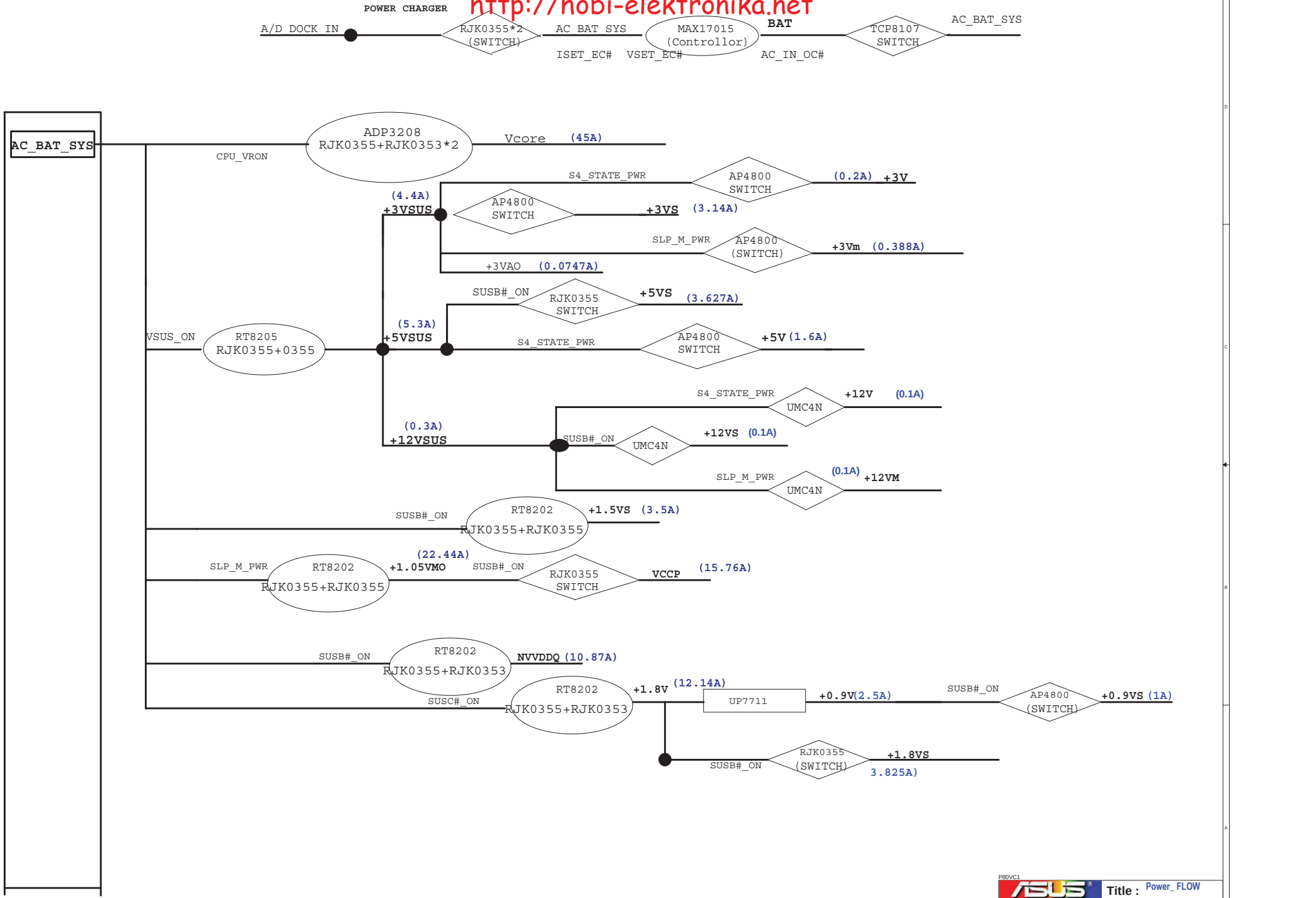
Size	Project Name	Rev
Custom	P80VC / A/ Q	R1.1

Date: Tuesday, December 16, 2008 Sheet 45 of 52



P80VC1

ASUSTeK COMPUTER INC. NB6	Title : Screw Hole	
	Engineer: SZ_NB2	
Size: Custom	Project Name: P80VC / A/ Q	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 46 of 52	



P80VC1

ASUSTeK COMPUTER INC	Title : Power_ FLOW	
	Engineer: N/A	
Size: C	Project Name: P80M	Rev: 1.1
Date: Tuesday, December 16, 2008	Sheet 47 of 54	

(45A)

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.33 A
2. Ripple Current:
   Iripple=3A
3. Ripple Voltage:
   Vripple=Iripple*ESR=13.5mV
4. Dynamic:
   Ipeak=45A
   ESR=4.5mohm
   V=100mV
5. Inductor Spec:
   Isat=26A
   Idc=20.8A
   Rdcmax=1.09mOhm
   Rdcmtyp=1.02mOhm
6. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355/RJK0353
   Rds(on)=11.8/5.4mOhm (Vgs=4.5V)
   Icont=30/35A (T=25)/
   Ipeak=120/140A (Pause<10us)

Controller

1. Voltage & Current:
   +VCORE:1.1V/45A
2. Frequency:
   Setting the clock Frequency:
   RT=(Vvid+1.0V)/(2*n*Fsw*7.2pF)-35Kohm
   Fsw=2.05V/(4*7.2pF*235Kohm)=303K
3. OCP:
   DCR*Imax*R2/(R1+R2)=22.5mV
   Imax=10.87A
4. tss time:
   TSS=1.8ms TSt=1.8ms
5. LoadLine:
   Out Droop Resistance :
   Ro=Rcs*Rsense/Rph
   =206.69Kohm*1.02mohm/120Kohm=1.76mohm

VCORE_SEL1	VCORE_SEL2	VCORE_SEL3	Voltage
0	1	1	VID-100mV
1	0	1	VID-50mV
1	1	1	VID
1	1	0	VID+50mV

Current limit:
Rclim=Rcs*10*Rsense*Iclim*2/(Rph*10uA*n)
162Kohm=206.69*10*1ohm*I*2/(100Kohm*10uA*2)
I=78.38A

Setting the clock Frequency:
RT=(Vvid+1.0V)/(2*n*Fsw*7.2pF)-35Kohm
Fsw=2.05V/(4*7.2pF*235Kohm)=303K

Out Droop Resistance :
Ro=Rcs*Rsense/Rph
=206.69Kohm*1mohm/100Kohm=2.07mohm

P80VC1

ASUSTek Computer INC.

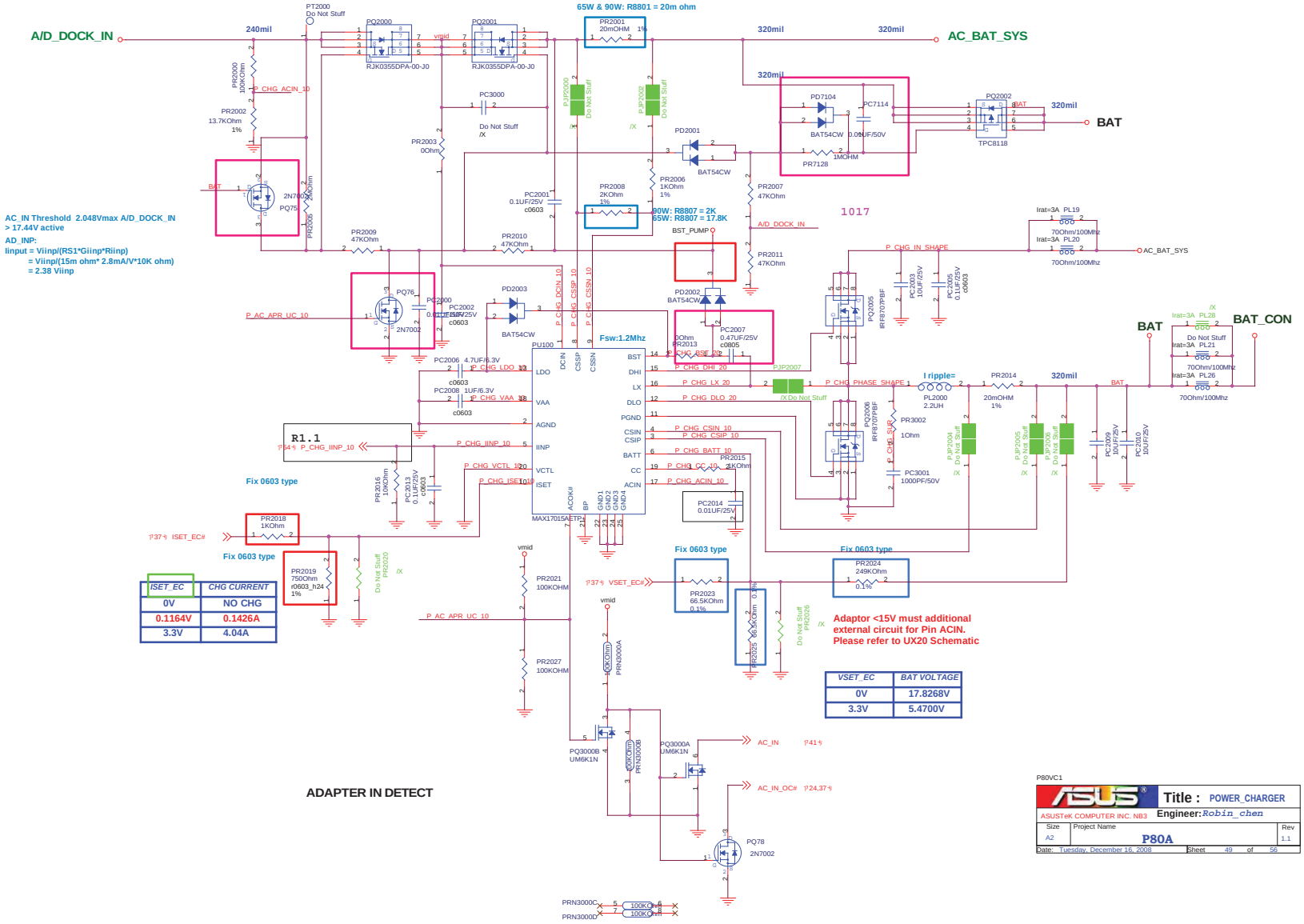
Title : POWER_VCORE

Engineer: Robin_chen

Size	Project Name	Rev
A2	P80	1.1

Date: Tuesday, December 16, 2008 Sheet 48 of 56

POWER PATH & BAT_LEARN



ISET_EC	CHG CURRENT
0V	NO CHG
0.1164V	0.1426A
3.3V	4.04A

VSET_EC	BAT VOLTAGE
0V	17.8268V
3.3V	5.4700V

Power stage

1. Ripple Current:
   Iripple=3A
2. Inductor Spec:
   Isat=14A
   Idc=8A
   DCR=18mOhm
3. MOSFET Spec:
   H-side and L-side MOSFET:AP4800
   Rds(on)=21mOhm (Vgs=4.5V)
   Icont=9.6 (T=25)
   Ipeak=40 (Pause<10us)

Controller

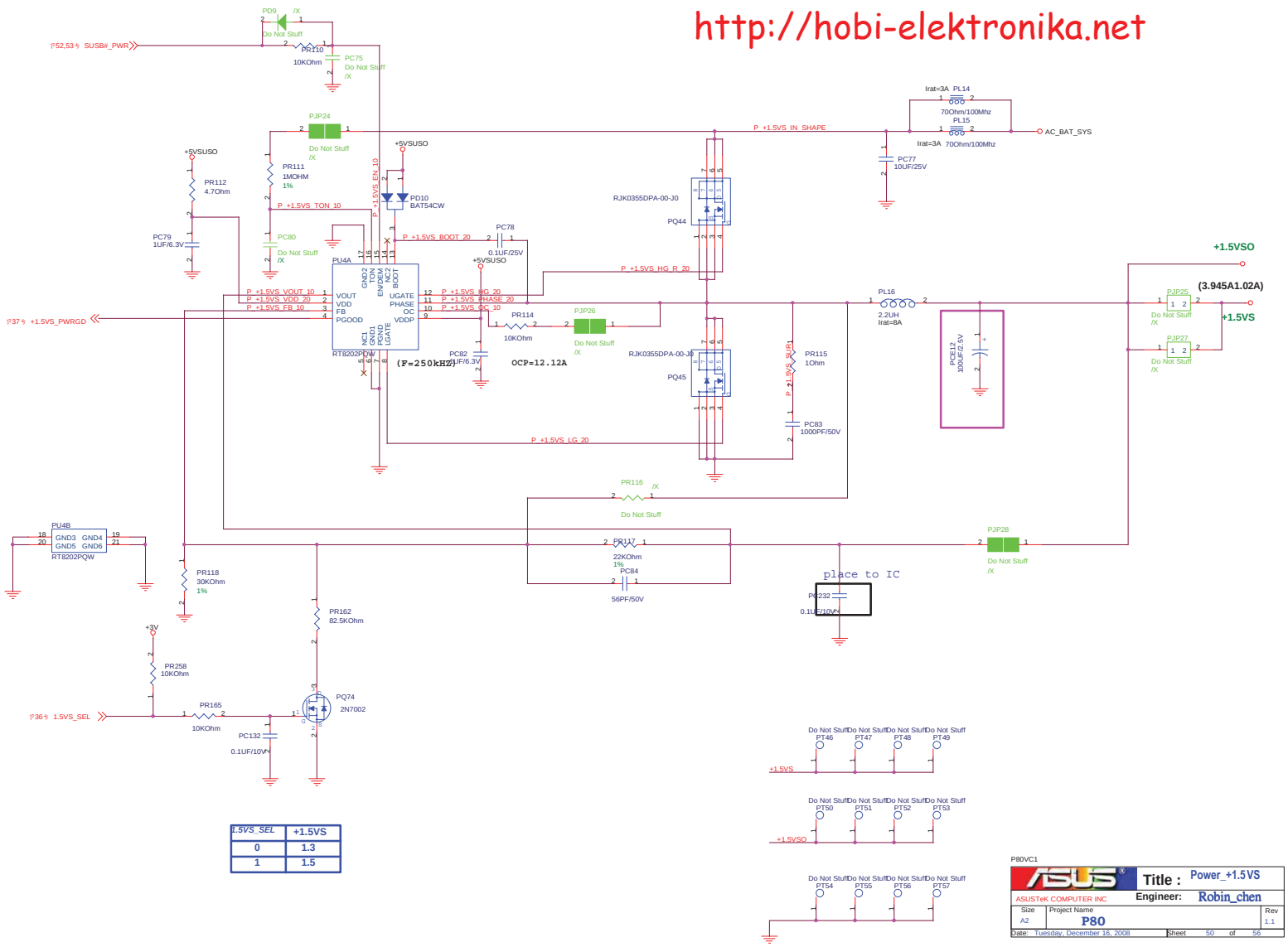
1. Frequency:
   1.2MHZ
2. Current limit
   4.5A(90W)
   3.16A(65W)

P80VC1

ASUSTeK COMPUTER INC. NB3 — Title : POWER_CHARGER — Engineer: Robin_chen

Size	Project Name	Rev
A2	P80A	1.1

Date: Tuesday, December 16, 2008 — Sheet 49 of 56



1.5VS_SEL	+1.5VS
0	1.3
1	1.5

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =0.368A
2. Ripple Current:
   Iripple=3A
3. Dynamic:
   Ipeak=3.503A
   ESR/2=4.5mohm
   V=14.18mV
4. Inductor Spec:
   Isat=14A
   Idc=8A
   DCR=18mOhm
5. MOSFET Spec:

H-side and L-side MOSFET:RJK0355
Rds(on)=11.8mOhm (Vgs=4.5V)
Icont=30 (T=25)
Ipeak=120 (Pause<10us)

Controller

1. Voltage & Current:
   +1.5V&3.5A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =250KHZ
3. OCP:
   Set PR7504=14KOhm
   Iocp=Rocp*20/Rds(on)=16.94A
4. Soft start time:
   Soft-Star duration is 2ms

P80VC1

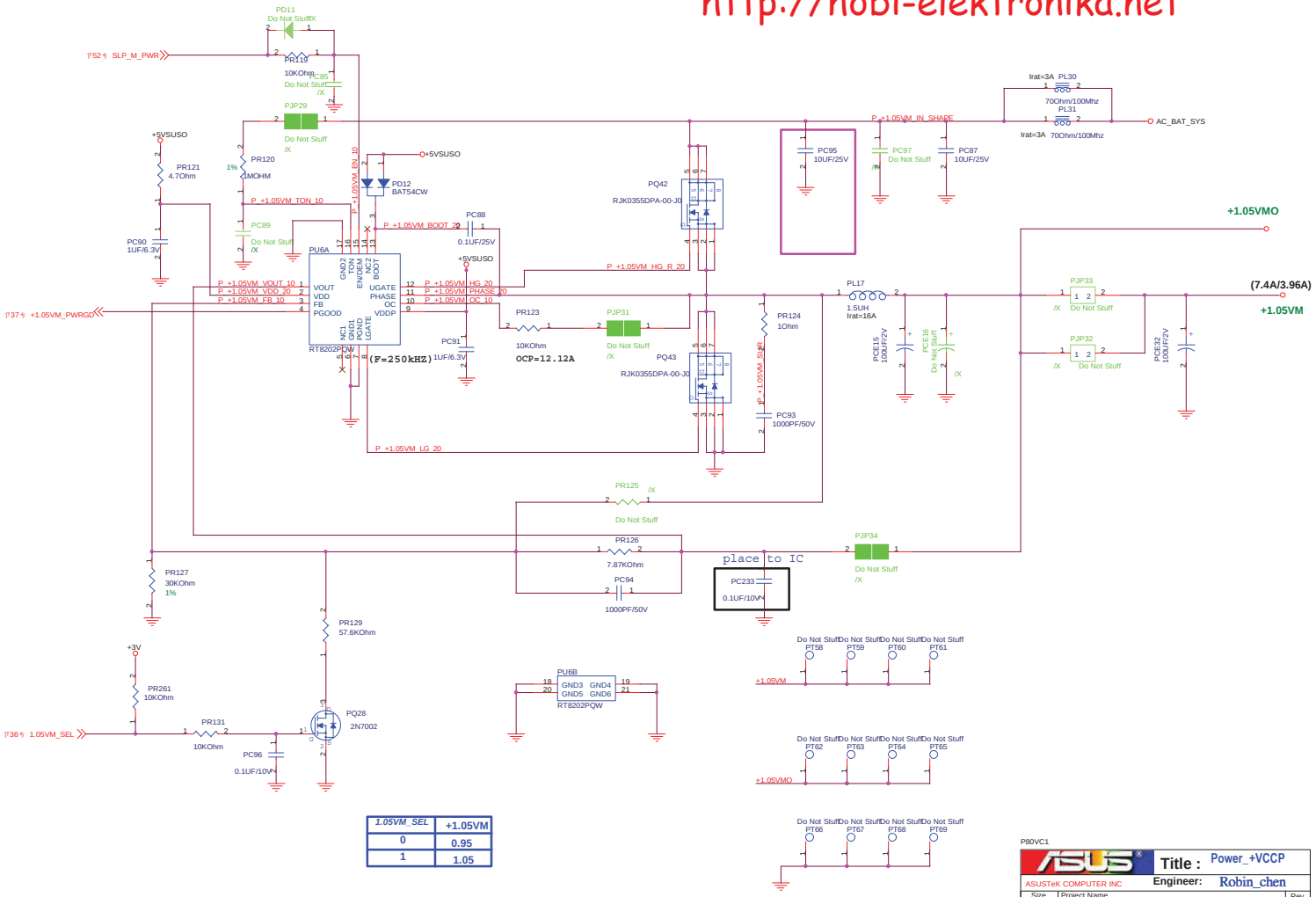
ASUSTeK COMPUTER INC

Title : Power_+1.5VS

Engineer: Robin_chen

Size	Project Name	Rev
A2	P80	1.1

Date: Tuesday, December 16, 2008 Sheet 50 of 56



1.05VM_SEL	+1.05VM
0	0.95
1	1.05

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.65A
2. Ripple Current:
   Iripple=3A
3. Dynamic:
   Ipeak=22.44A
   ESR/2=9mohm
   V=162mV
4. Inductor Spec:
   Isat=33A
   Idc=16A
   DCR=3.8mOhm
5. MOSFET Spec:

H-side and L-side MOSFET:RJK0355
Rds(on)=11.8mOhm (Vgs=4.5V)
Icont=30 (T=25)
Ipeak=120 (Pause<10us)

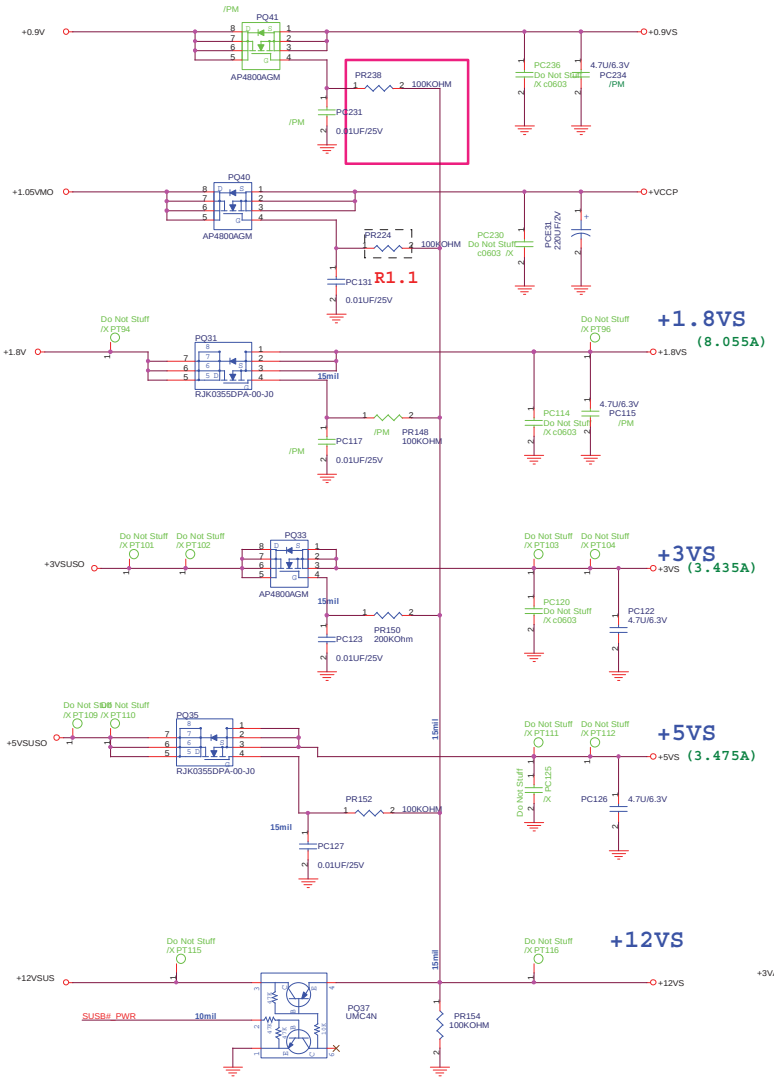
Controller

1. Voltage & Current:
   +1.05V&22.44A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =250KHZ
3. OCP:
   Set PR7504=14KOhm
   Iocp=Rocp*20/Rds(on)=16.94A
4. Soft start time:
   Soft-Star duration is 2ms

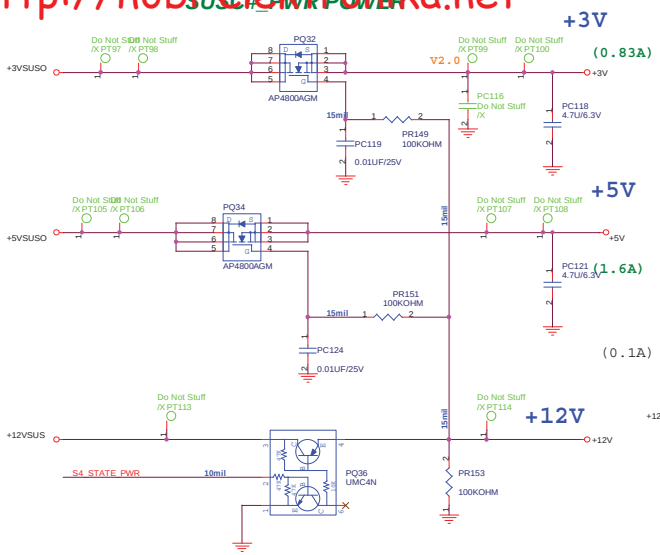
P80VC1

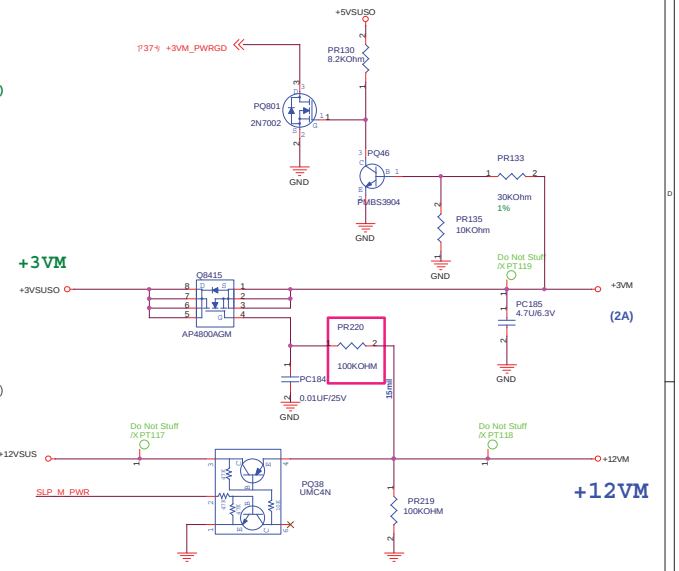
ASUSTeK COMPUTER INC	Title : Power_+VCCP		
	Engineer: Robin_chen		
Size: A2	Project Name: P80		Rev: 1.1
Date: Tuesday, December 16, 2008	Sheet 51 of 56		

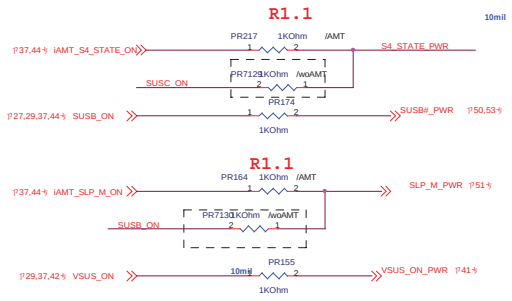
SUSB#_PWR POWER

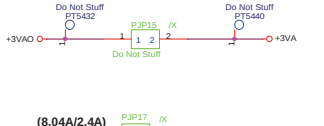


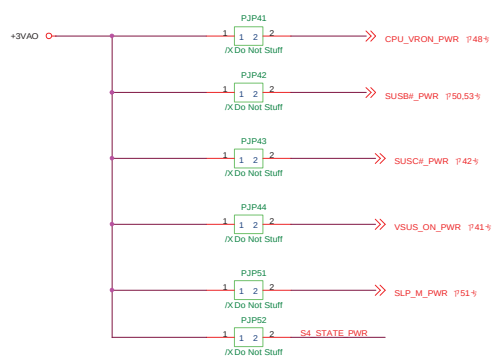
SUSC#_PWR POWER





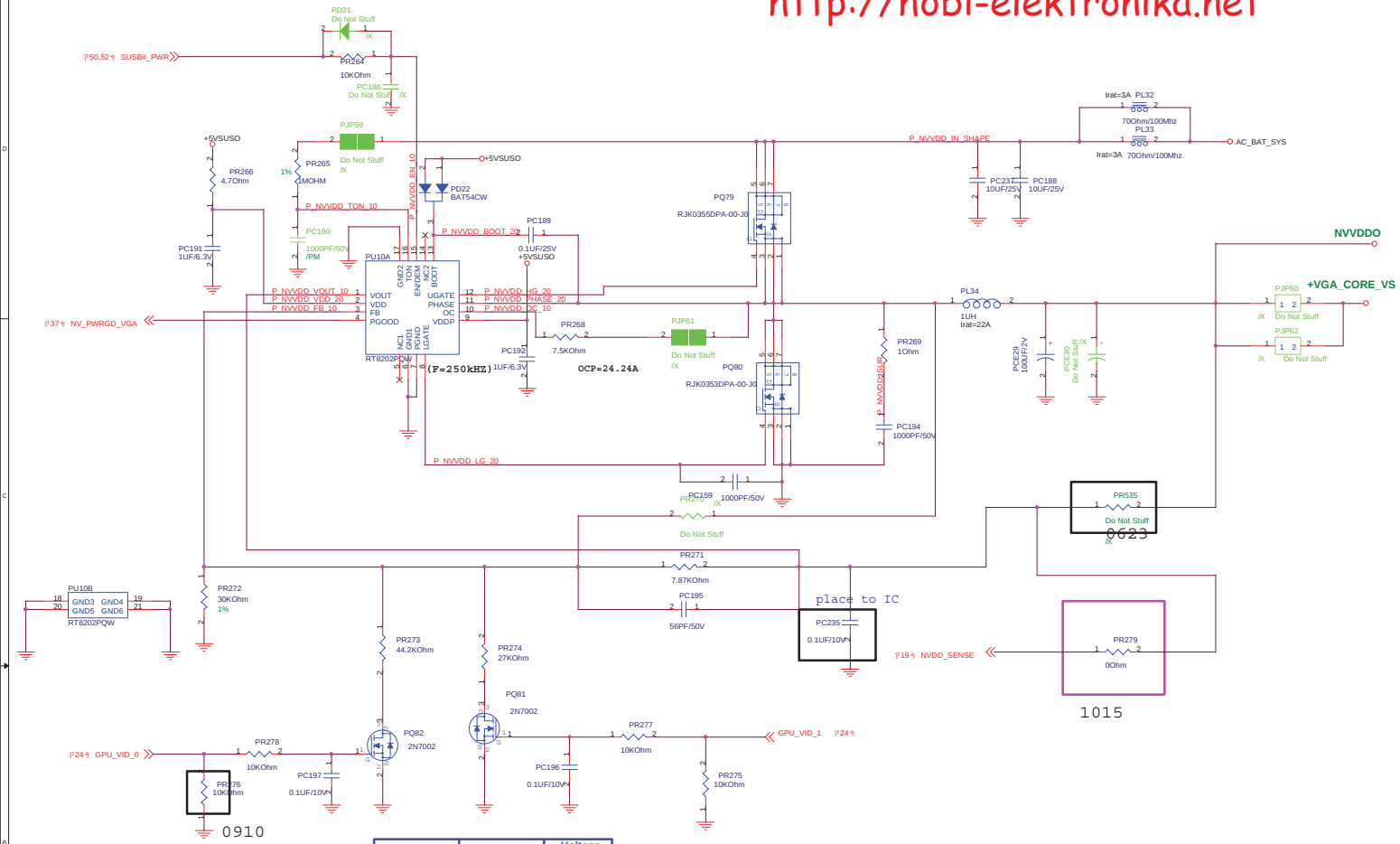






P80VC1

ASUSTek Computer INC.	Title : POWER_LOAD SWITCH	
	Engineer:	
Size: A2	Project Name: P80	Rev: 1.1
Date: Tuesday, December 16, 2008	Sheet 52 of 56	



GPU_VID_0	GPU_VID_1	Voltage
L	L	0.946V
H	L	1.00V
L	H	1.17V
H	H	X

Power stage

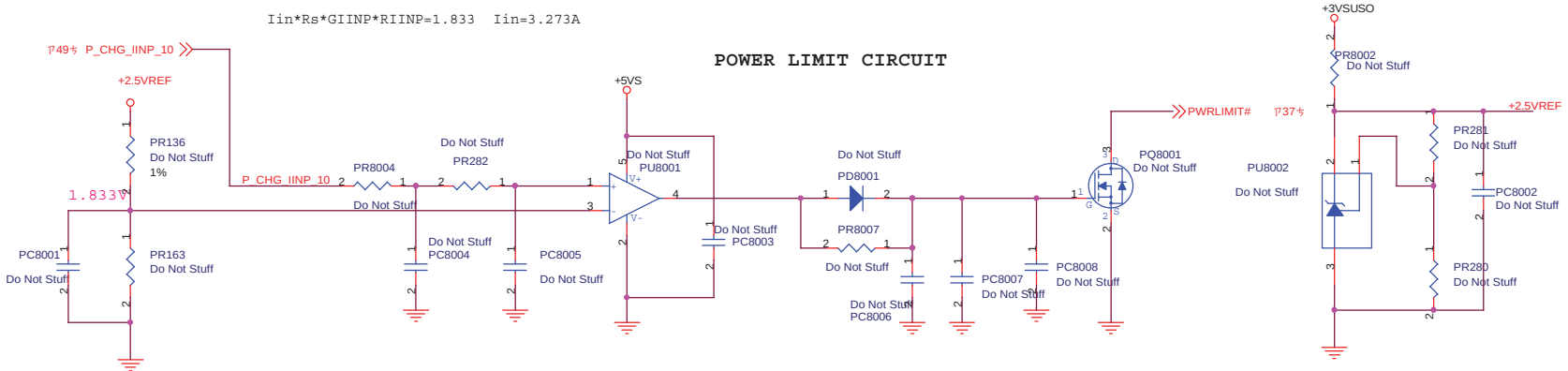
1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =2.3 A
2. Ripple Current:
   Iripple=3A
3. Dynamic:
   Ipeak=10.87A
   ESR/2=4.5mohm
   V=44mV
4. Inductor Spec:
   Isat=22A
   Idc=11A
   DCR=9mOhm
5. MOSFET Spec:
   H-side and L-side MOSFET:RJK0355/RJK0353
   Rds(on)=11.8/5.4mOhm (Vgs=10V)
   Icont=30/35A (T=25)
   Ipeak=120/140A (Pause<10us)

Controller

1. Voltage & Current:
   +VGA:0.94&10.08A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =250KHZ
3. OCP:
   Set PR7504=14KOhm
   Iocp=Rocp*20/Rds(on)=24A
4. Soft start time:
   Soft-Star duration is 2ms

P80VC1

ASUSTeK COMPUTER INC	Title : Power_+VGA	
	Engineer: robin_chen	
Size: A2	Project Name: P80	Rev: 1.1
Date: Tuesday, December 16, 2008	Sheet 53 of 56	



P80VC1

ASUSTek Computer INC.	Title : Power_Charger	
	Engineer: Robin_chen	
Size: A3	Project Name: P80	Rev: R1.1
Date: Tuesday, December 16, 2008	Sheet 54 of 80	