PCB P/N AND DESCRIPTION

PCB ED5 MB(8L,309X218, REVA)
P/N: DA0ED5MB8A8

PCB ED5 MB(8L,309X218,REVB)
P/N: DA0ED5MB8B6

PCB ED5 USB/B(8L, 47.5X16.8, REVA)
P/N: DA0ED5SB8A5

PCB ED5 USB/B(8L,47.5X16.8,REVB)
P/N: DA0ED5SB8B3

ED5

SATA
ED5 SATA ASSY P/N
ED5 MB S/S ASSY P/N: 51ED5SS0018
ED5 MB C/S ASSY P/N: 41ED5CS0015
ED5 MB ASSY P/N: 31ED5MB0012

W/O ANT
ED5 USB/B S/S ASSY P/N: 4NED5SS0011
ED5 USB/B ASSY P/N: 3NED5UB0011

PATA
ED5 ASSY P/N
ED5 MB S/S ASSY P/N: 51ED5SS0000
ED5 MB C/S ASSY P/N: 41ED5CS0007
ED5 MB ASSY P/N: 31ED5MB0004

ANT
ED5 USB/B S/S ASSY P/N: 4NED5SS0002
ED5 USB/B ASSY P/N: 3NED5UB0003

VCC_CORE → **CPU VR** PG 30

+1.2V, +VCCP → **+1.2V +VCCP** PG 31

+1.8VSUS, +1.8V, SMDDR_VTERM → **+1.8VSUS SMDDR VTERM** PG 32

+3VPCU, +3V_S5, +3VSUS, +5VSUS, +5V, +12V → **3V/5V** PG 33

VIN → **CHARGER** PG 34

DDRII-SODIMM1 PG 7,8
DDRII-SODIMM2 PG 7,8
533/ 667 MHZ DDR II

AMD S1
Turion 64 Rev.F Dual-Core/ Sempron Rev.F Single-Core
Dual-Core 35W / Single-Core 25W
(638 S1g1 socket)
PG 3,4,5,6

HOST 133/166MHz
PCIE 100MHz
VGA 96MHz
USB 48MHz
REF 14MHz

CLOCK GENERATOR
ICS951462
PG 13

HT_LINK

Panel Connector PG 20 — LVDS
S-Video PG 20 — TVOUT
VGA PG 20 — VGA

RS485
465 FCBGA
PG 9,10,11,12

PCI-E, 1X → **Express Card** PCIE1 & USB4 NEW CARD PG 24

PG 19 PCI-E, 1X → **Mini PCI-E Card (WLAN)** PCIE2 PCI Express Mini Card PG 19

PCI-E, 1X → **Mini PCI-E Card (TV)** PCIE3 & USB5 PCI Express Mini Card PG 19

WIRE

PCI-E, 1X → **LAN RTL8111B-GR** PCIE0 PG 23 — **Magnetics** — **RJ45**

A_LINK

SATA - HDD PG 21 — ***SATA0***
PATA - HDD PG 21 — ***PATA 100***
Internal ODD CD-ROM PG 21

SB460
549 BGA
PG 14,15,16,17

USB2.0 (P0~P7)

Bluetooth USB7 PG 22

B/B CN. USB2 & USB3 PG 22

USB2.0 I/O Ports USB0 & USB1 PG 22

DSC USB I/F USB6 PG 22

ANTENNA JACK

USB2.0 I/O

USB DAUGHTERBOARD

Azalia

Azalia Audio PG 26

Amplifier MAX9755A PG 27

Azalia MDC PG 26

MIC. PG 27
INT. S.P. PG 27
H.P PG 27
MODEM RJ 11 PG 23

LPC

KBC
NS97551
PG 28

X-Bus

K/B CONN. PG 29
Touch Pad PG 29
Flash ROM PG 28

SWITCH LED PG 29

PCI Bus 33MHz

TI PCI8402
AD17
REQ3#, GNT3#
INTE#, INTG#, INTH#
PG 24,25

MINI PCI CN.
AD20
REQ2#, GNT2#
INTF#, INTG#
DEBUG PURPOSE ONLY PG 18

Card Reader PG 25
IEEE1394 CN. PG 25

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A
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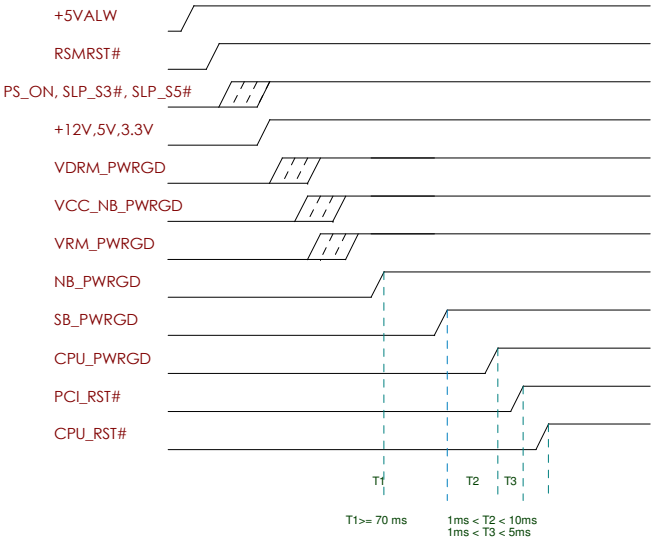
TABLE OF CONTENTS

	POWER	VOLTAGE	ACTIVE SCOPE	ROUTING	PAGE
SYSTEM	+12V	+12V	OFF IN S3-S5	PLANE	41
	-12V	-12V	OFF IN S3-S5	TRACE 20 MIL	41
	+5V	+5V	OFF IN S3-S5	PLANE	41
	+3.3V	+3.3V	OFF IN S3-S5	PLANE	41
	+5VALW	+5V	S0-S5	PLANE/ 50 MIL	41
	+3.3VALW	+3.3V	S0-S5	TRACE 30 MIL	41
	+1.8VALW	+2.5V	S0-S5	TRACE 30 MIL	21
	+5V_DUAL	+5V	S0-S5	PLANE/ 100 MIL	41
	+3.3V_DUAL	+3.3V	S0-S5	PLANE/ 50 MIL	41
CPU	VCCCORE	VID[0..6]	OFF IN S3-S5	PLANE+COPER	37
	VCCP	+1.05V	OFF IN S3-S5	PLANE+COPER	38
	VCCA	+1.5V	OFF IN S3-S5	TRACE 20 MIL	38
RC485 NB	VCC_NB	+1.2V/1.0V	OFF IN S3-S5	PLANE+COPER	39
	VDD_CPU	+1.05V	OFF IN S3-S5	PLANE+COPER	38
	VDD_MEM	+1.8V	S0-S3	PLANE+COPER	40
	VDD18	+1.8V	OFF IN S3-S5	TRACE 20 MIL	12
	VDDA18	+1.8V	OFF IN S3-S5	COPPER	12
	VDDA12	+1.2V	OFF IN S3-S5	PLANE+COPPER	12
	AVDD	+3.3V	OFF IN S3-S5	TRACE 20 MIL	11
	AVDDQ	+1.8V	OFF IN S3-S5	TRACE 20 MIL	11
	PLVDD	+1.8V	OFF IN S3-S5	TRACE 20 MIL	11
	LPVDD	+1.8V	OFF IN S3-S5	TRACE 20 MIL	11
	LVDDR	+1.8V	OFF IN S3-S5	TRACE 30 MIL	11
	VDDR3	+3.3V	OFF IN S3-S5	TRACE 30 MIL	11
	VTT_DDR	+0.9V	OFF IN S3-S5	COPPER	40
	VDD_CLK	+3.3V	OFF IN S3-S5	COPPER	14
SB460 SB	+3.3V_SB	+3.3V	OFF IN S3-S5	PLANE	21
	+1.8V_SB	+1.8V	OFF IN S3-S5	PLANE	21
	+3.3VALW_SB	+3.3V	S0-S5	PLANE	21
	+1.8VALW_SB	+1.8V	S0-S5	PLANE	21
	+1.8V_SUB_PHY	+1.8V	S0-S5	TRACE 30 MIL	21
	AVDD_CK	+1.8V	OFF IN S3-S5	TRACE 10 MIL	21
	V5_REF	+5V	OFF IN S3-S5	TRACE 10 MIL	21
	CPU-PWR	+1.05V	OFF IN S3-S5	TRACE 20 MIL	21
	PCIE_PVDD	+1.8V	OFF IN S3-S5	TRACE 20 MIL	18
	PCIE_VDDR	+1.8V	OFF IN S3-S5	PLANE+COPER	18
	+1.8V_ATA	+1.8V	OFF IN S3-S5	PLANE	20
	PLLVDD_ATA	+1.8V	OFF IN S3-S5	TRACE 20 MIL	20
	XTLVDD_ATA	+1.8V	OFF IN S3-S5	TRACE 20 MIL	20
	AVDD_USB_TX	+1.8V	S0-S5	PLANE+COPER	19
	AVDD_USB_RX	+1.8V	S0-S5	PLANE+COPER	19
	+3.3V_AVDDC	+3.3V	S0-S5	TRACE 20 MIL	19
	V_BAT	+3.0V	--	TRACE 10 MIL	18

BONEFISH POWER UP SEQUENCE



PROJECT : ED5
Quanta Computer Inc.

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	BLOCK DIAGRAM	1A
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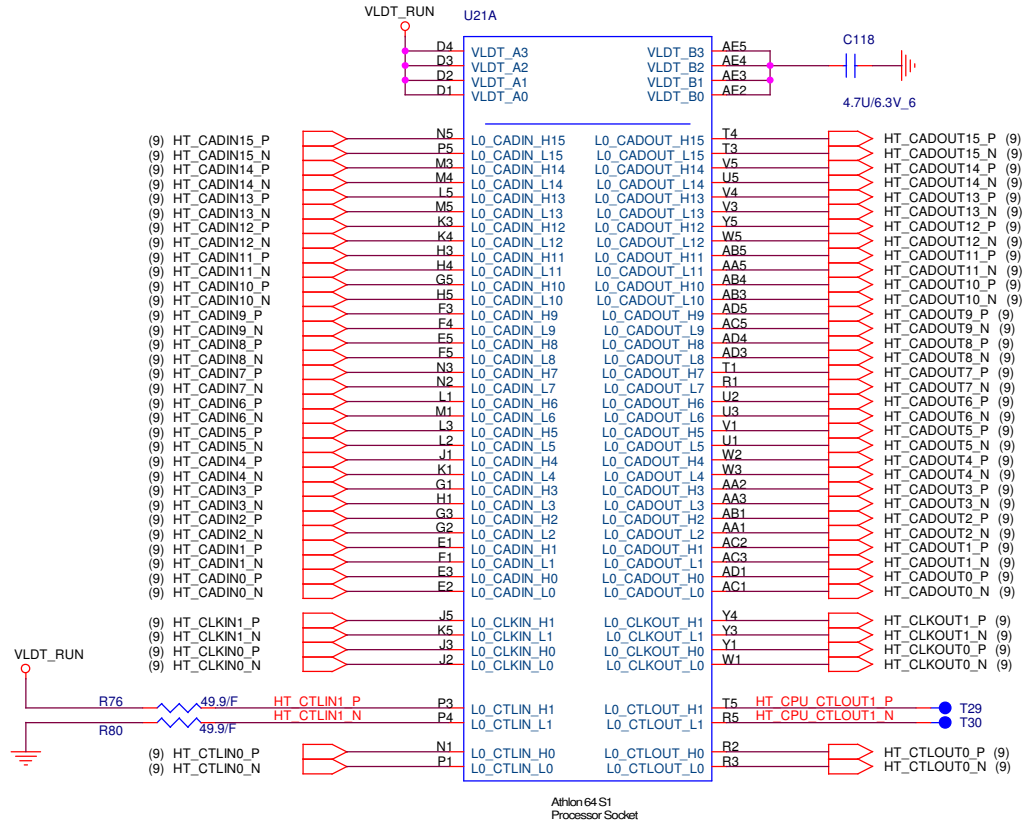
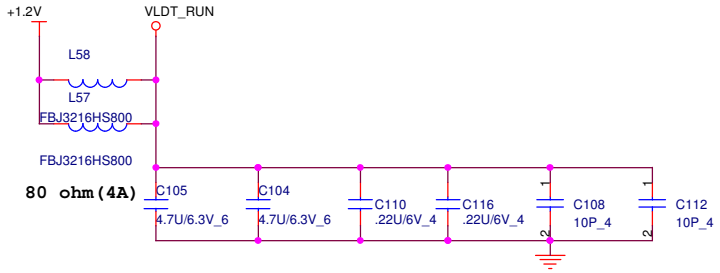
PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE





LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

PROJECT : ED5
Quanta Computer Inc.

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	ATHLON64 HT I/F	1A
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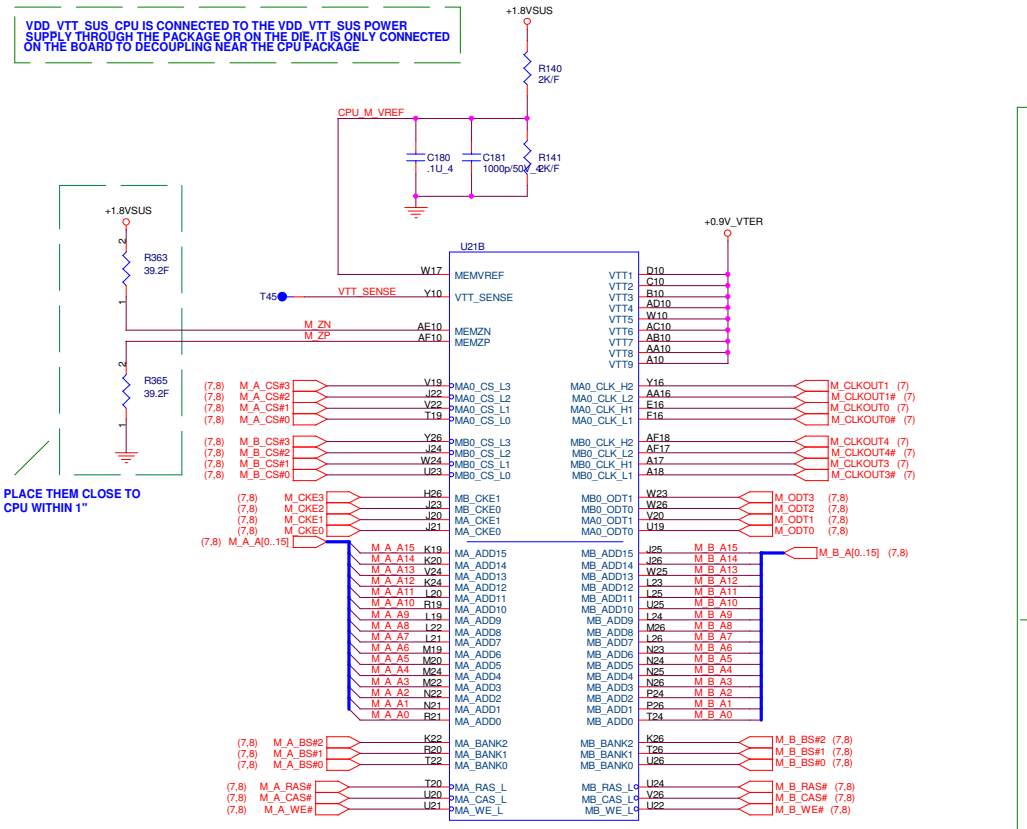
Processor DDR2 Memory Interface

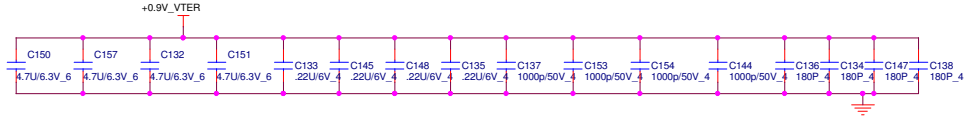
VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

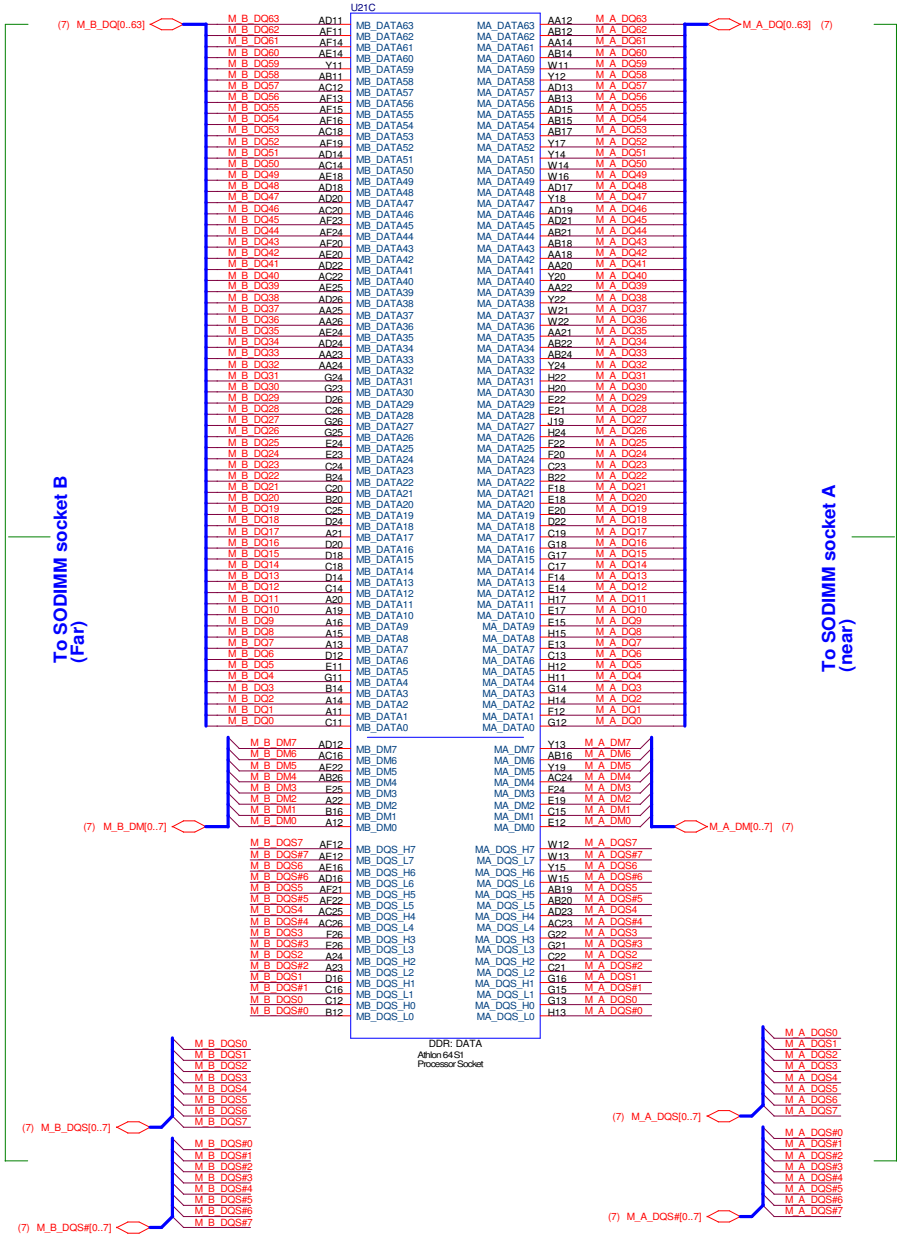
PLACE THEM CLOSE TO CPU WITHIN 1"



DDR II: CMD/CTRL/CLK

Athlon 64 S1 Processor Socket





DDR: DATA

Athlon 64 S1 Processor Socket

PROJECT : ED5

Quanta Computer Inc.

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	ATHLON64 DDRII MEMORY I/F	1A
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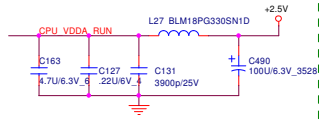
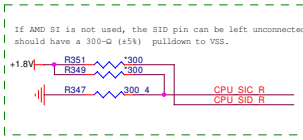
ATHLON Control and Debug

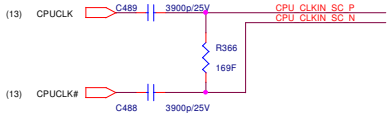
LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

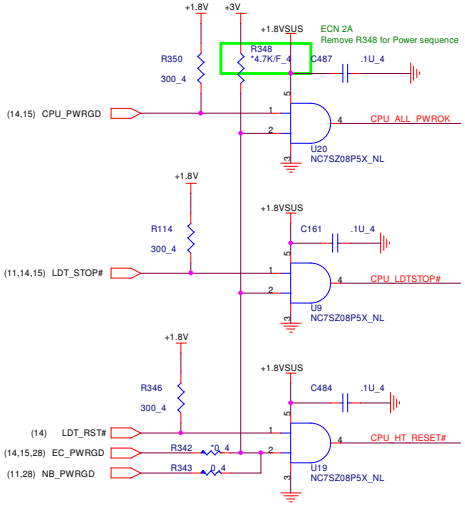
CPU_VDDA_RUN



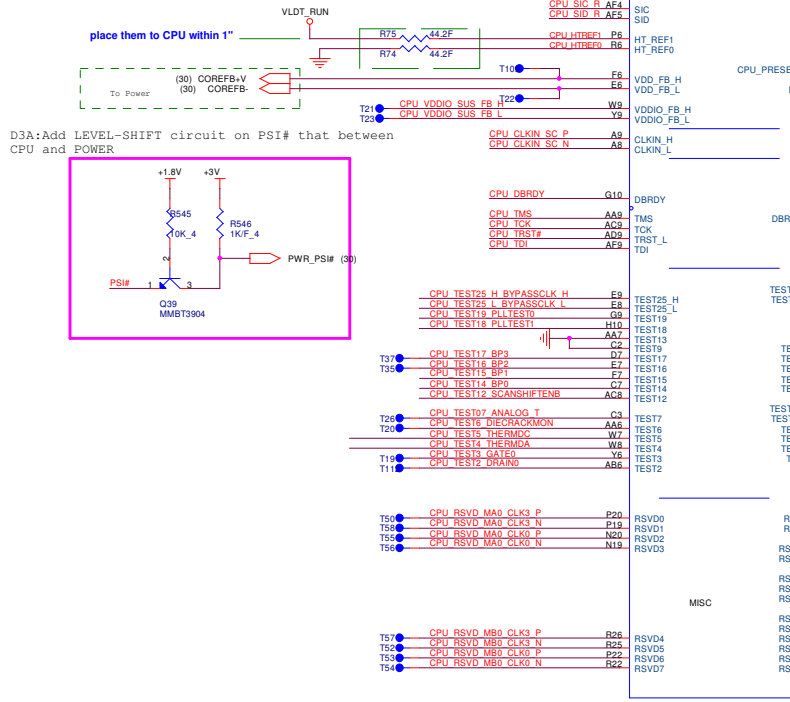
If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.



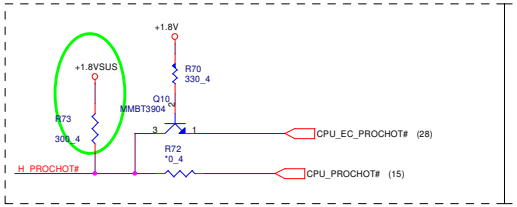


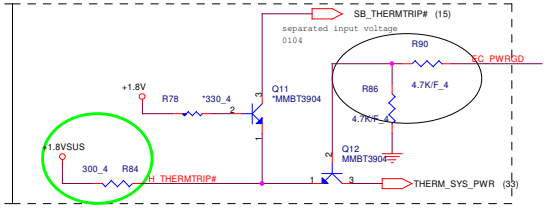


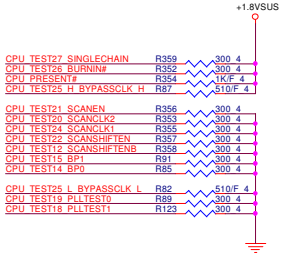
D3A:Add LEVEL-SHIFT circuit on PSI# that between CPU and POWER



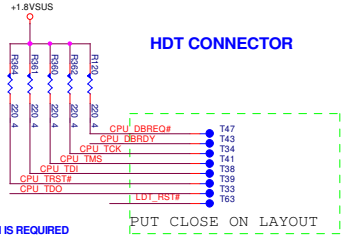
PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports "skipmode, or diode emulation mode". PSI_L is asserted by the processor during the C3 and S1 states.





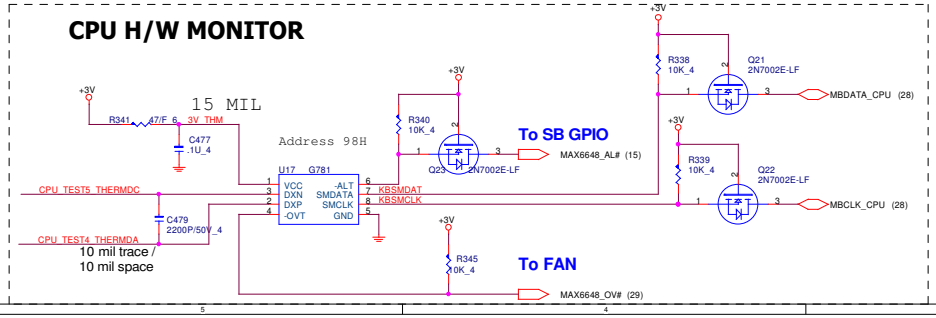


IF no use which Net need pull-up or down



NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

CPU H/W MONITOR



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Quanta Computer Inc.

Size	Document Number	Rev
	ATHLON64 CTRL & DEBUG	2A
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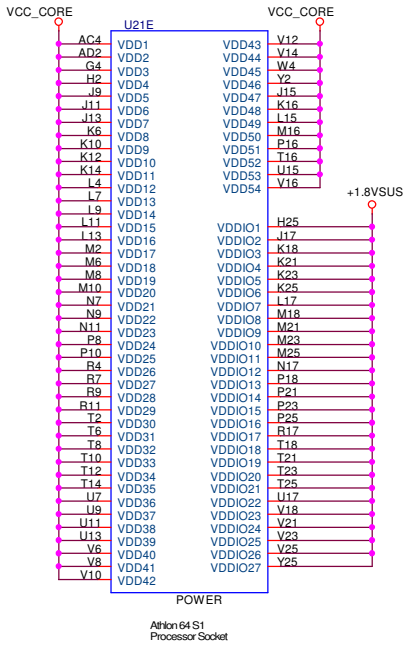
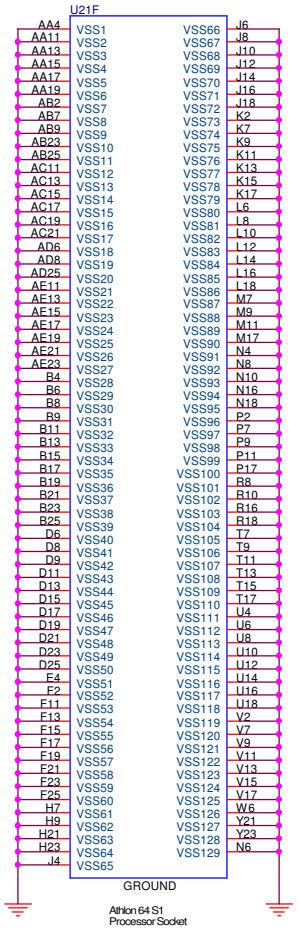
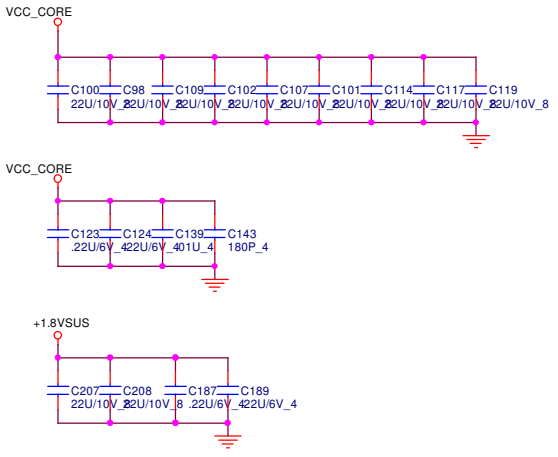
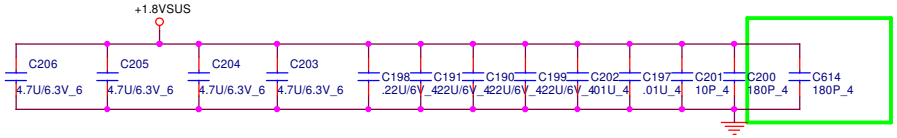


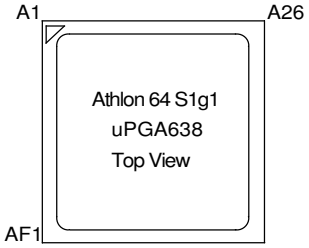


BOTTOMSIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE





PROCESSOR POWER AND GROUND

PROJECT : ED5
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Size	Document Number	Rev
	ATHLON64 PWR & GND	1A
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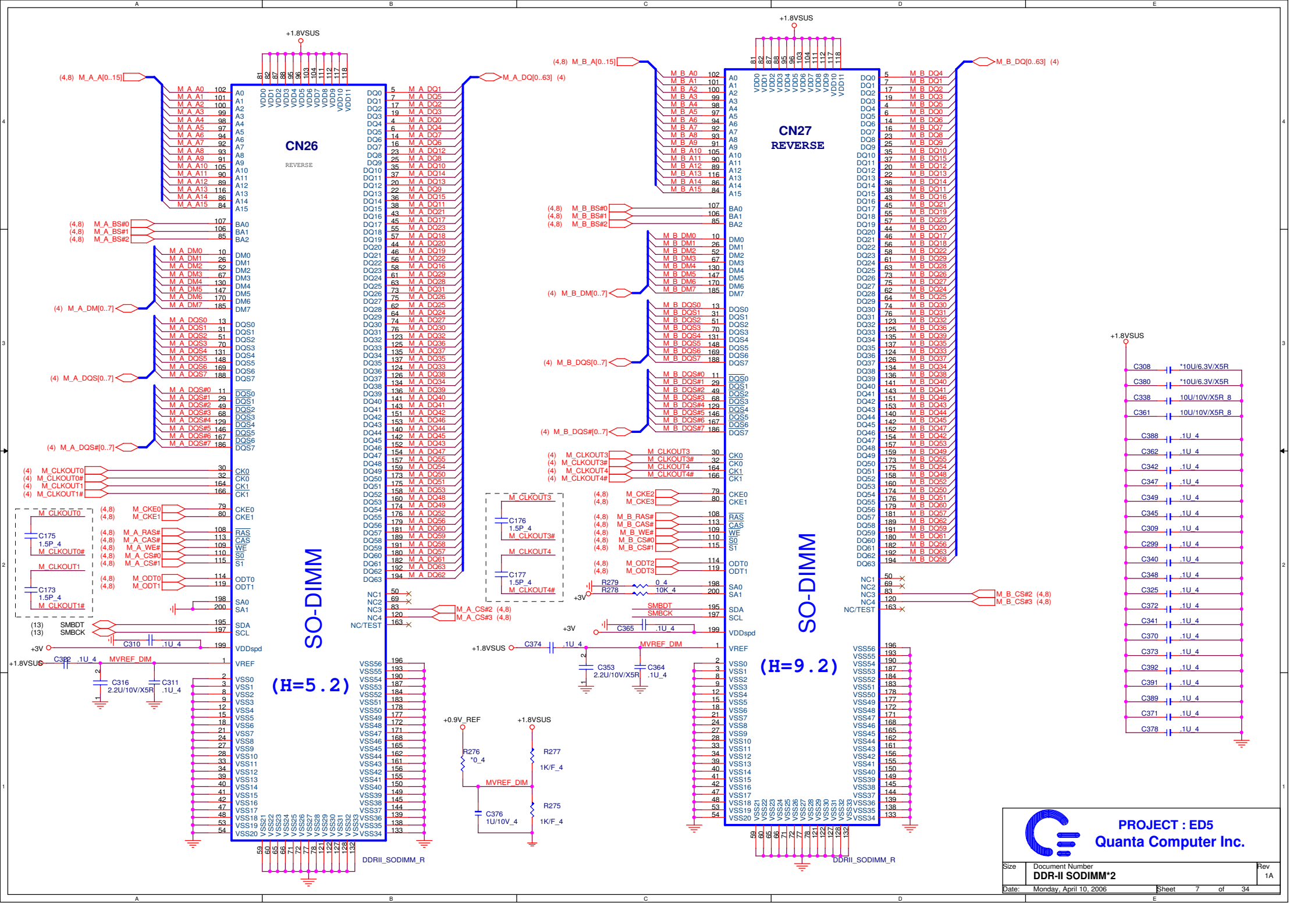
CN26
REVERSE
SO-DIMM
(H=5.2)
CN27
REVERSE
SO-DIMM
(H=9.2)
+1.8VSUS
+3V
+0.9V_REF
M_A_A[0..15]
M_A_BS#0
M_A_BS#1
M_A_BS#2
M_A_DM[0..7]
M_A_DQS[0..7]
M_A_DQS#[0..7]
M_A_DQ[0..63]
M_CLKOUT0
M_CLKOUT0#
M_CLKOUT1
M_CLKOUT1#
M_CKE0
M_CKE1
M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_CS#0
M_A_CS#1
M_ODT0
M_ODT1
SMBDT
SMBCK
MVREF_DIM
M_A_CS#2 (4,8)
M_A_CS#3 (4,8)
M_B_A[0..15]
M_B_BS#0
M_B_BS#1
M_B_BS#2
M_B_DM[0..7]
M_B_DQS[0..7]
M_B_DQS#[0..7]
M_B_DQ[0..63]
M_CLKOUT3
M_CLKOUT3#
M_CLKOUT4
M_CLKOUT4#
M_CKE2
M_CKE3
M_B_RAS#
M_B_CAS#
M_B_WE#
M_B_CS#0
M_B_CS#1
M_ODT2
M_ODT3
M_B_CS#2 (4,8)
M_B_CS#3 (4,8)
C310 .1U_4
C309 .1U_4
C316 2.2U/10V/X5R
C311 .1U_4
C374 .1U_4
C353 2.2U/10V/X5R
C364 .1U_4
C365 .1U_4
C376 1U/10V_4
R276 *0_4
R277 1K/F_4
R275 1K/F_4
R279 0_4
R278 10K_4
C308 *10U/6.3V/X5R
C380 *10U/6.3V/X5R
C338 10U/10V/X5R_8
C361 10U/10V/X5R_8
C388 .1U_4
C362 .1U_4
C342 .1U_4
C347 .1U_4
C349 .1U_4
C345 .1U_4
C299 .1U_4
C340 .1U_4
C348 .1U_4
C325 .1U_4
C372 .1U_4
C341 .1U_4
C370 .1U_4
C373 .1U_4
C392 .1U_4
C391 .1U_4
C389 .1U_4
C371 .1U_4
C378 .1U_4
DDRII_SODIMM_R
PROJECT : ED5
Quanta Computer Inc.
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Rev
1A
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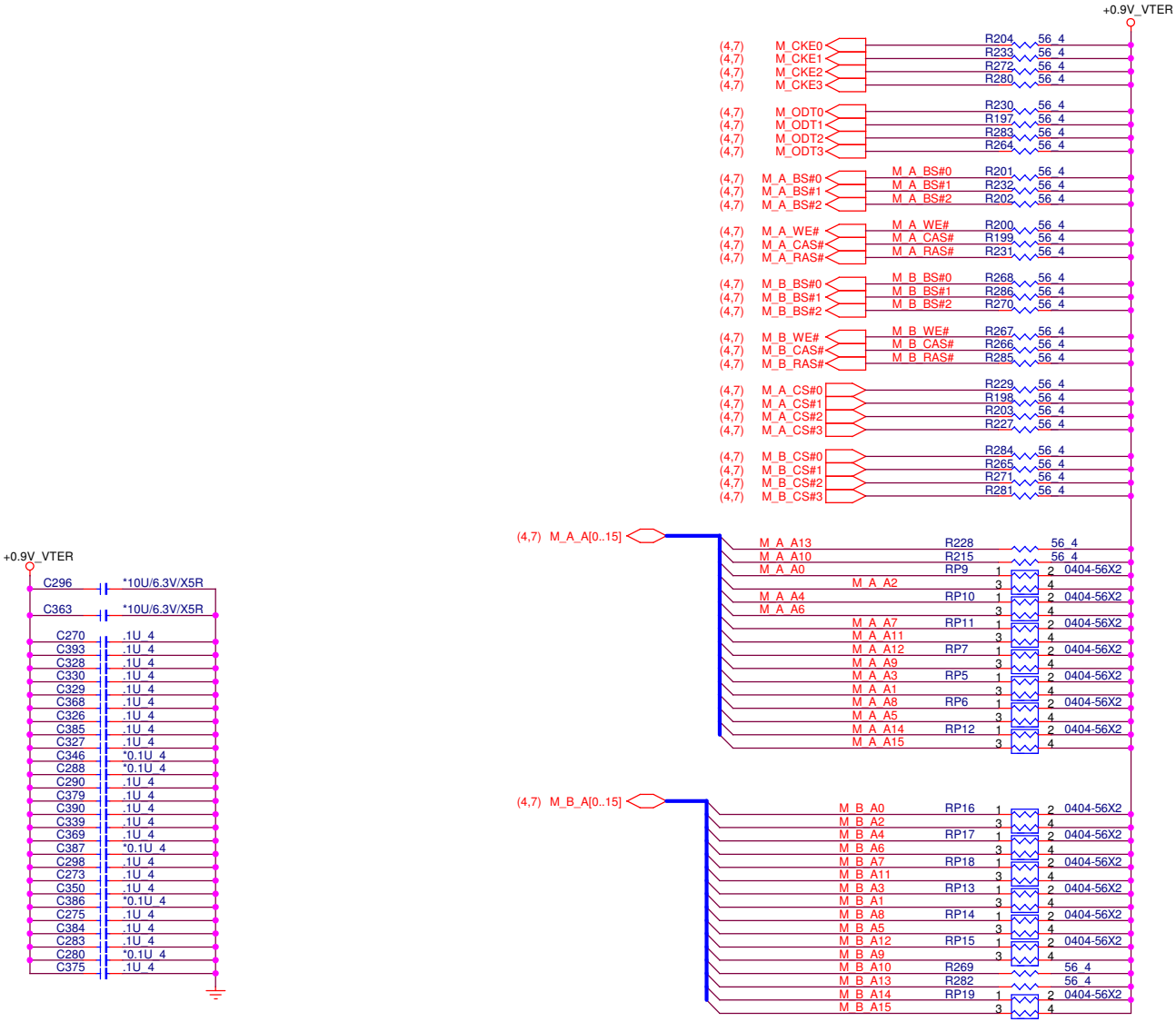

PROJECT : ED5

Quanta Computer Inc.

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	DDR-II TERMINATION	1A
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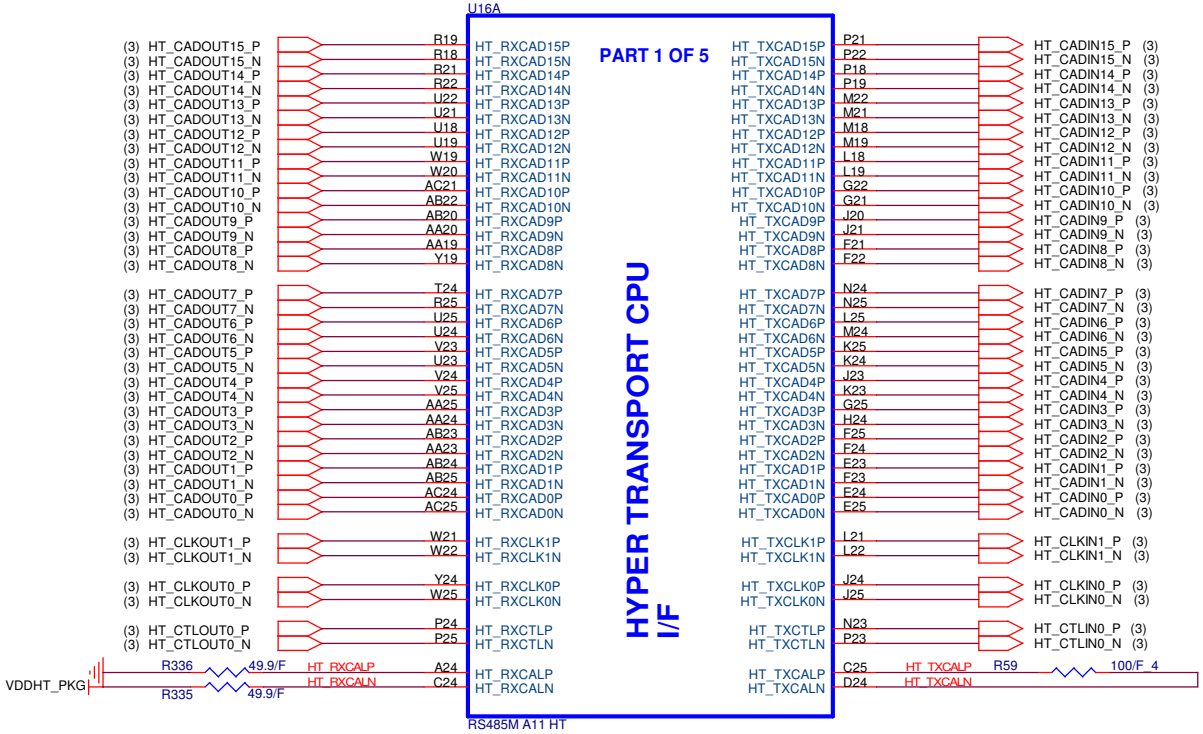

PROJECT : ED5

Quanta Computer Inc.

Size	Document Number	Rev
	RS485-HT LINK0 I/F	1A
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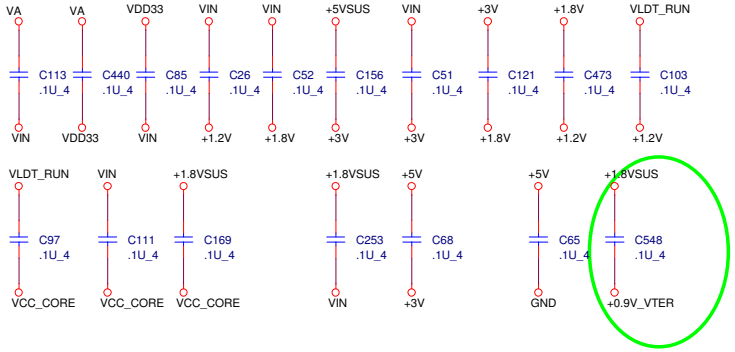

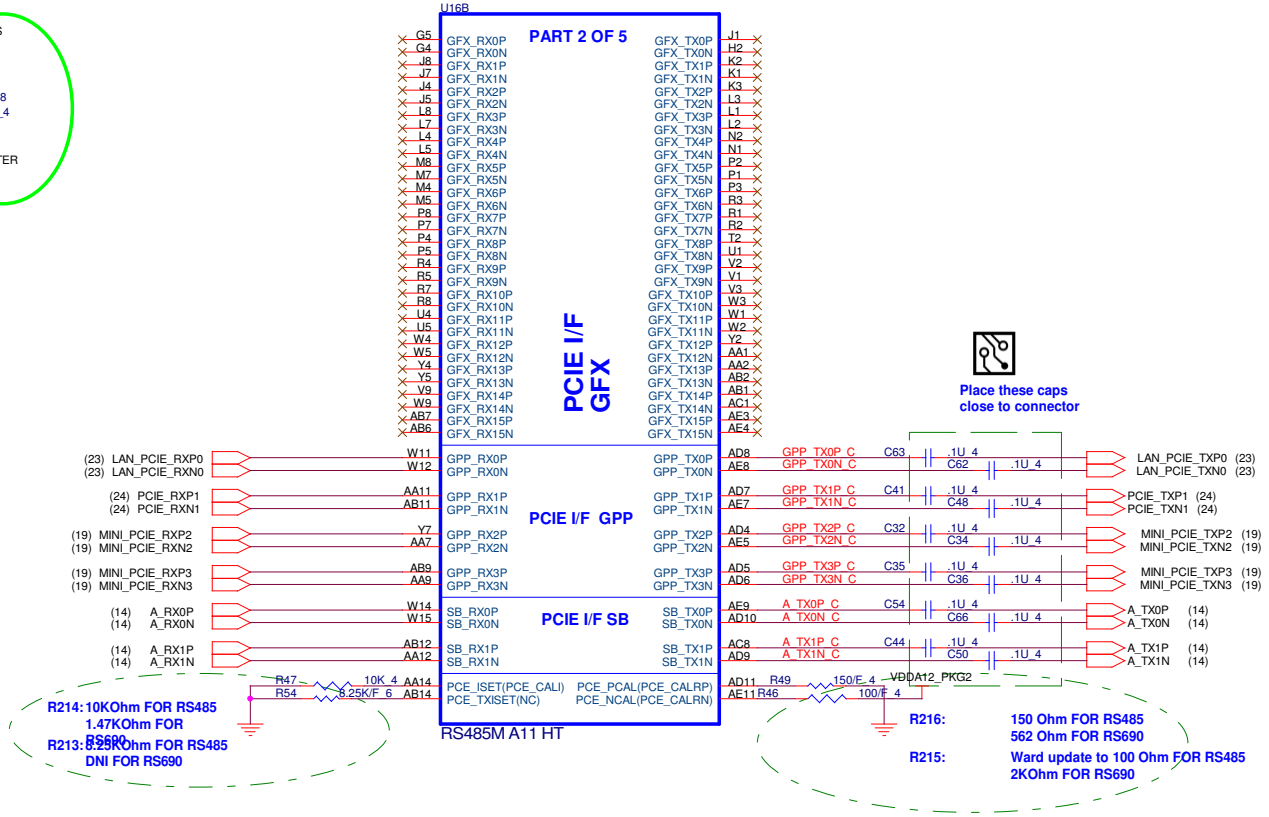

PROJECT : ED5
Quanta Computer Inc.

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	RS485-PCIE LINK I/F	1A
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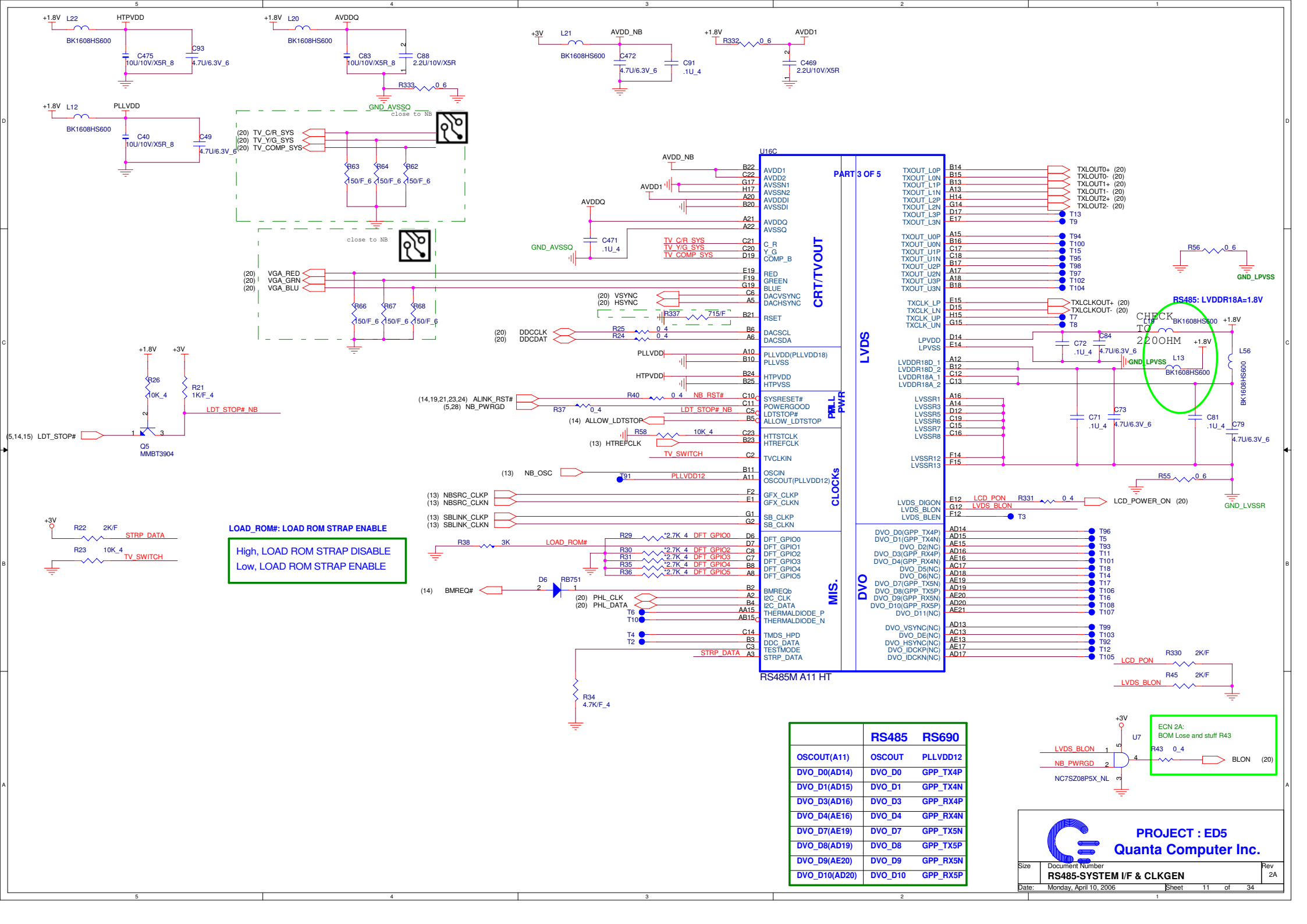

	RS485	RS690
OSCOUT(A11)	OSCOUT	PLLVDD12
DVO_D0(AD14)	DVO_D0	GPP_TX4P
DVO_D1(AD15)	DVO_D1	GPP_TX4N
DVO_D3(AD16)	DVO_D3	GPP_RX4P
DVO_D4(AE16)	DVO_D4	GPP_RX4N
DVO_D7(AE19)	DVO_D7	GPP_TX5N
DVO_D8(AD19)	DVO_D8	GPP_TX5P
DVO_D9(AE20)	DVO_D9	GPP_RX5N
DVO_D10(AD20)	DVO_D10	GPP_RX5P

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Quanta Computer Inc.

Size	Document Number	Rev
	RS485-SYSTEM I/F & CLKGEN	2A
Date: Monday, April 10, 2006	Sheet 11 of 34	

SUGGEST REMOVE L11 BEAD SAME AS CPU
1.2 PLAN FSB UNDER THIS PLAN

VLDT_RUN
80 ohm(4A)

U16E
RS485M A11 HT
PAR 5 OF 5
GROUND

+1.2V
80 ohm(4A)
L54
FBJ3216HS800

VDDA12
C46 1U/10V_4
C45 1U/10V_4
C39 1U/10V_4
C447 10U/10V/X5R_8
C448 10U/10V/X5R_8
C449 100U/6.3V_3528

VCC_NB
D3A:Remove Jump
+1.2V
C466 10U/10V/X5R_8
C460 10U/10V/X5R_8
C470 1U/10V_4
C75 1U/10V_4
C55 1U/10V_4
C70 1U/10V_4
C458 100U/6.3V_3528
C82 1U/10V_4
C74 1U/10V_4
C60 1U/10V_4

U16D
PART 4 OF 5
POWER
RS485M A11 HT

C95 10U/10V/X5R_8
C96 10U/10V/X5R_8
C90 1U/10V_4
C89 1U/10V_4
C92 1U/10V_4
C80 1U/10V_4
C87 1U/10V_4

+3V
D25 SW1010C
D24 SW1010C
D23 SW1010C

+1.8V
L18 TI201209G121
VDD18
C67 2.2U/10V/X5R
C467 2.2U/10V/X5R

RS485: VDDA18=1.8V
+1.8V
L55 BLM18PG330SN1D
33 ohm (3000mA)
VDDA18
C450 10U/10V/X5R_8
C443 10U/10V/X5R_8
C43 1U/10V_4
C445 1U/10V_4
C27 1U/10V_4
C31 1U/10V_4
C444 1U/10V_4

+3V
L11 TI201209G121
VDDR3
C53 4.7U/6.3V_6

+1.8V
L17 TI201209G121
VDDDVO
C78 1U/10V_4
C77 1U/10V_4
C76 1U/10V_4

VDDA12
R41 0_6
VDDPLL
RS485: 0 Ohm RESISTOR
C42 4.7U/6.3V_6
C38 1U/10V_4

VDDA12_PKG1
C446 10U/10V/X5R_8

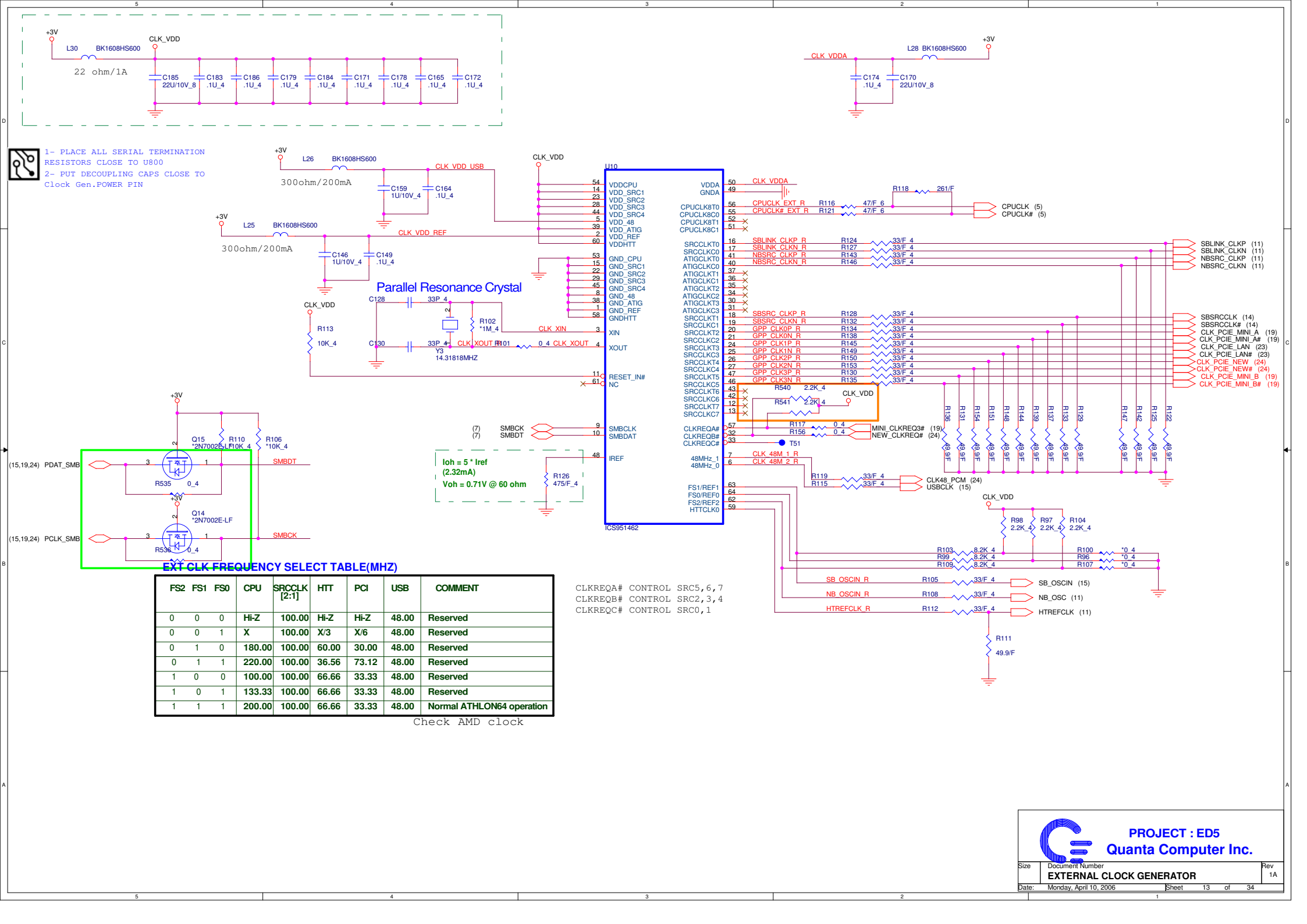
VDDHT_PKG
VDDA12_PKG1
VDDA12_PKG2

NB RS485 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	RS485-POWER	1A
Date: Monday, April 10, 2006	Sheet 12 of 34	

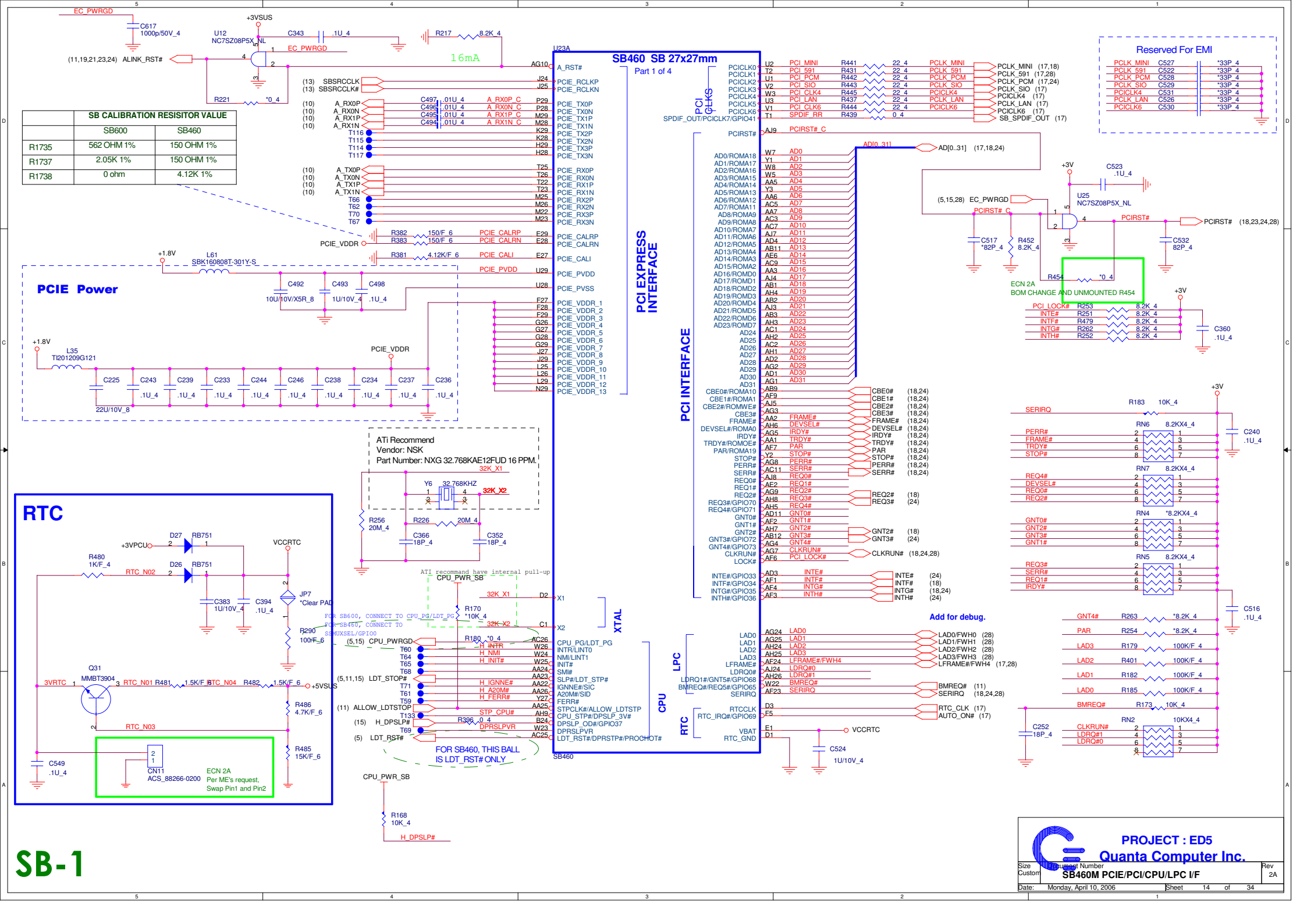


EXT CLK FREQUENCY SELECT TABLE(MHZ)

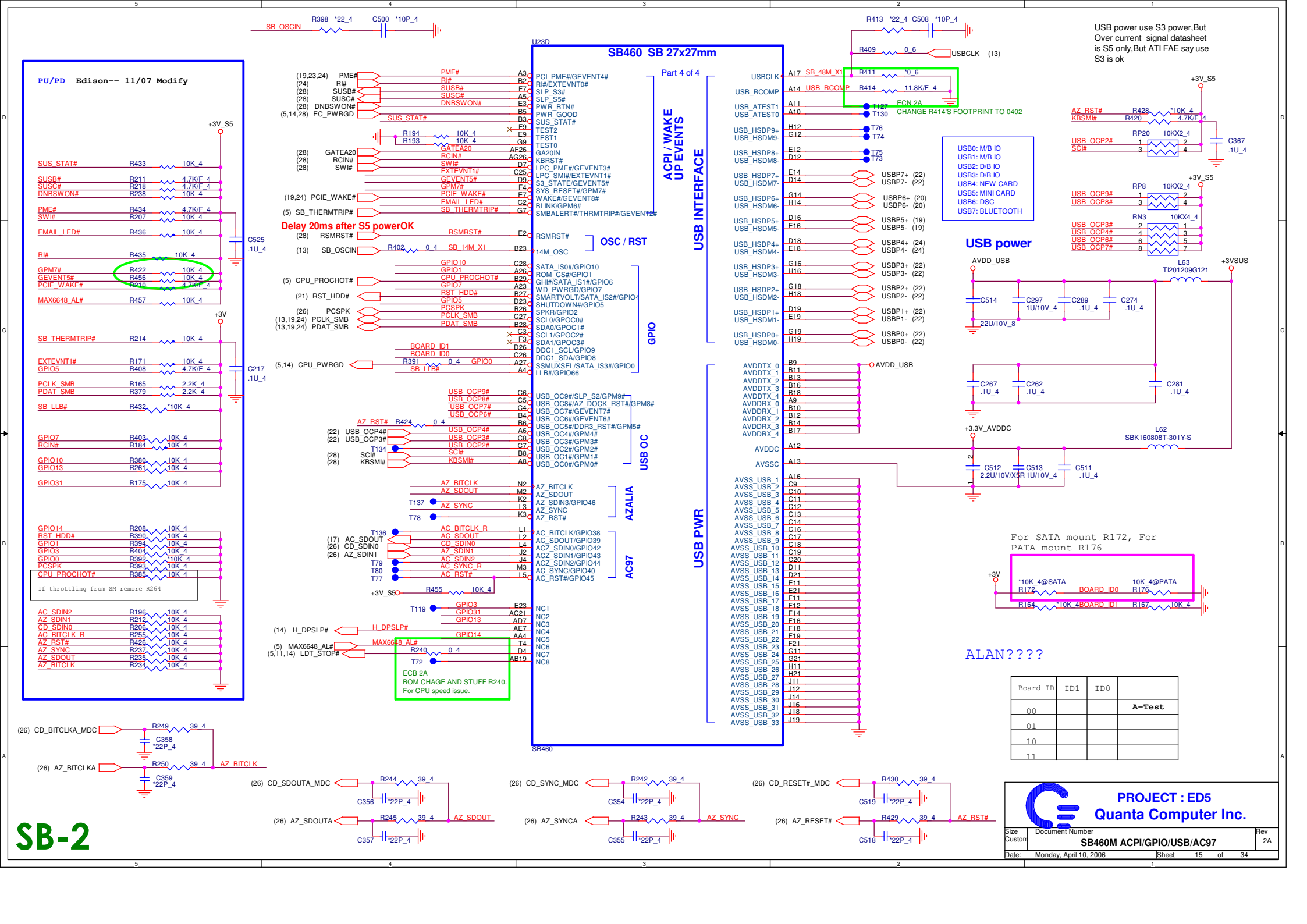
FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

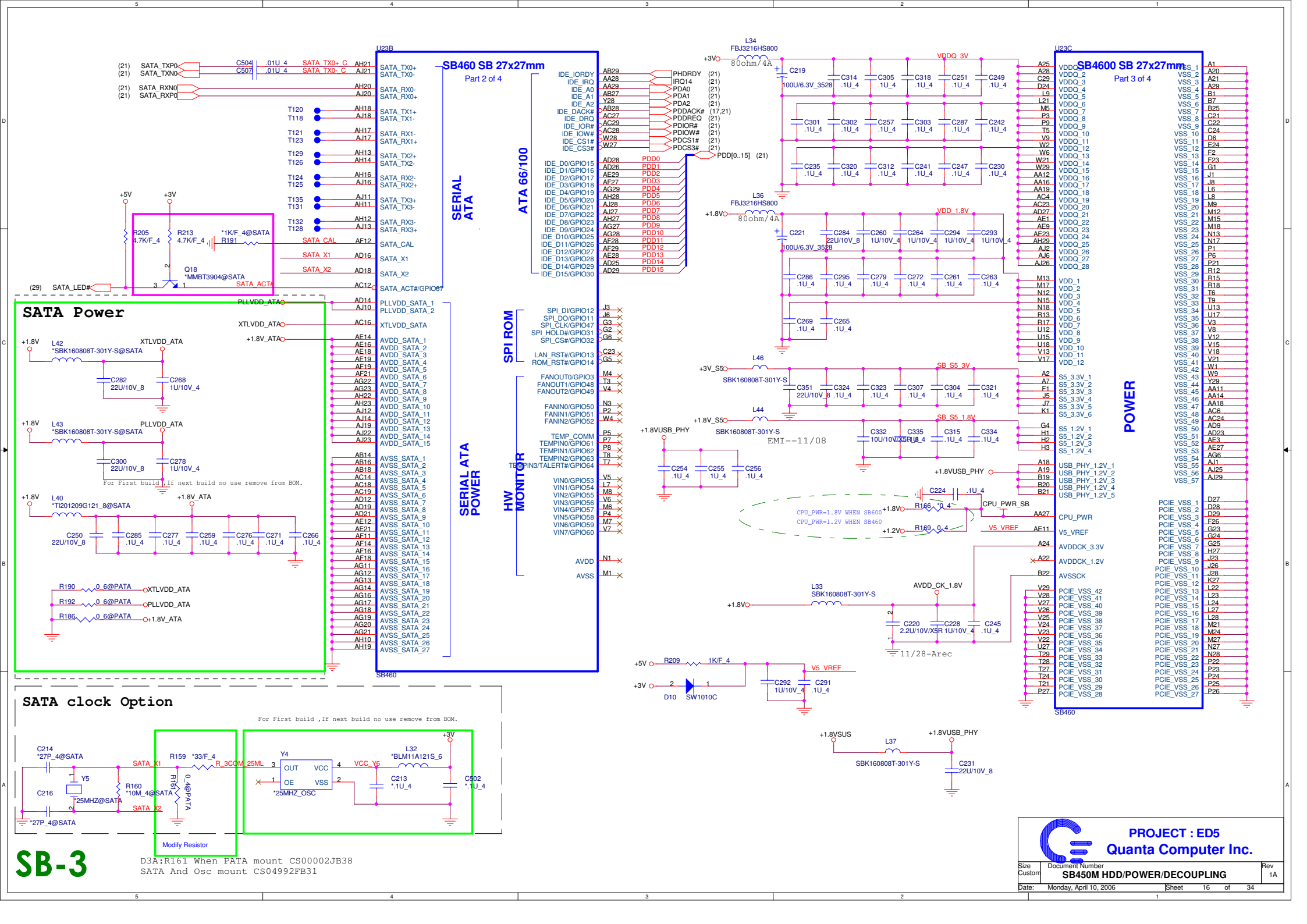
PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	EXTERNAL CLOCK GENERATOR	1A
Date: Monday, April 10, 2006	Sheet 13 of 34	

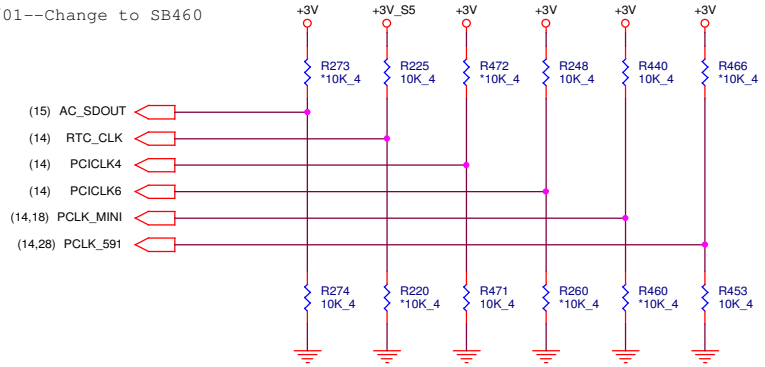


	SB CALIBRATION RESISITOR VALUE	
	SB600	SB460
R1735	562 OHM 1%	150 OHM 1%
R1737	2.05K 1%	150 OHM 1%
R1738	0 ohm	4.12K 1%

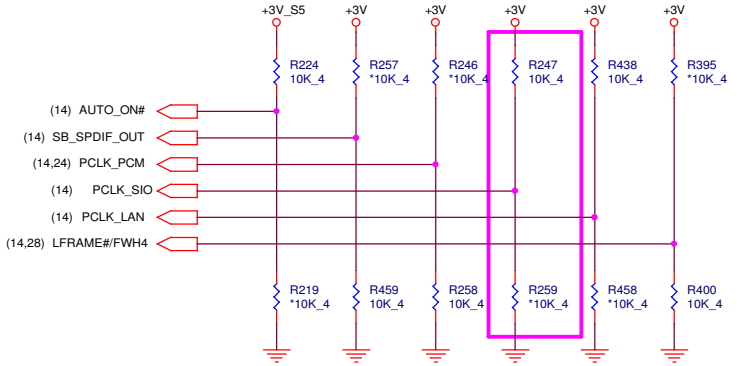

PU/PD Edison-- 11/07 Modify
SB460 SB 27x27mm
Part 4 of 4
USB INTERFACE
ACPI / WAKE UP EVENTS
GPIO
OSC / RST
USB OC
AZALIA
AC97
USB PWR
USB power
USB power use S3 power,But Over current signal datasheet is S5 only,But ATI FAE say use S3 is ok
USB0: M/B IO
USB1: M/B IO
USB2: D/B IO
USB3: D/B IO
USB4: NEW CARD
USB5: MINI CARD
USB6: DSC
USB7: BLUETOOTH
Delay 20ms after S5 powerOK
If throttling from SM remore R264
For SATA mount R172, For PATA mount R176
ECB 2A
BOM CHAGE AND STUFF R240.
For CPU speed issue.
ECN 2A
CHANGE R414'S FOOTPRINT TO 0402
ALAN????
Board ID
ID1
ID0
A-Test
PROJECT : ED5
Quanta Computer Inc.
SB460M ACPI/GPIO/USB/AC97
SB-2


SB460 SB 27x27mm
Part 2 of 4
SERIAL ATA
ATA 66/100
SPI ROM
SERIAL ATA POWER
HW MONITOR
SATA Power
SATA clock Option
For First build ,If next build no use remove from BOM.
Modify Resistor
SB4600 SB 27x27mm
Part 3 of 4
POWER
SB460
EMI--11/08
11/28-Arec
CPU_PWR=1.8V WHEN SB600
CPU_PWR=1.2V WHEN SB460
SB-3
D3A:R161 When PATA mount CS00002JB38
SATA And Osc mount CS04992FB31
PROJECT : ED5
Quanta Computer Inc.
SB450M HDD/POWER/DECOUPLING
Monday, April 10, 2006

Edison-11/01--Change to SB460



D3A:BOM change. R247: Stuff, R259: Un-stuff. Disable USB PHY POWERDOWN.

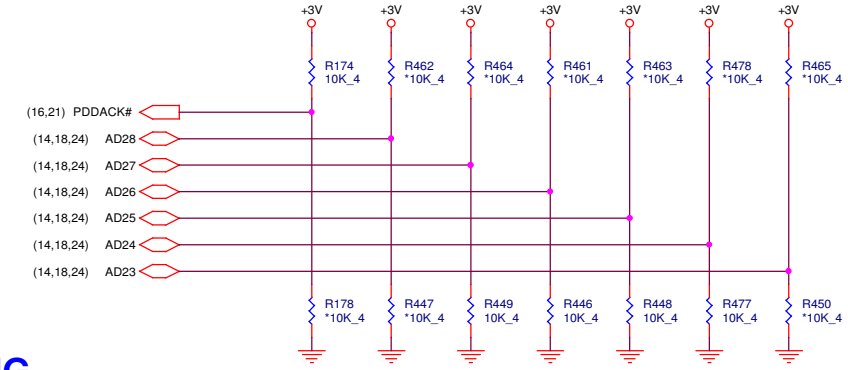


REQUIRED STRAPS

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCLK_MINI PCLK_591
					PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM DEFAULT L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT	NOTE:FOR SB460,PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]

	AUTO_ON#	SB_SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCLK_LAN	LFRAME#
	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

BIOS ENABLE AFTER STARTUP



DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

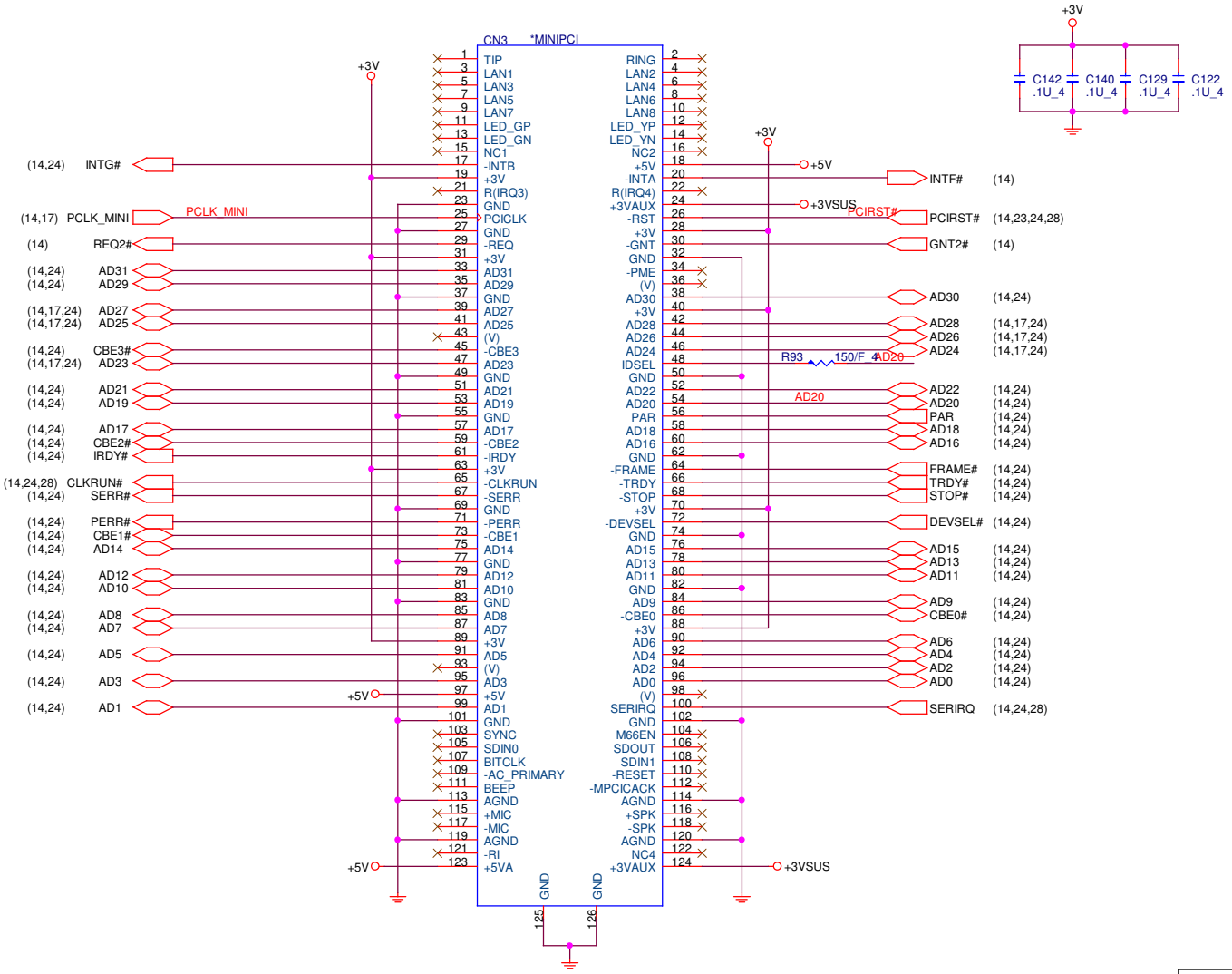
SB-4

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB460M STRAPS	1A
Date: Monday, April 10, 2006	Sheet 17 of 34	

ID Select : AD20
Interrupt Pin : INTG# , INTF#
Request Indicate : REQ2#
Grant Indicate : GNT2#

DEBUG PURPOSE ONLY



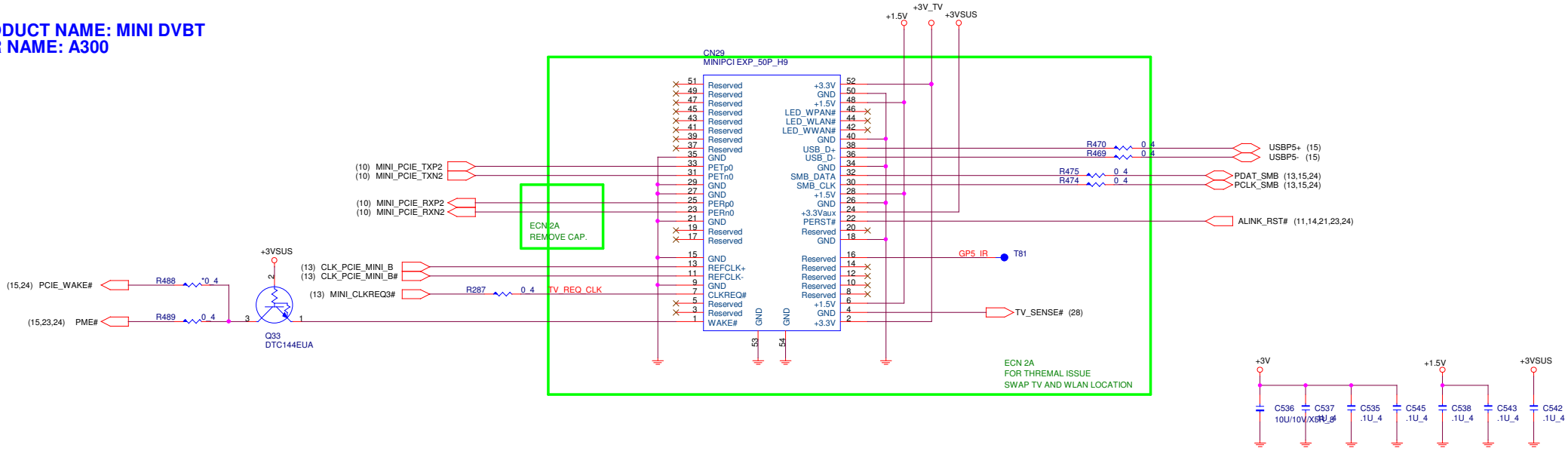
MPC

PROJECT : ED5
Quanta Computer Inc.

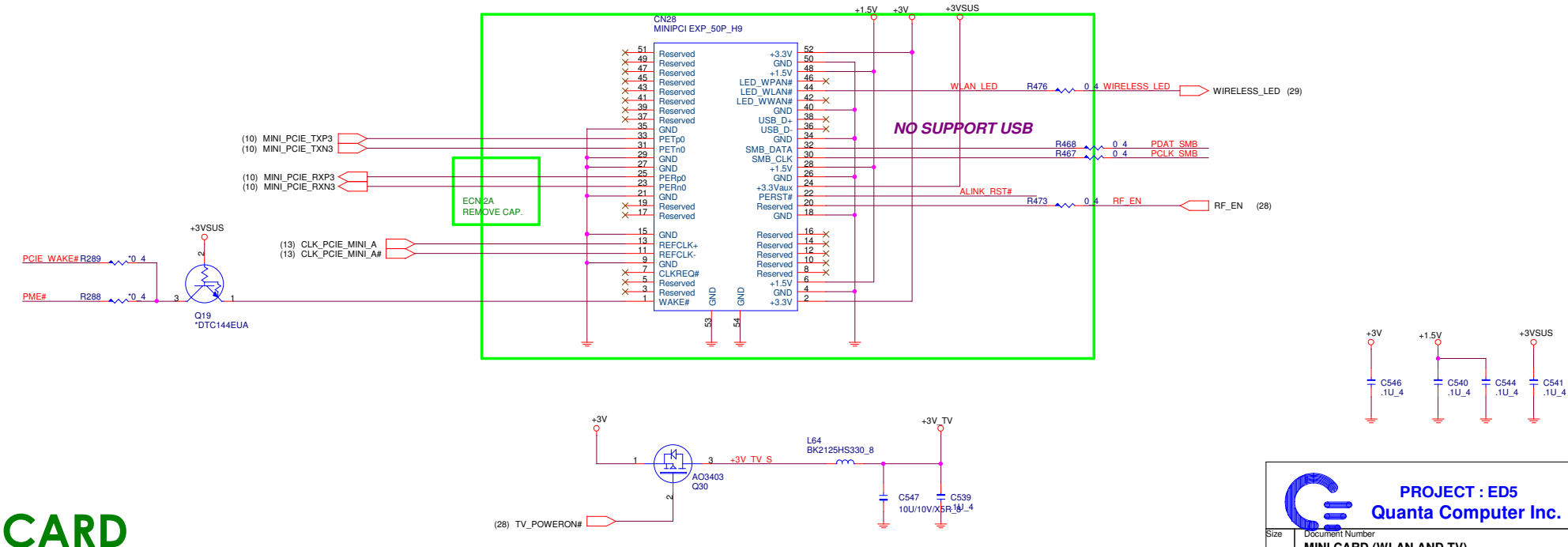
Size	Document Number	Rev
	MINI PCI CONNECTOR (DEBUG ONLY)	1A
Date: Monday, April 10, 2006	Sheet 18 of 34	

TV MINI CARD

PRODUCT NAME: MINI DVBT
MFR NAME: A300



WLAN MINI CARD

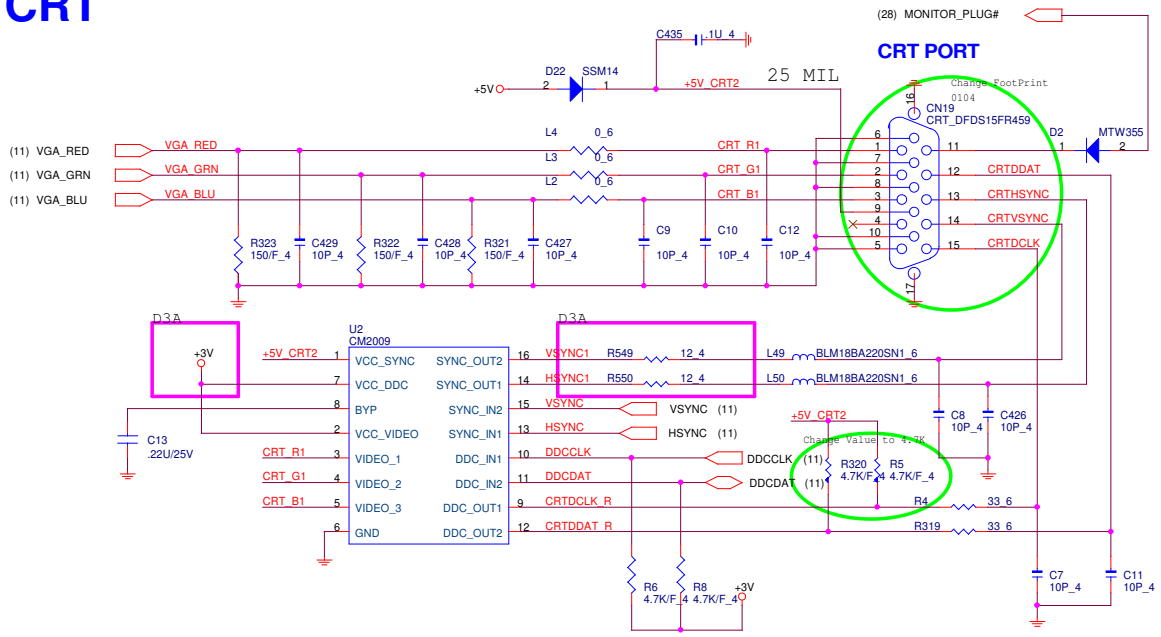


MINI CARD

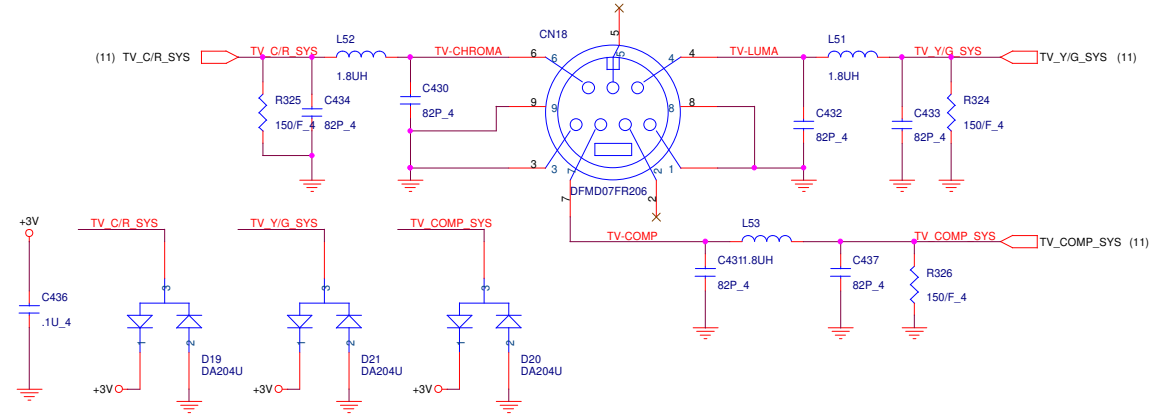
PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	MINI CARD (WLAN AND TV)	2A
Date: Monday, April 10, 2006	Sheet 19 of 34	

CRT

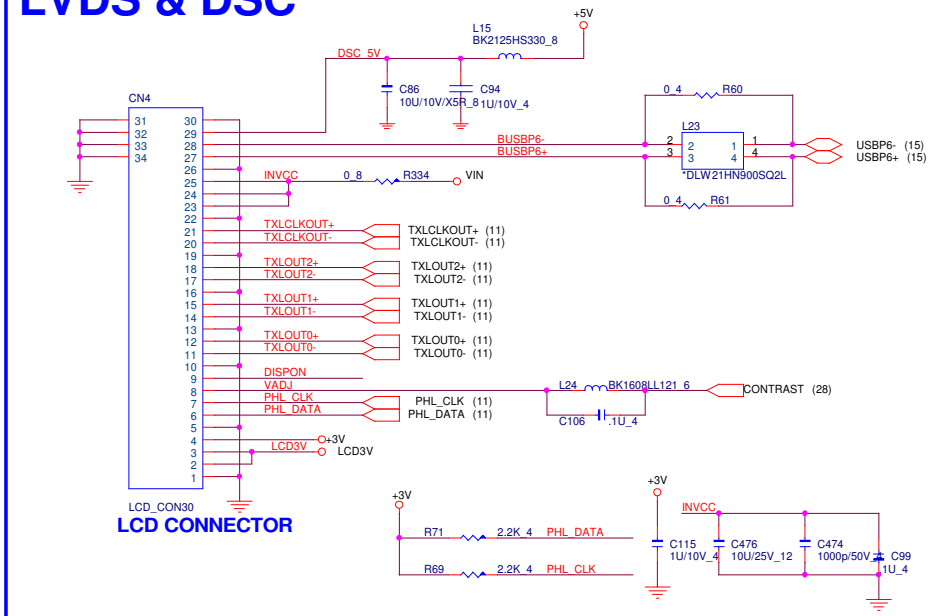


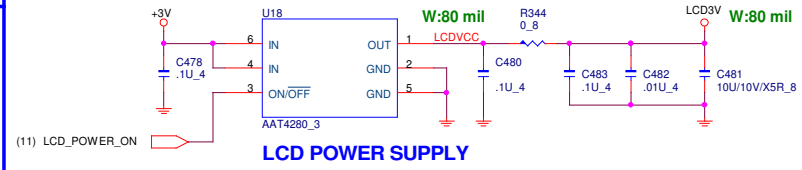
TV

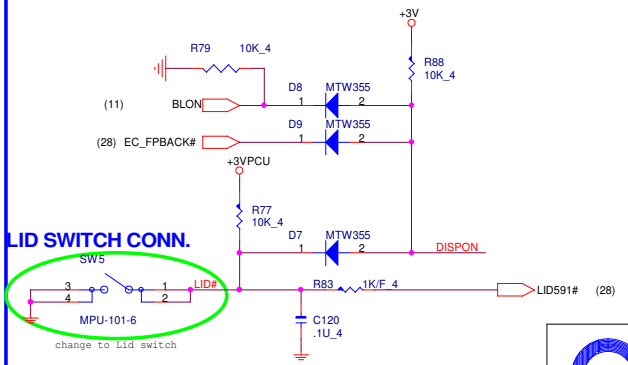


CRT, LVDS, TV, DSC

LVDS & DSC

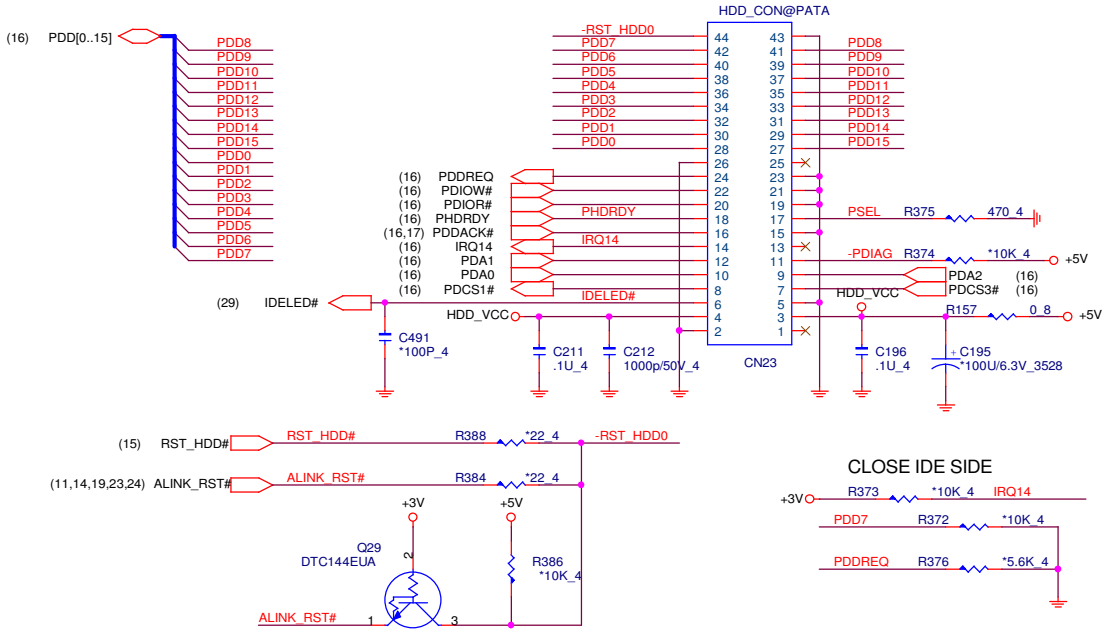




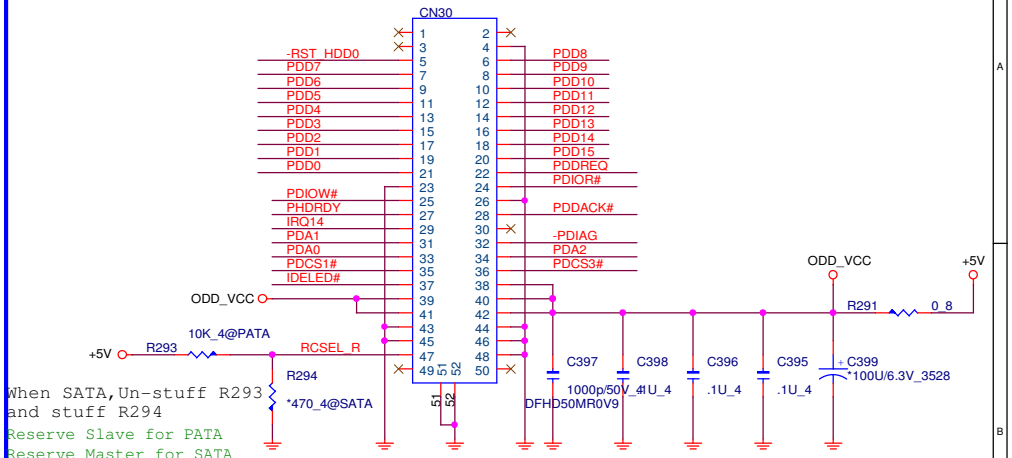


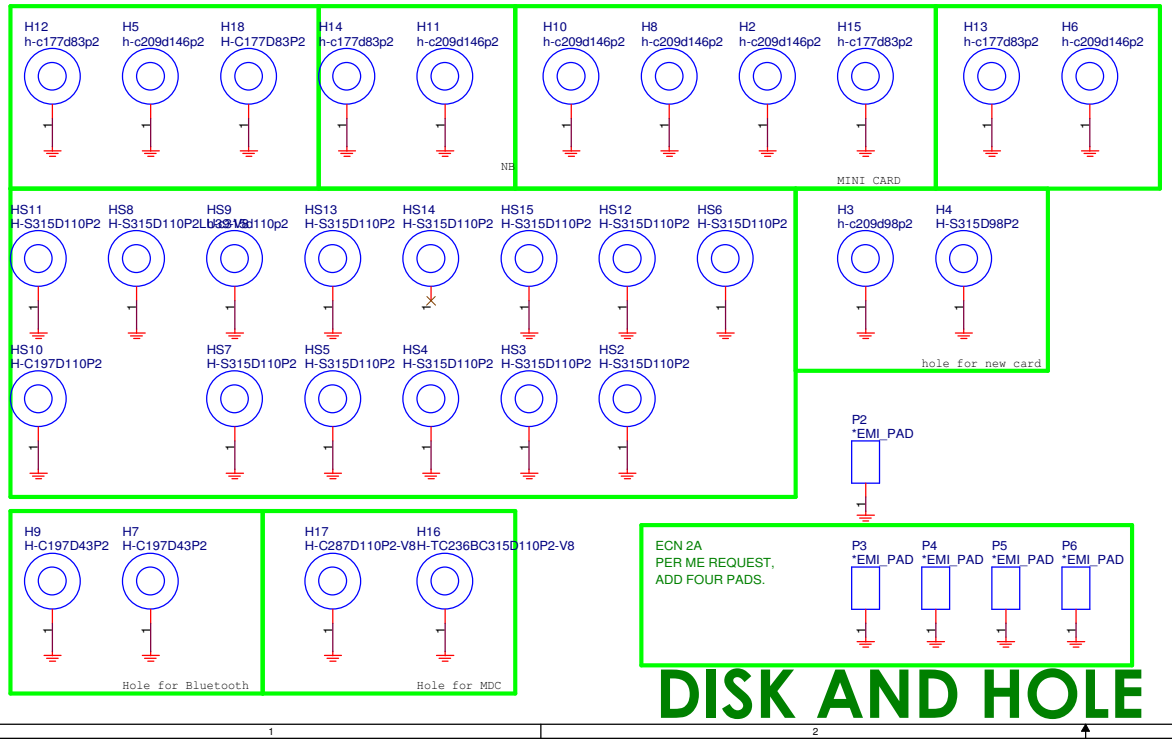
PROJECT : ED5		
Quanta Computer Inc.		
Size	Document Number	Rev
	VGA Ports, LID, S-VIDEO, DSC	1A
Date: Monday, April 10, 2006	Sheet 20 of 34	

PATA HDD



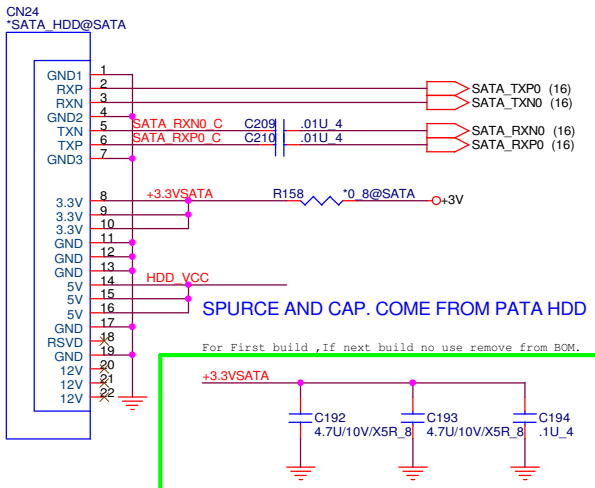
PATA ODD

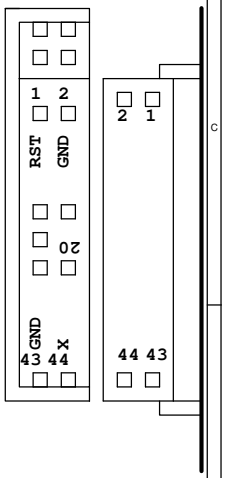




DISK AND HOLE

SATA HDD



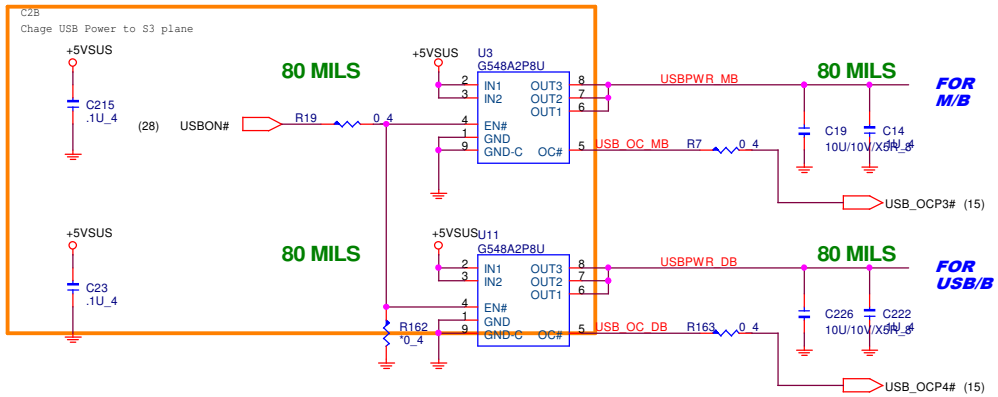


PROJECT : ED5

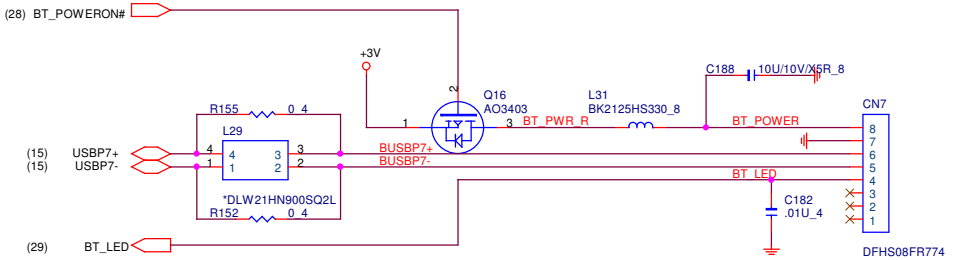
Quanta Computer Inc.

Size	Document Number	Rev
	HDD & CDROM , HOLES	2A
Date: Monday, April 10, 2006	Sheet 21 of 34	

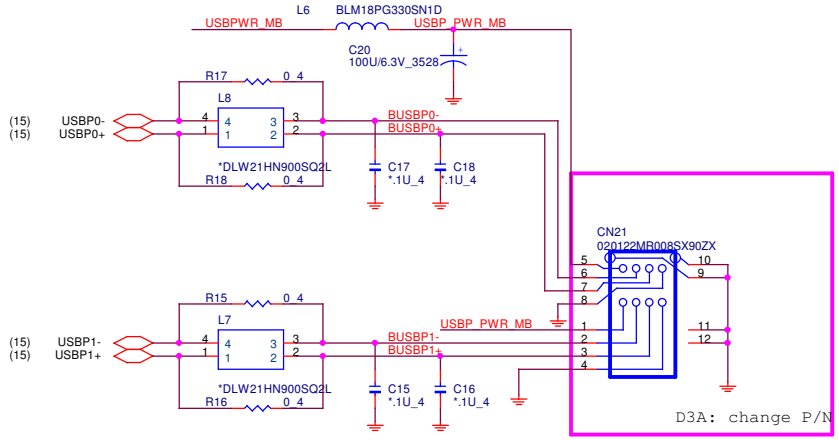
USB POWER SUPPLY



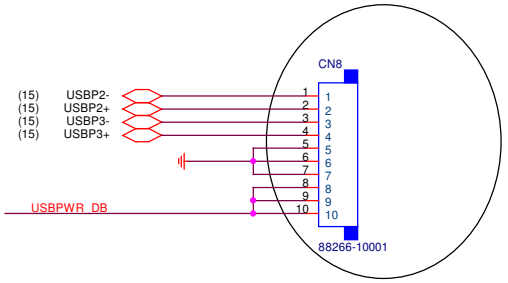
BLUETOOTH



USB I/O CONNECTORS



USB BAORD WIRE CONNECTOR

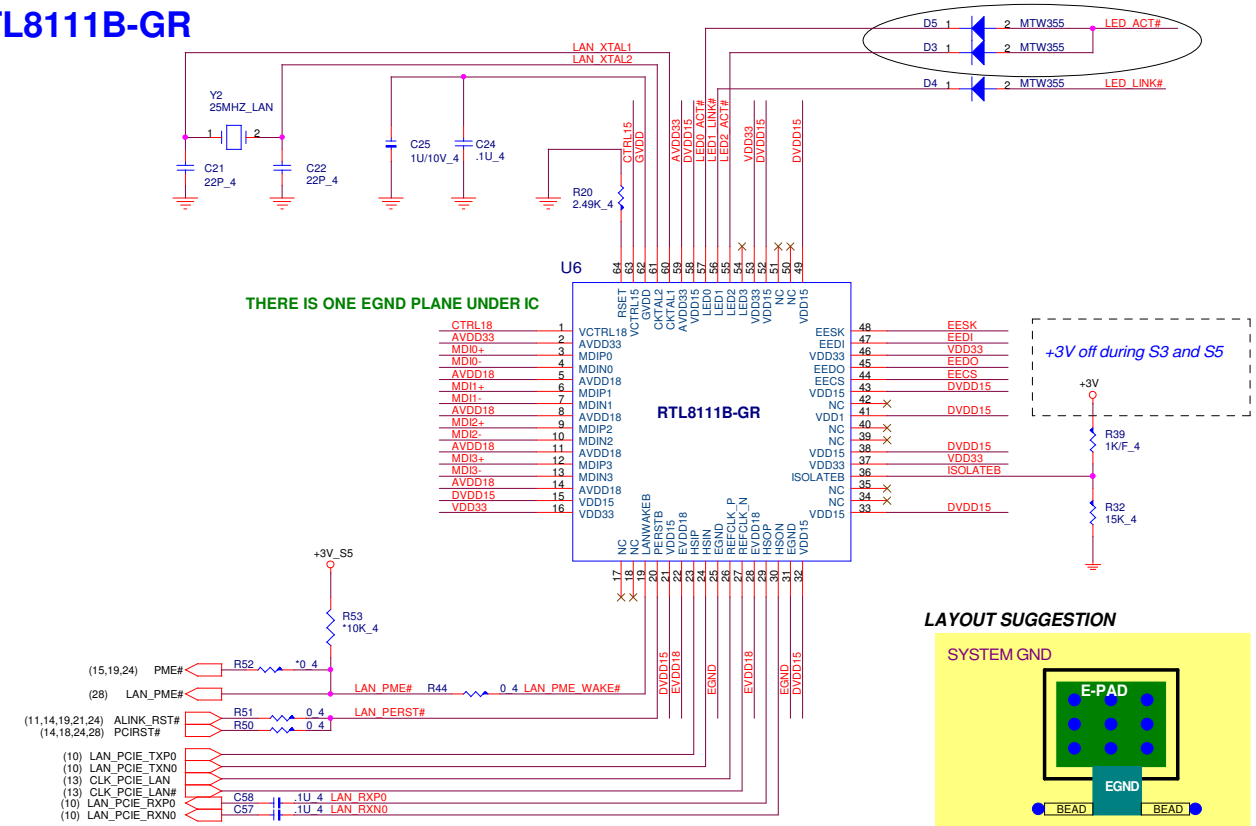


USB, BT, USB/B COONECTOR

PROJECT : ED5
Quanta Computer Inc.

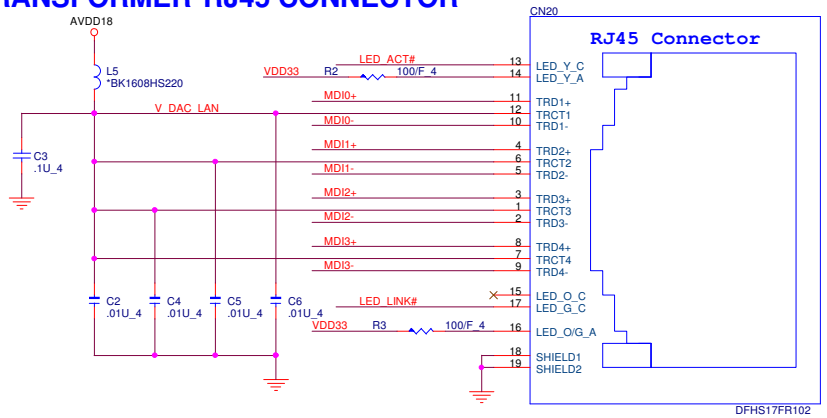
Size	Document Number	Rev
	MINI PCI & USB PORT & BT	1A
Date: Monday, April 10, 2006	Sheet 22 of 34	

RTL8111B-GR

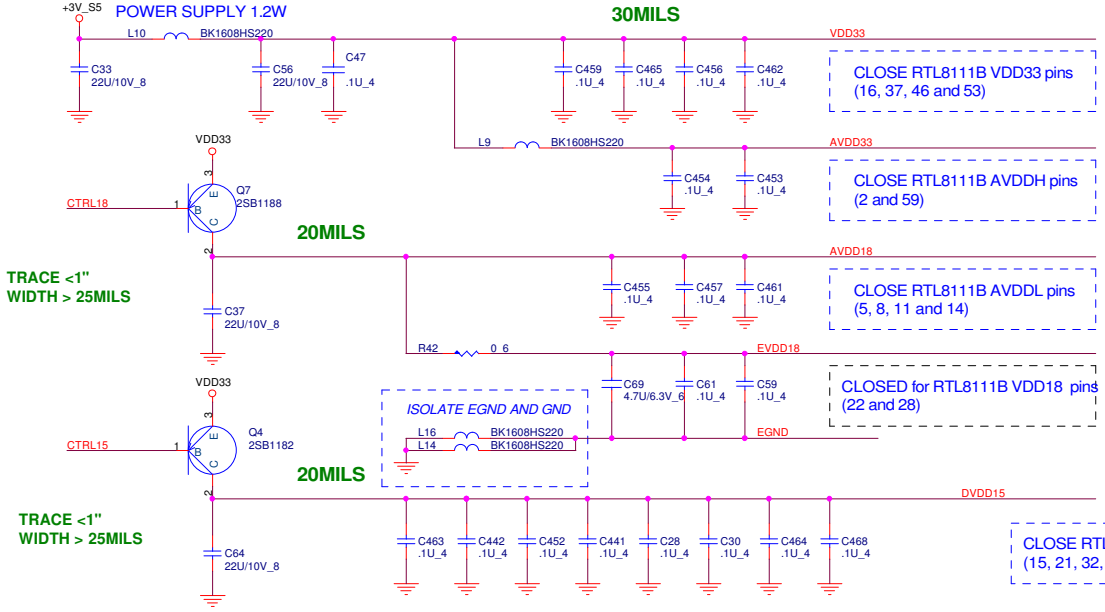


LAYOUT SUGGESTION

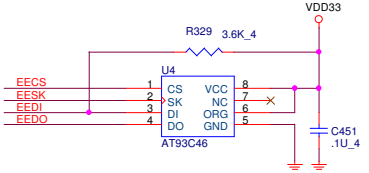
TRANSFORMER RJ45 CONNECTOR



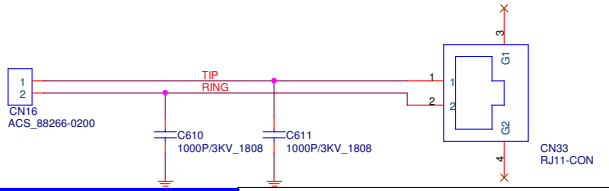
POWER SUPPLY



EEPROM



RJ11



LAN

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	LAN RTL8111B-GR PCI-E & RJ11	1A

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PCI8402 PCI I/F

ID Select : AD17
Interrupt Pin : INTE# , INTG#, INTH#
Request Indicate : REQ3#
Grant Indicate : GNT3#

AD17 R405 150/F_4 PCM_IDSEL

ECN 2A
BOM CHANGE
REMOVE Y7 AND C509
STUFF R407

R407 0_4 CLK48_PCM (13)

Y7 *48MHz C509 *.1U_4 +3V

(14,17,18) AD[0..31] AD[0..31]

U24A PCIXX12_0

CLK48 F1 CLK48M 3
GRST K5 GRST#_8412
SUSPEND J5 8402_SUS# R415 10K_4 +3V

MFUNC0 G1 INTE# R416 0_4 INTE# (14)
MFUNC1 H5 INTH# INTG# (14,18)
MFUNC2 H2 SERIRQ INTH# (14)
MFUNC3 H1 3VSP R406 4.7K/F_4 SERIRQ (14,18,28)
MFUNC4 J1 FM_LED +3V
MFUNC5 J2 CLKRUN# FM_LED (25)
MFUNC6 J3 CLKRUN# (14,18,28)

PCLK L1 PCLK_PCM PCLK_PCM (14,17)
PRST K3 PCIRST# PCIRST# (14,18,23,28)
SPKROUT H3 PCMSPK PCMSPK (26)
RI_OUT/PME L5 PCM_PME# R189 *0_4 RI# (15)

SDA G3 SDA_CARD
SCL G2 SCL_CARD

LATCH C9
DATA B9
CLOCK A9

USB_EN E10 USB_EN# R427 *10K_4 +3V

PHY_TEST_MA P17 TEST_MA R216 4.7K/F_4 1394_AVDD
TEST0 P12
PSMODE C4 R417 10K_4 +3V
RSVD // VD0 // VCCD1# E5
NC

Q17 DTC144EUA +3V PME#
R188 0_4

(14,18) CBE0# CBE1# CBE2# CBE3#
(14,18) PAR DEVSEL# FRAME# GNT3# PCM_IDSEL
(14,18) IRDY# PERR# REQ3# SERR# STOP# TRDY#

PCLK_PCM R397 *22_4 PCLK_PCM_R C499 *10p_4
CLK48_PCM R399 *22_4 CLK48_PCM_R C501 *10p_4

U24B PCMCIA PORT PCIXX12_0

(15,19,23)

NEW CARD

NEW CARD HEADER: DFHD26MR074 (13081-1)
NEW CARD EJECTER: FBZF1026019 (130851-3)

CN6 FOXCONN_NEW_CARD

(10) PCIE_TXP1 (10) PCIE_TXN1
(10) PCIE_RXP1 (10) PCIE_RXN1
C126 .1U_4 PERP1
C125 .1U_4 PERN1
(13) CLK_PCIE_NEW (13) CLK_PCIE_NEW#
CPPE#
(13) NEW_CLKREQ#
+NEW_3V
NEW_PERST#
+NEW_3VAUX
NEWCARD_PCIE_WAKE#
+NEW_1.5V
(13,15,19) PDAT_SMB (13,15,19) PCLK_SMB
CPUSB#
(15) USBP4+ (15) USBP4-
R95 0_4 BUSBP4+
R94 0_4 BUSBP4-

+3V_S5 Q13 DTC144EUA
(15,19) PCIE_WAKE# NEWCARD_PCIE_WAKE#

NEW CARD'S POWER SWITCH

U8 TPS2231PWG4

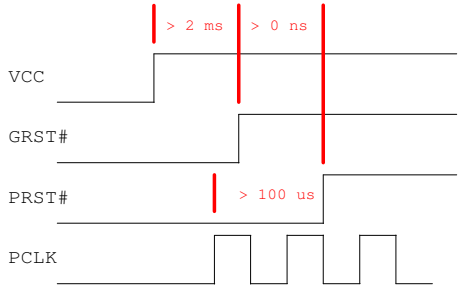
+3V +3V_S5 +1.5V
(11,14,19,21,23) ALINK_RST#
+NEW_3V +NEW_3VAUX +NEW_1.5V
CPPE# CPUSB# NEW_PERST#

CPPE# : (Internal Pull Up , active low when card support PCIE)
CPUSB# : (Internal Pull Up , active low when card support USB)
SHDN# : (Internal Pull Up)

IEEE1394 EEPROM

+3V R389 2.2K_4 R387 2.2K_4
SDA_CARD SCL_CARD
U22 24LC08
WP GND VCC +3V C506 .1U_4

+3V R181 22K/F_4 GRST#_8412 C232 .22U/6V_4



+3V C155 .1U_4 C141 .1U_4 C158 .1U_4
+NEW_3VAUX C152 .1U_4
+NEW_3V C168 10U/10V/X5R_8 C160 .1U_4 C166 .1U_4
+NEW_1.5V C167 10U/10V/X5R_8 C162 .1U_4

IEEE1394 & NEW CARD

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Quanta Computer Inc.

Size	Document Number	Rev
	PCI8402-1 & NEW CARD	2A
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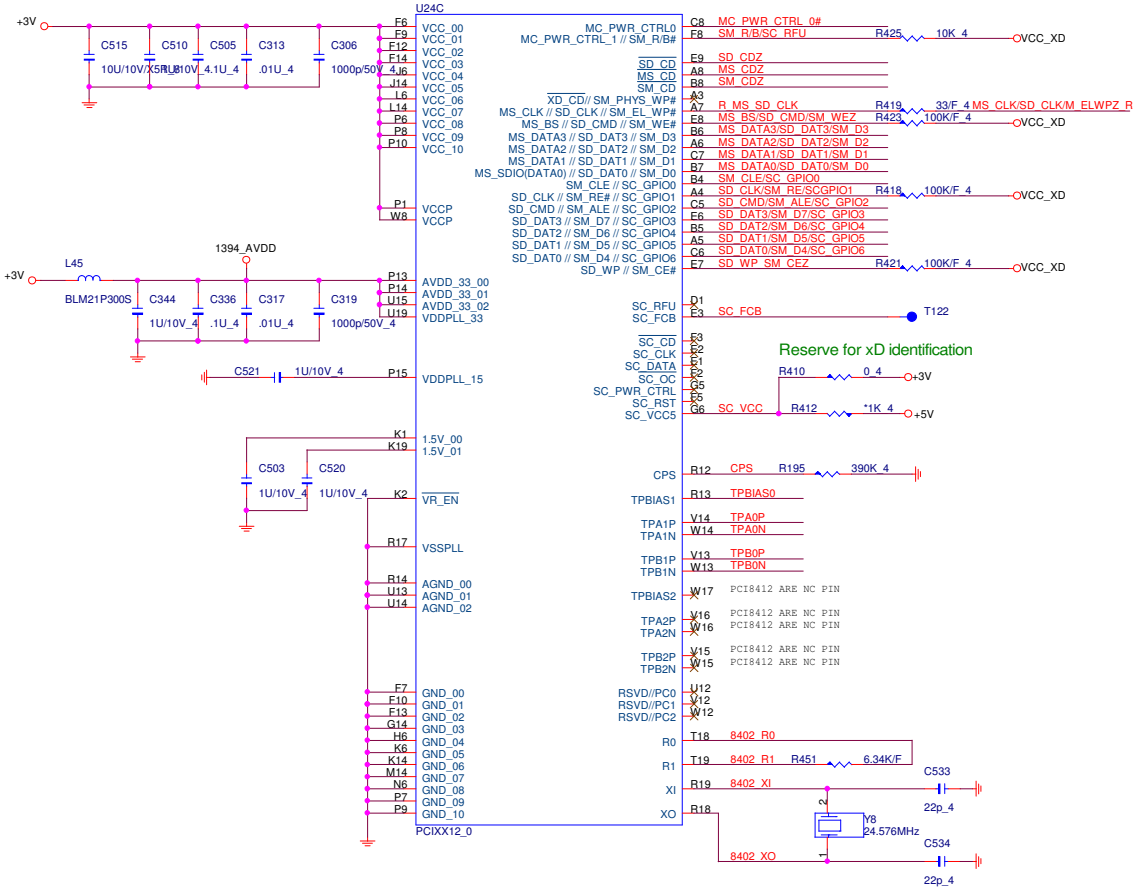
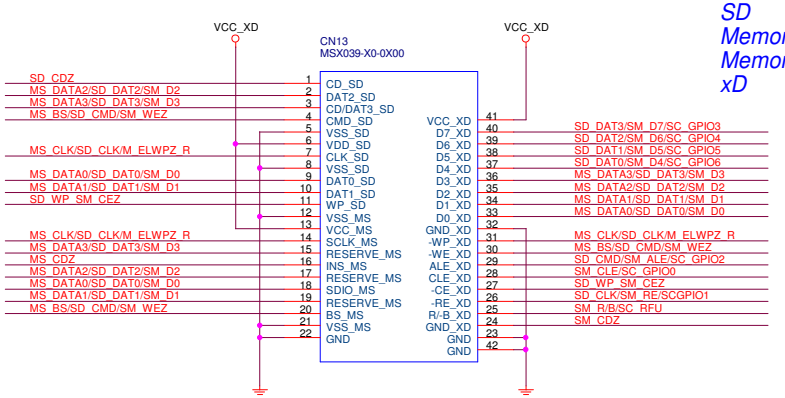
PCI8402 I/F OF 1394 & CARD READER



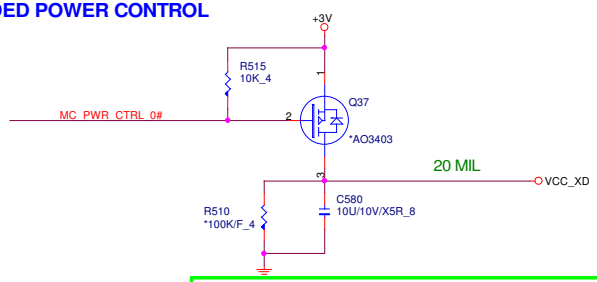
5 IN 1 MEMORY CARD READER

Support :

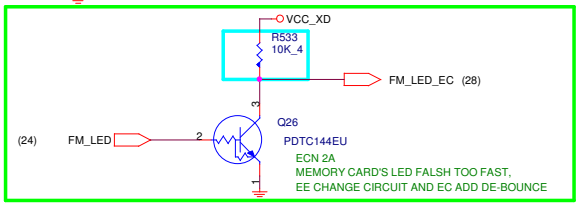
MMC
SD
Memory Stick
Memory Stick Pro
xD



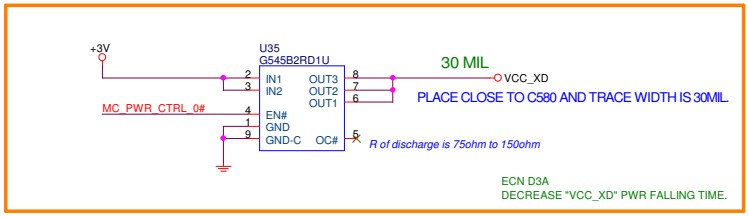
MEMORY CARD READED POWER CONTROL



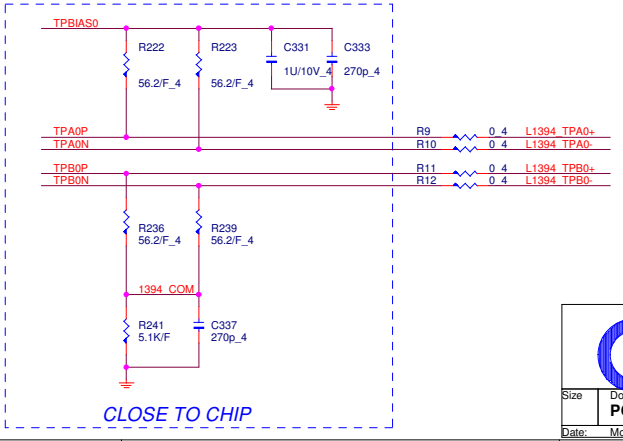
MEMORY CARD READED LED INDICATE

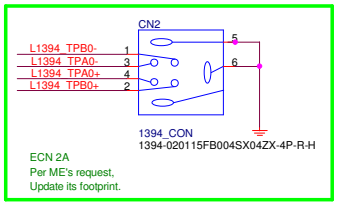


MEMORY CARD READED POWER CONTROL (IC SOLUTION FOR C-TEST)



IEEE1394 CONNECTOR





IEEE1394 & CARD REDER

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	PCI8402-2 (1394 & 5 IN 1)	2A
Date: Monday, April 10, 2006	Sheet 25 of 34	

AUDIO CODEC ALC262

ALC262 GPIO TABLE

GPIO 0	SRS	LO: SRS OFF (EC) HI: SRS ON (EC)
GPIO 1	H.P.	LO: NO PLUG-IN HI: PLUG-IN

D3A In order to Vista's request,
EAPD force MUTE,Remove Q34,R490

60 mils

RESERVE BYPASS PATH

ECN C2B
ADD CODEC_JD

ECN C2B
PER VISTA REQUEST,
ADD PWR FOR MIC.

ECN C2B
PER VISTA REQUEST,
MODIFY MIC PATH

Layout note:

CD_GND	5mil	5mil
CD_L	5mil	10mil
CD_GND	5mil	5mil
CD_R	5mil	10mil
CD_GND		5mil

AUDIO POWER AND GND

20 mil

20 mil

Vout=Vset(1+R(4,5)/R(5,gnd))
Vset=1.25V

Vout=1.25(1+29.4K/10K)=4.925V
Vout=1.25(1+28.7K/10K)=4.8375V
Vout=1.25(1+27K/10K)=4.625V

SPRAY THE BRIDGE ON THE GAP OF A/DGND UNIFORMLY.

AZALIA MDC INTERFACE

AUDIO CODEC & MDC

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Quanta Computer Inc.

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	AUDIO CODEC ALC262 AND MDC	2A

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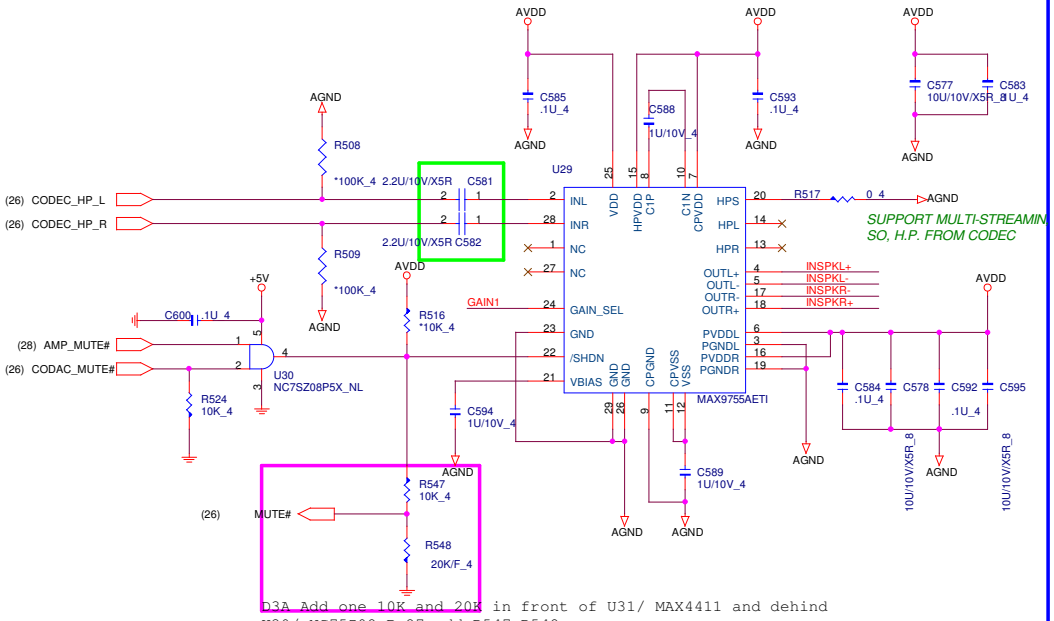
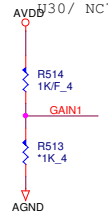
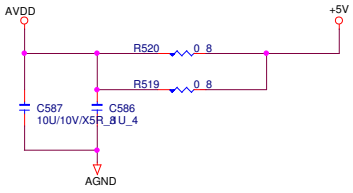
AUDIO AMP. (MAX9755)

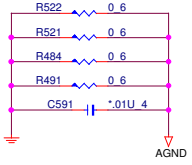


D3A Add one 10K and 20K in front of U31/ MAX4411 and dehind U30/ NC75Z08 P.27 add R547,R548



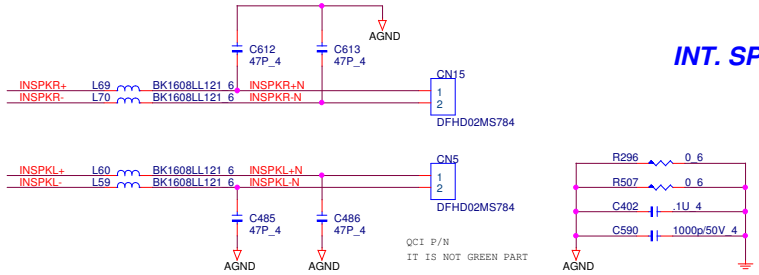
GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0

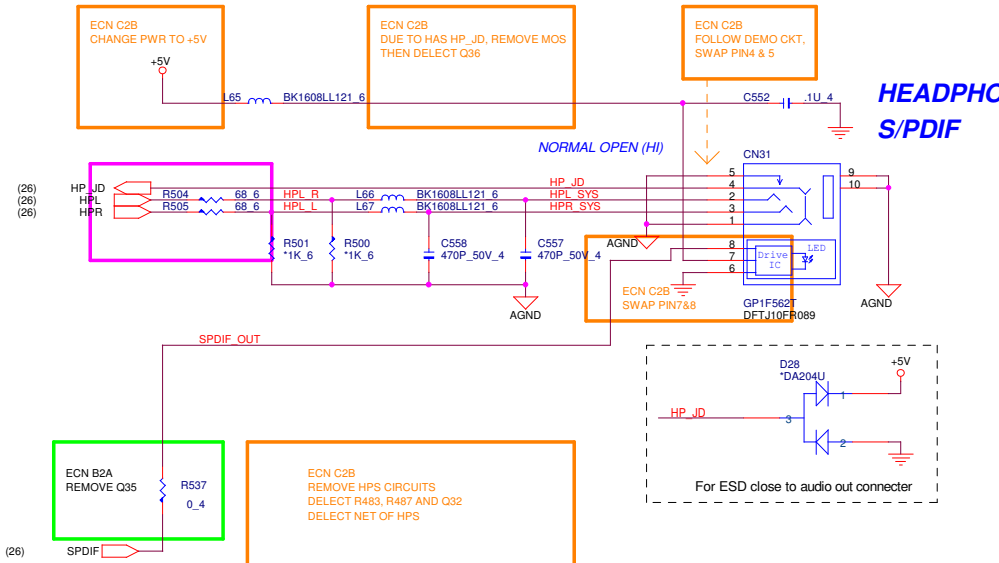


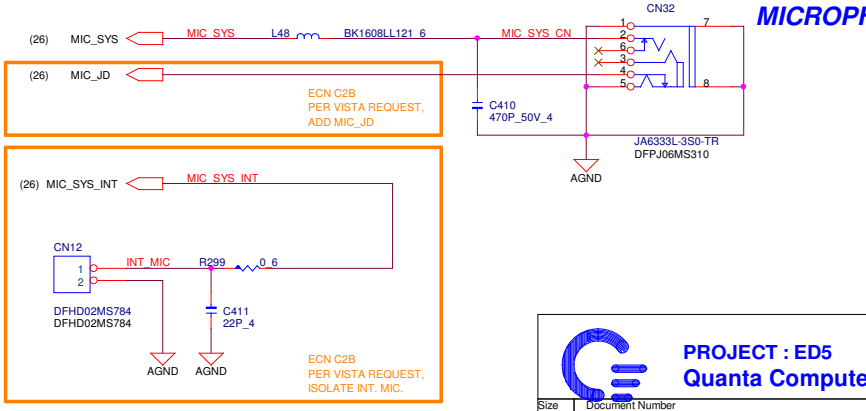


AMP. POWER SUPPLY

AUDIO JACK







AUDIO AMP. & JACK

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	AMP. & JACK	1A
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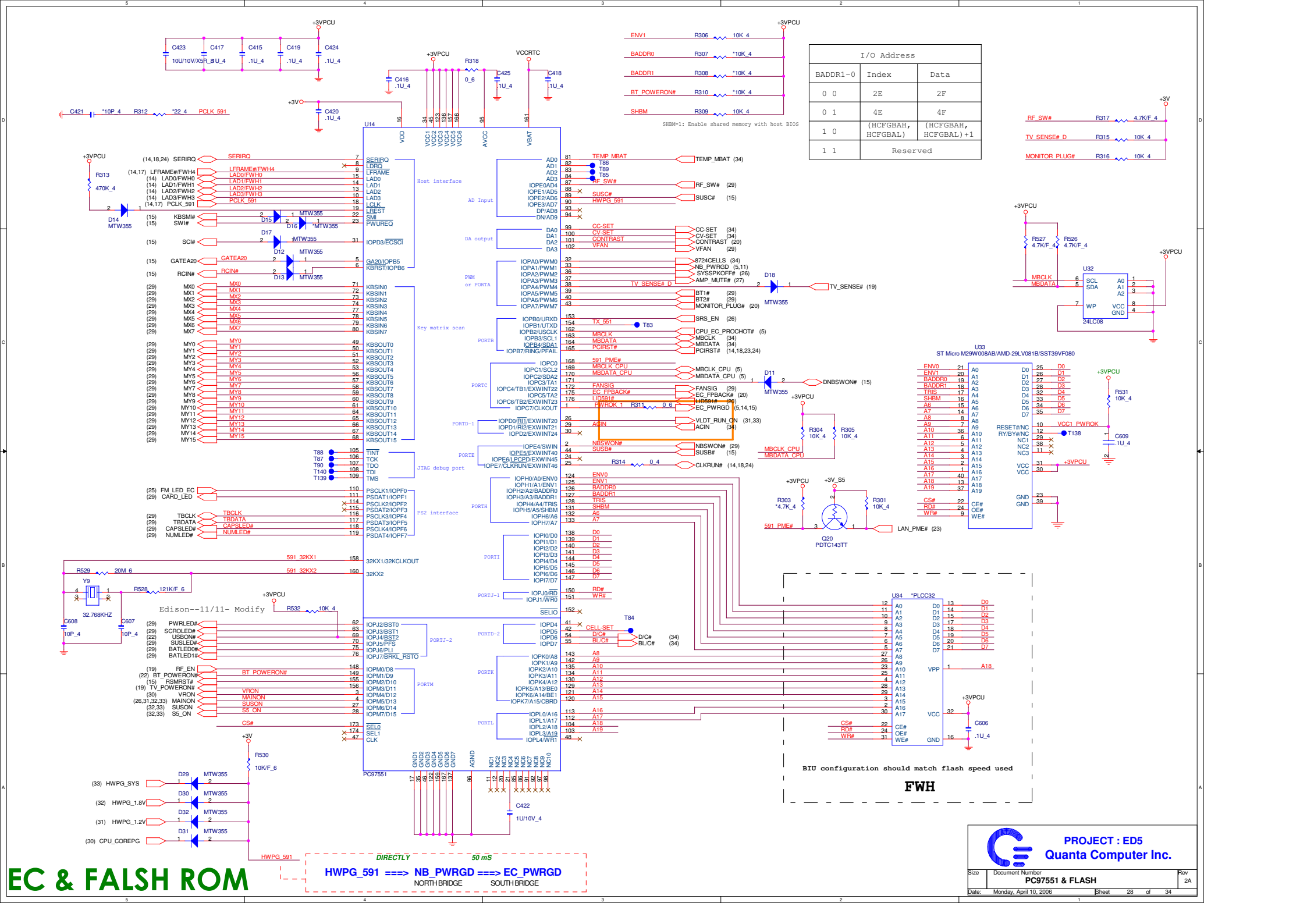
I/O Address
BADDR1-0 | Index | Data
0 0 | 2E | 2F
0 1 | 4E | 4F
1 0 | (HCFGBAH, HCFGBAL) | (HCFGBAH, HCFGBAL)+1
1 1 | Reserved
SHBM=1: Enable shared memory with host BIOS
U14
PC97551
Host interface
AD Input
DA output
PWM or PORTA
Key matrix scan
PORTB
PORTC
PORTD-1
PORTE
JTAG debug port
PS2 interface
PORTH
PORTI
PORTJ-1
PORTD-2
PORTJ-2
PORTK
PORTM
PORTL
U33
ST Micro M29W008AB/AMD-29LV081B/SST39VF080
U32
24LC08
U34 *PLCC32
Edison--11/11- Modify
BIU configuration should match flash speed used
FWH
DIRECTLY
50 mS
HWPG_591 ===> NB_PWRGD ===> EC_PWRGD
NORTH BRIDGE
SOUTH BRIDGE
EC & FALSH ROM
PROJECT : ED5
Quanta Computer Inc.
Document Number
PC97551 & FLASH
Rev
2A
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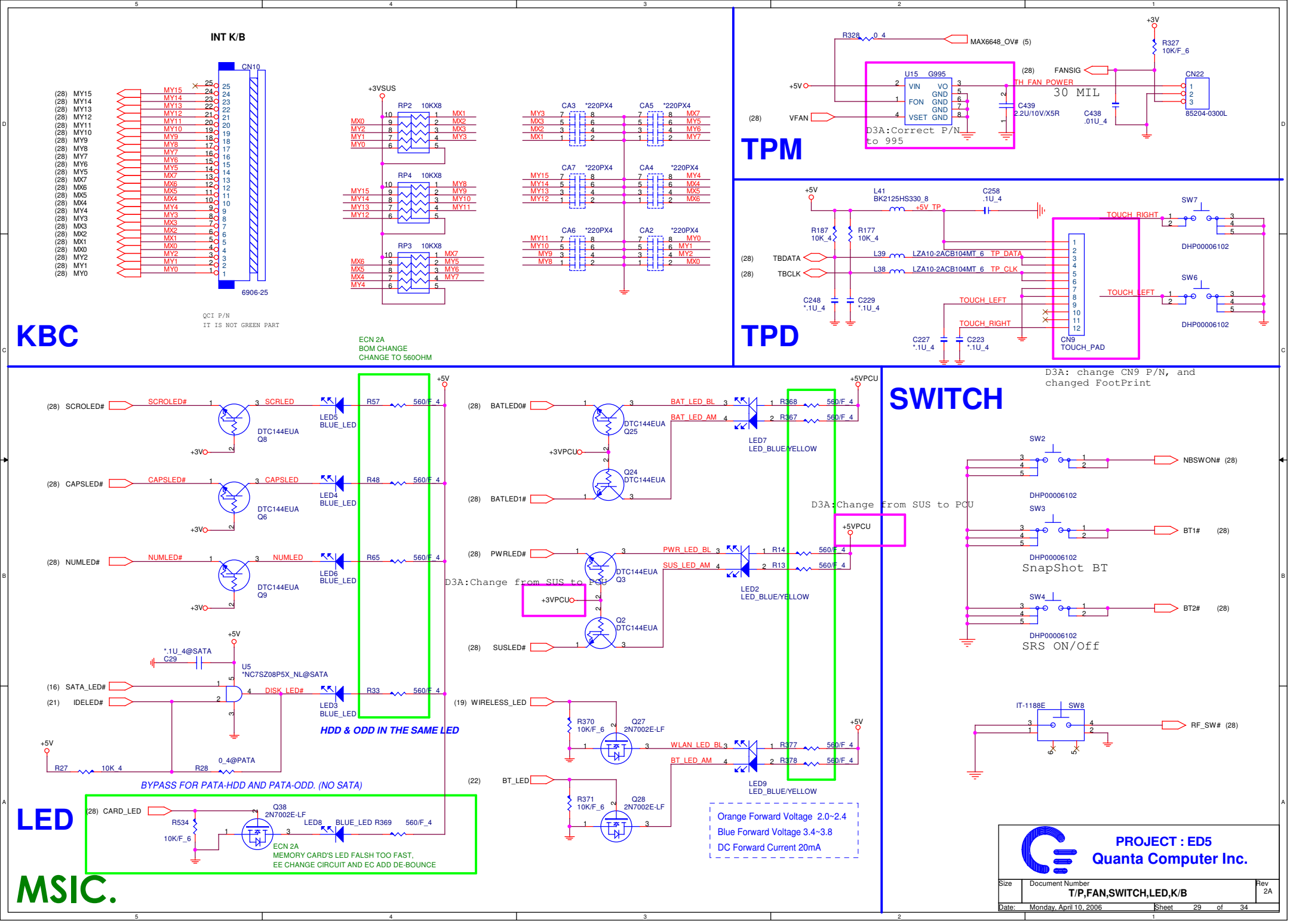
INT K/B
CN10
6906-25
QCI P/N
IT IS NOT GREEN PART
KBC
+3VSUS
RP2 10KX8
RP4 10KX8
RP3 10KX8
ECN 2A
BOM CHANGE
CHANGE TO 560OHM
R328 0_4
MAX6648_OV# (5)
U15 G995
D3A:Correct P/N to 995
FANSIG
TH_FAN_POWER
30 MIL
R327 10K/F_6
CN22
85204-0300L
C439 2.2U/10V/X5R
C438 .01U_4
TPM
L41 BK2125HS330_8
C258 .1U_4
+5V_TP
R187 10K_4
R177 10K_4
TBDATA
TBCLK
L39 LZA10-2ACB104MT_6 TP_DATA
L38 LZA10-2ACB104MT_6 TP_CLK
C248 *.1U_4
C229 *.1U_4
TOUCH_LEFT
TOUCH_RIGHT
SW7
SW6
DHP00006102
C227 *.1U_4
C223 *.1U_4
CN9
TOUCH_PAD
TPD
D3A: change CN9 P/N, and changed FootPrint
SCROLED#
CAPSLED#
NUMLED#
DTC144EUA
LED5 BLUE_LED
LED4 BLUE_LED
LED6 BLUE_LED
R57 560/F_4
R48 560/F_4
R65 560/F_4
*.1U_4@SATA C29
U5 *NC7SZ08P5X_NL@SATA
SATA_LED#
IDELED#
DISK_LED#
LED3 BLUE_LED
R33 560/F_4
R27 10K_4
R28 0_4@PATA
HDD & ODD IN THE SAME LED
BYPASS FOR PATA-HDD AND PATA-ODD. (NO SATA)
BATLED0#
BATLED1#
BAT_LED_BL
BAT_LED_AM
LED7 LED_BLUE/YELLOW
D3A:Change from SUS to PCU
PWRLED#
SUSLED#
PWR_LED_BL
SUS_LED_AM
LED2 LED_BLUE/YELLOW
WIRELESS_LED
BT_LED
WLAN_LED_BL
BT_LED_AM
LED9 LED_BLUE/YELLOW
Orange Forward Voltage 2.0~2.4
Blue Forward Voltage 3.4~3.8
DC Forward Current 20mA
LED
CARD_LED
Q38 2N7002E-LF
R534 10K/F_6
LED8 BLUE_LED R369 560/F_4
ECN 2A
MEMORY CARD'S LED FALSH TOO FAST,
EE CHANGE CIRCUIT AND EC ADD DE-BOUNCE
MSIC.
SWITCH
SW2
SW3
SW4
NBSWON# (28)
BT1# (28)
BT2# (28)
SnapShot BT
SRS ON/Off
IT-1188E SW8
RF_SW# (28)
PROJECT : ED5
Quanta Computer Inc.
Size
Document Number
T/P,FAN,SWITCH,LED,K/B
Rev 2A
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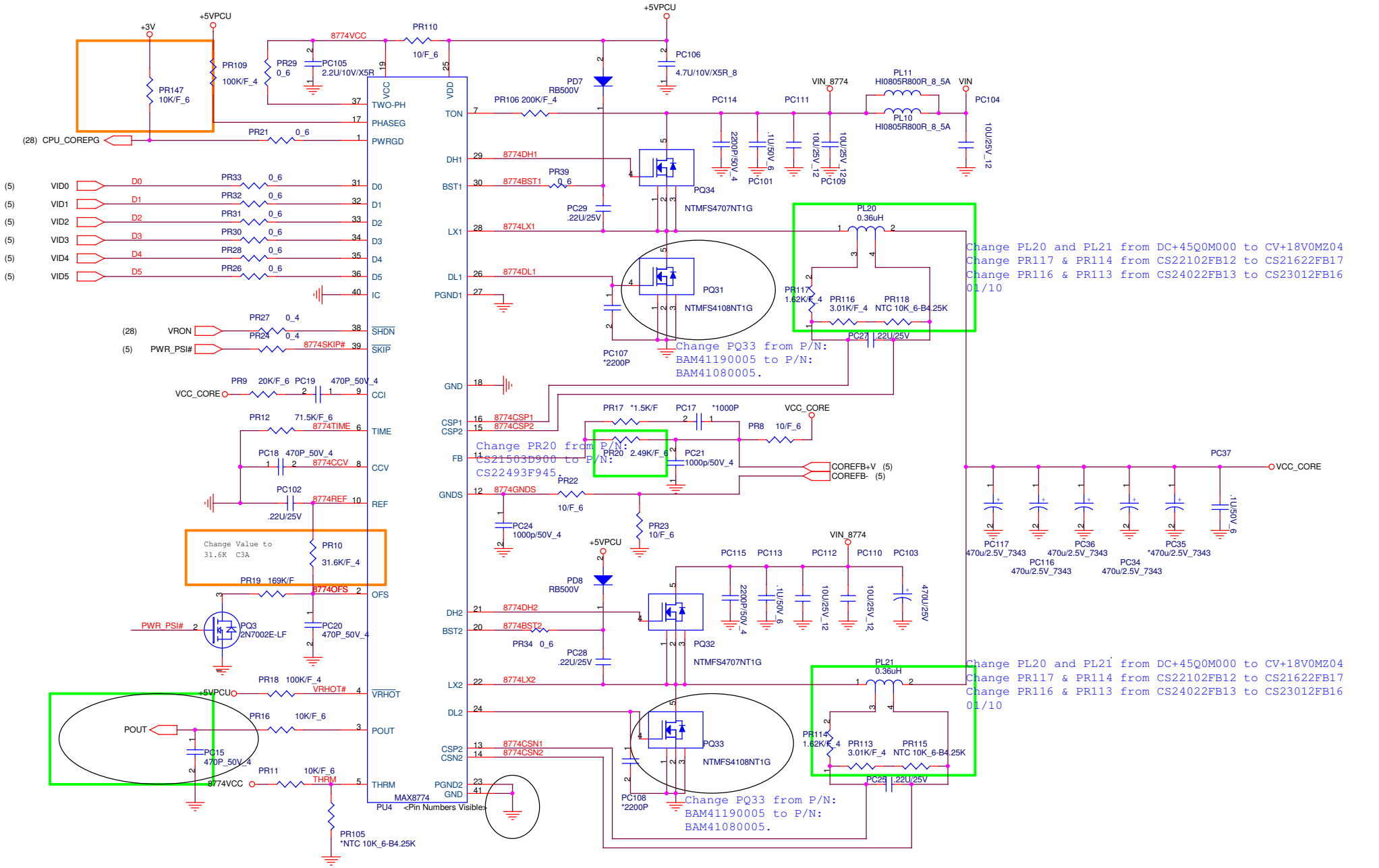

PROJECT : ED5

Quanta Computer Inc.

Size	Document Number	Rev
	CPU CORE MAX8760	2A
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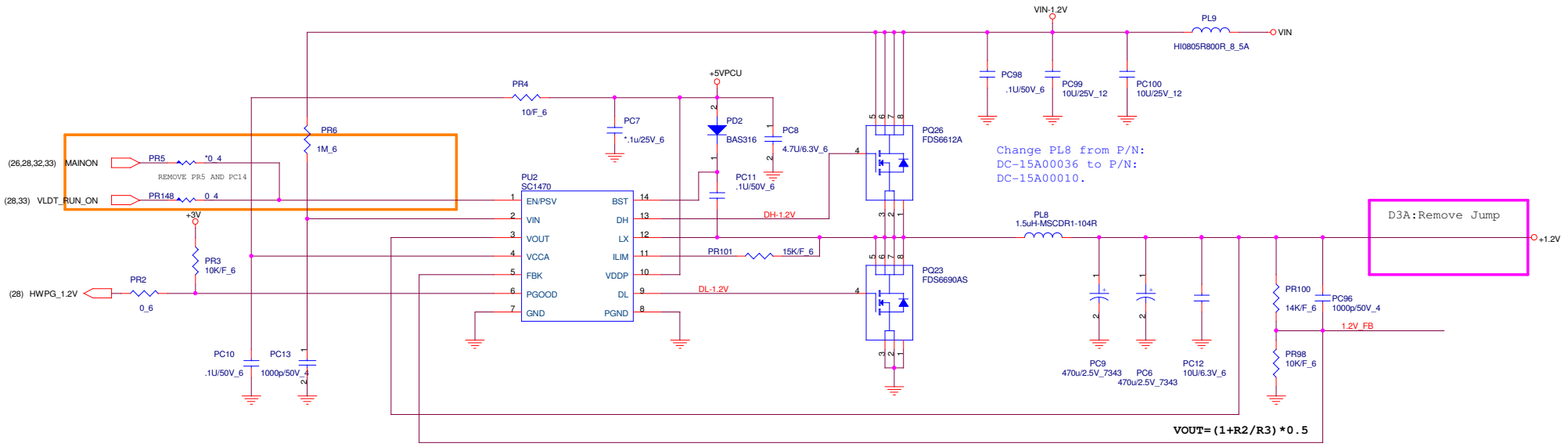
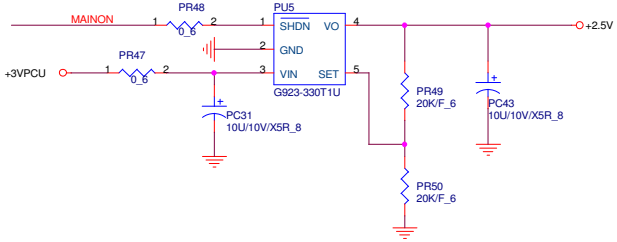
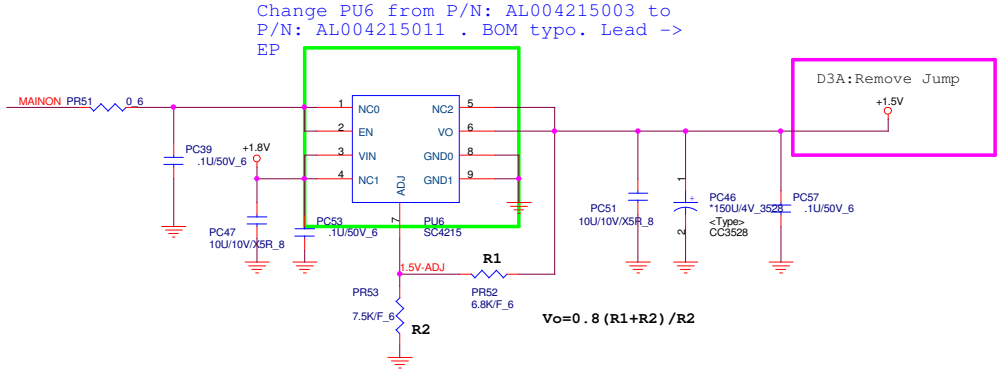


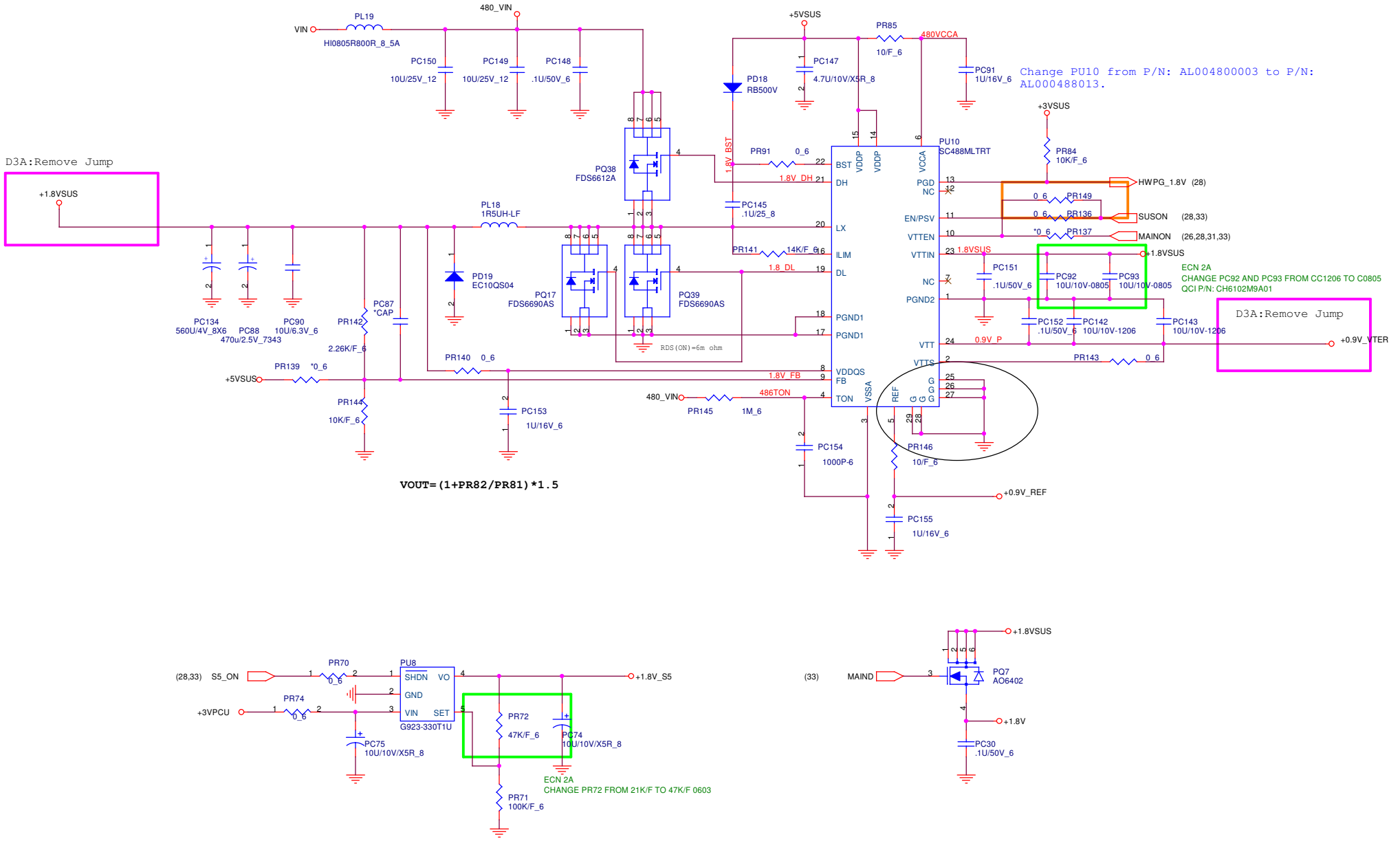




Vout =1.25(1+R1/R2)
= 1.25 (1+20K/20K)
= 2.5V

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.2V & NBRUN	2A
Date: Monday, April 10, 2006	Sheet 31 of 34	



PROJECT : ED5

Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.8V&DDR	2A
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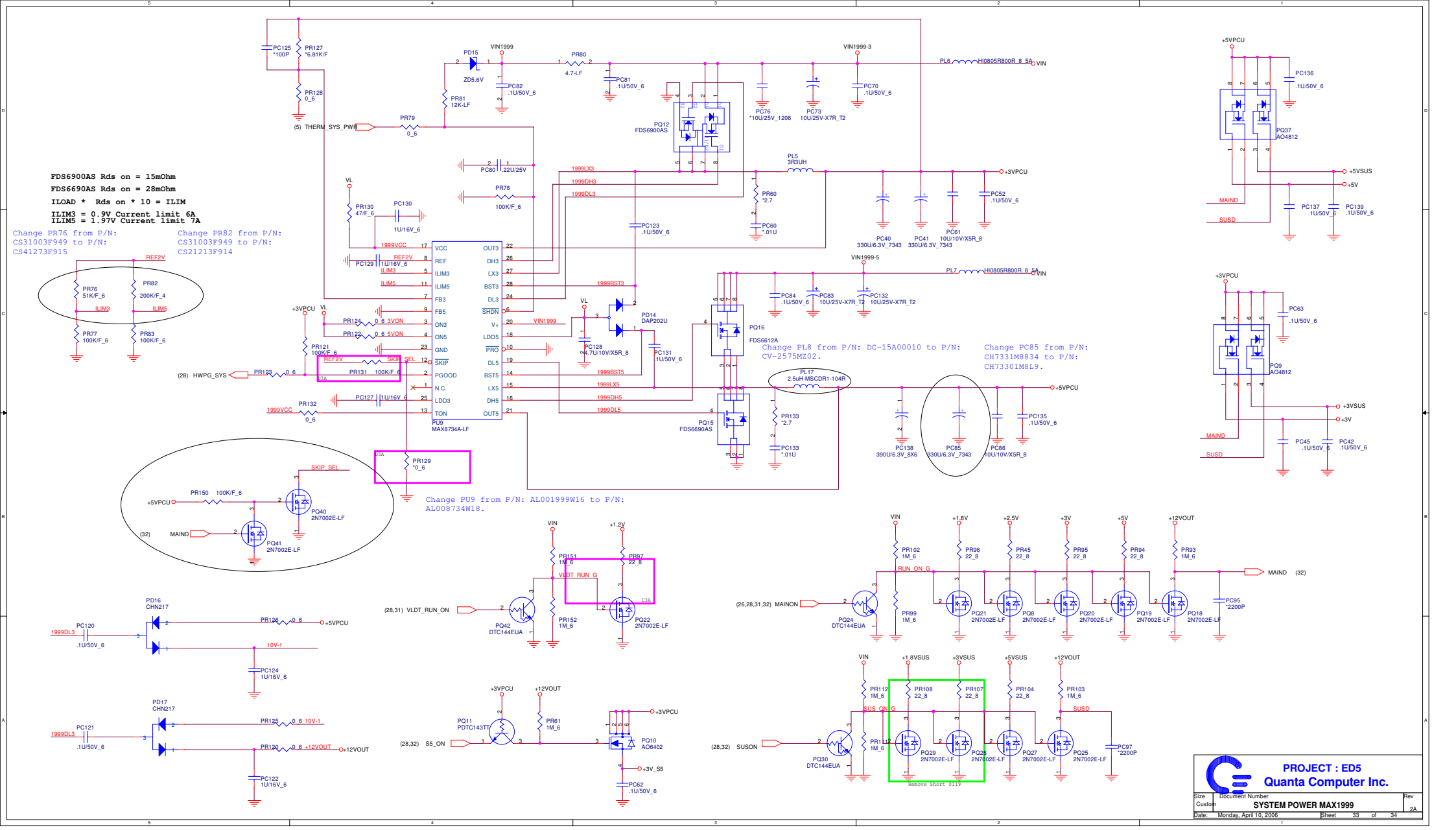
FDS6900AS Rds on = 15mOhm
FDS6690AS Rds on = 28mOhm
ILOAD * Rds on * 10 = ILIM
ILIM3 = 0.9V Current limit 6A
ILIM5 = 1.97V Current limit 7A
Change PR76 from P/N: CS31003F949 to P/N: CS41273F915
Change PR82 from P/N: CS31003F949 to P/N: CS21213F914
Change PL8 from P/N: DC-15A00010 to P/N: CV-2575MZ02.
Change PC85 from P/N: CH7331M8834 to P/N: CH73301M8L9.
Change PU9 from P/N: AL001999W16 to P/N: AL008734W18.
PU9 MAX8734A-LF
PROJECT : ED5
Quanta Computer Inc.
SYSTEM POWER MAX1999
Monday, April 10, 2006
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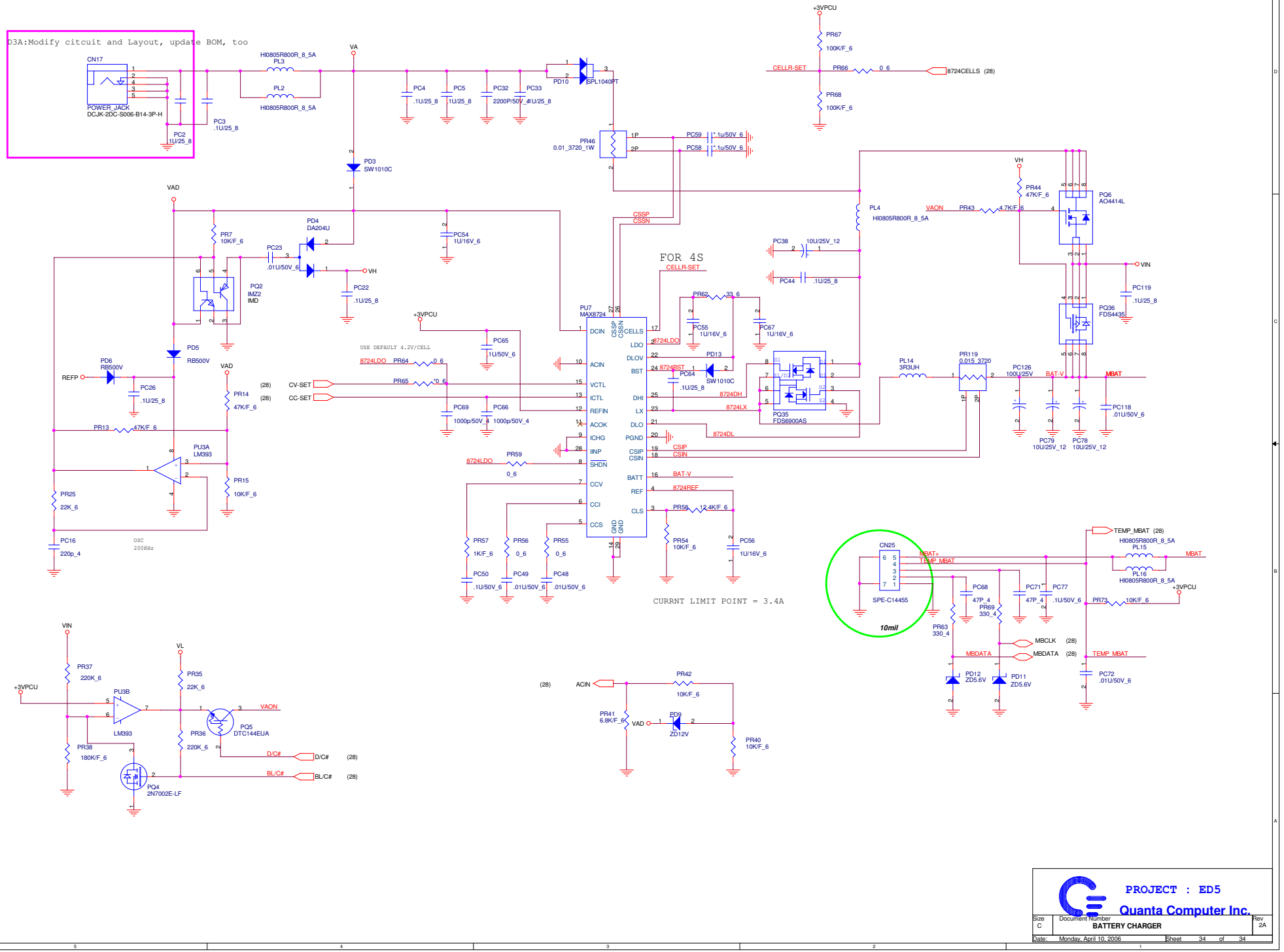
D3A:Modify citcuit and Layout, update BOM, too
CN17
POWER_JACK
DCJK-2DC-S006-B14-3P-H
HI0805R800R_8_5A
PL3
PL2
HI0805R800R_8_5A
VA
PC4 .1U/25_8
PC5 1U/25_8
PC32 2200P/50V_4
PC33 1U/25_8
PC2 1U/25_8
PC3 .1U/25_8
PD10
SPL1040PT
PD3
SW1010C
PR46
0.01_3720_1W
PC59 *.1u/50V_6
PC58 *.1u/50V_6
+3VPCU
PR67
100K/F_6
CELLR-SET
PR66 0_6
8724CELLS (28)
PR68
100K/F_6
VAD
PR7
10K/F_6
PC23
.01U/50V_6
PD4
DA204U
VH
PC22
.1U/25_8
PC54
1U/16V_6
PQ2
IMZ2
IMD
CSSP
CSSN
FOR 4S
CELLR-SET
PC38
10U/25V_12
PC44
.1U/25_8
PL4
HI0805R800R_8_5A
VAON
PR43
4.7K/F_6
VH
PR44
47K/F_6
PQ6
AO4414L
VIN
PC119
.1U/25_8
PQ36
FDS4435
PD5
RB500V
PD6
RB500V
REFP
PC26
.1U/25_8
PR13
47K/F_6
VAD
PR14
47K/F_6
(28) CV-SET
(28) CC-SET
PU3A
LM393
PR25
22K_6
PR15
10K/F_6
PC16
220p_4
OSC
200KHz
USE DEFAULT 4.2V/CELL
8724LDO
PR64 0_6
PR65 *0_6
+3VPCU
PC65
.1U/50V_6
PC69
1000p/50V_4
PC66
1000p/50V_4
PU7
MAX8724
DCIN
ACIN
VCTL
ICTL
REFIN
ACOK
ICHG
IINP
SHDN
CCV
CCI
CCS
CSSP
CSSN
CELLS
LDO
DLOV
BST
DHI
LX
DLO
PGND
CSIP
CSIN
BATT
REF
CLS
GND
PR62 33_6
PC55 1U/16V_6
PC67 1U/16V_6
8724LDO
PD13
8724BST
PC64 .1U/25_8
SW1010C
8724DH
8724LX
PQ35
FDS6900AS
8724DL
PL14
3R3UH
PR119
0.015_3720
PC126
100U/25V
BAT-V
MBAT
PC118
.01U/50V_6
PC79
10U/25V_12
PC78
10U/25V_12
CSIP
CSIN
BAT-V
8724REF
PR58 2.4K/F_6
PR59
0_6
8724LDO
PR57
1K/F_6
PR56
0_6
PR55
0_6
PC50
.1U/50V_6
PC49
.01U/50V_6
PC48
.01U/50V_6
PR54
10K/F_6
PC56
1U/16V_6
CURRNT LIMIT POINT = 3.4A
CN25
SPE-C14455
10mil
MBAT+
TEMP_MBAT
TEMP_MBAT (28)
HI0805R800R_8_5A
PL15
MBAT
PL16
HI0805R800R_8_5A
+3VPCU
PC68
47P_4
PR69
330_4
PC71
47P_4
PC77
.1U/50V_6
PR73
10K/F_6
PR63
330_4
MBCLK (28)
MBDATA (28)
MBDATA
TEMP_MBAT
PD12
ZD5.6V
PD11
ZD5.6V
PC72
.01U/50V_6
VIN
PR37
220K_6
+3VPCU
PU3B
LM393
PR38
180K/F_6
VL
PR35
22K_6
PR36
220K_6
PQ5
DTC144EUA
VAON
D/C#
D/C# (28)
BL/C#
BL/C# (28)
PQ4
2N7002E-LF
(28) ACIN
PR42
10K/F_6
PR41
6.8K/F_6
VAD
PD9
ZD12V
PR40
10K/F_6
PROJECT : ED5
Quanta Computer Inc.
Size C
Document Number
BATTERY CHARGER
Rev 2A
Date: Monday, April 10, 2006
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