CHELSEA DJ2 CP UMA Schematics Document

Arrandale

Intel PCH

2010-05-18

REV : A00

```
   DY : Nopop Component
 HDMI : Pop for HDMI function
 GIGA : Pop for GIGA LAN
10/100 : Pop for 10/100 LAN
65 BOM : Nopop for 65 BOM option
```

for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Cover Page		
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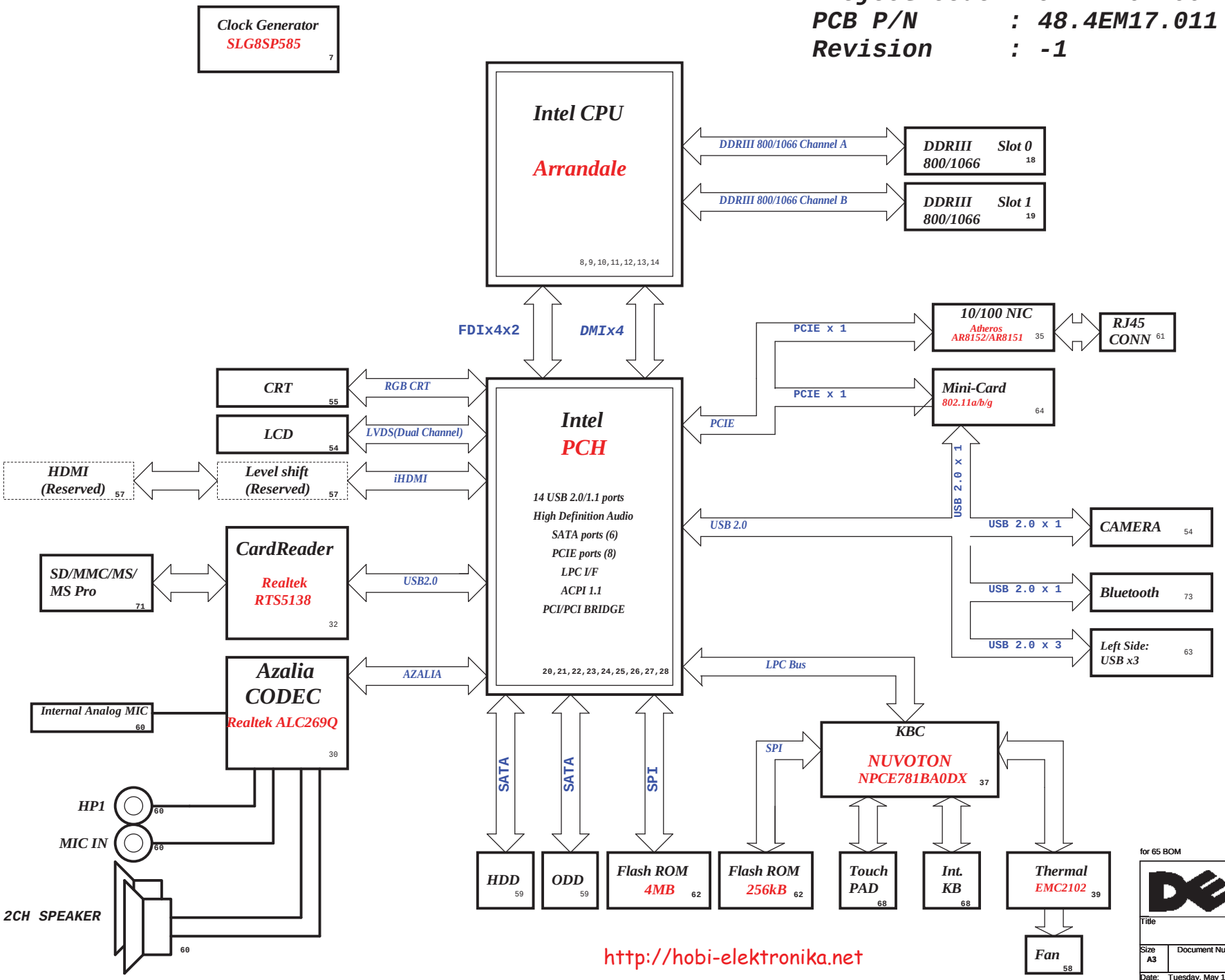
CHELSEA DJ2 CP UMA Block Diagram

Project code : 91.4EM01.001
PCB P/N : 48.4EM17.011
Revision : -1



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CPU DC/DC ISL62882	
INPUTS	
+PWR_SRC	

SYSTEM DC/DC TPS51218	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM DC/DC RT8205BGQW 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW

SYSTEM DC/DC RT8207GQW 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC APL5930KAI 90	
INPUTS	OUTPUTS
+1.5V_SUS	+1.1V_RUN

VGA RT8208BGQW 86	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE

MAXIM CHARGER BQ24745	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN +1.8V_DELAY

SYSTEM DC/DC Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN

PCB LAYER
L1: Top
L2: GND
L3: Signal
L4: Signal
L5 VCC
L6: Bottom

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Title: Block Diagram

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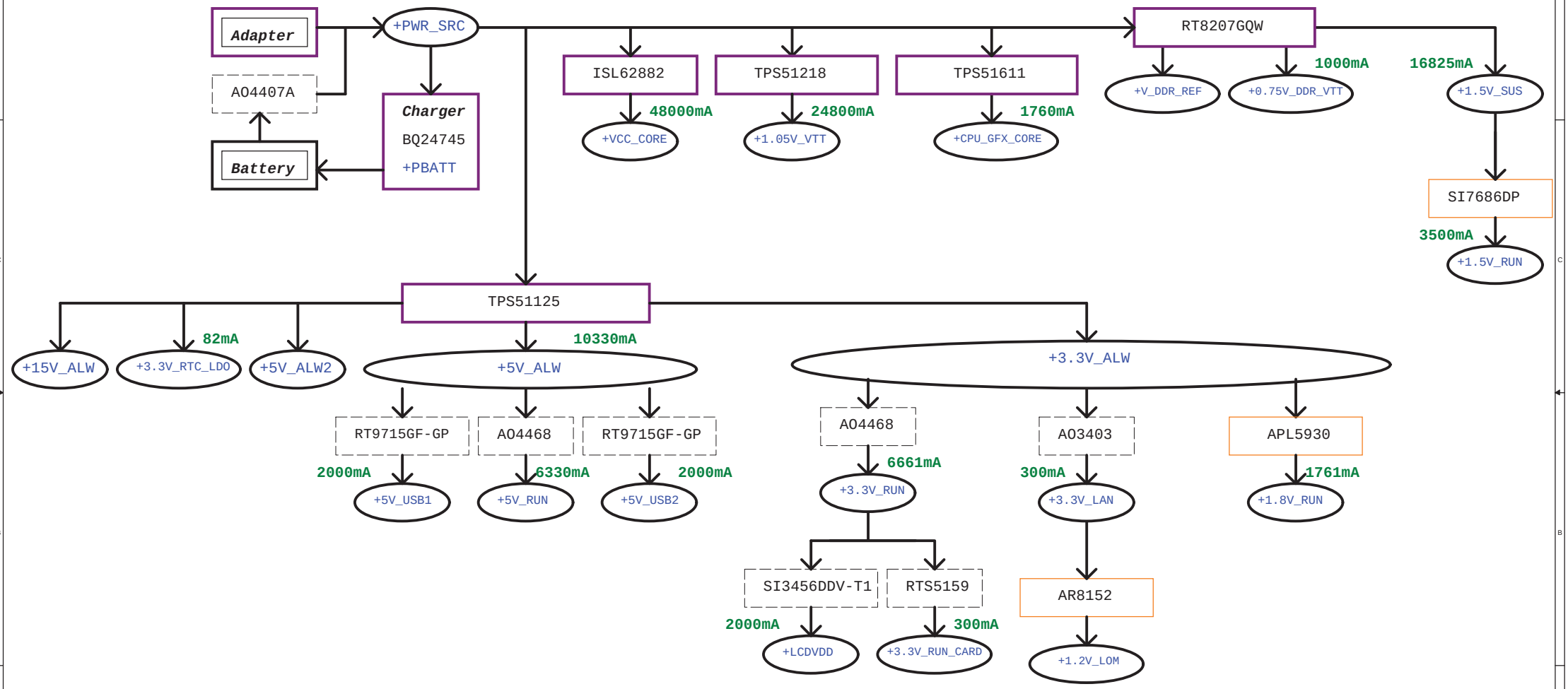

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Title: Power Block Diagram

Size	Document Number	Rev
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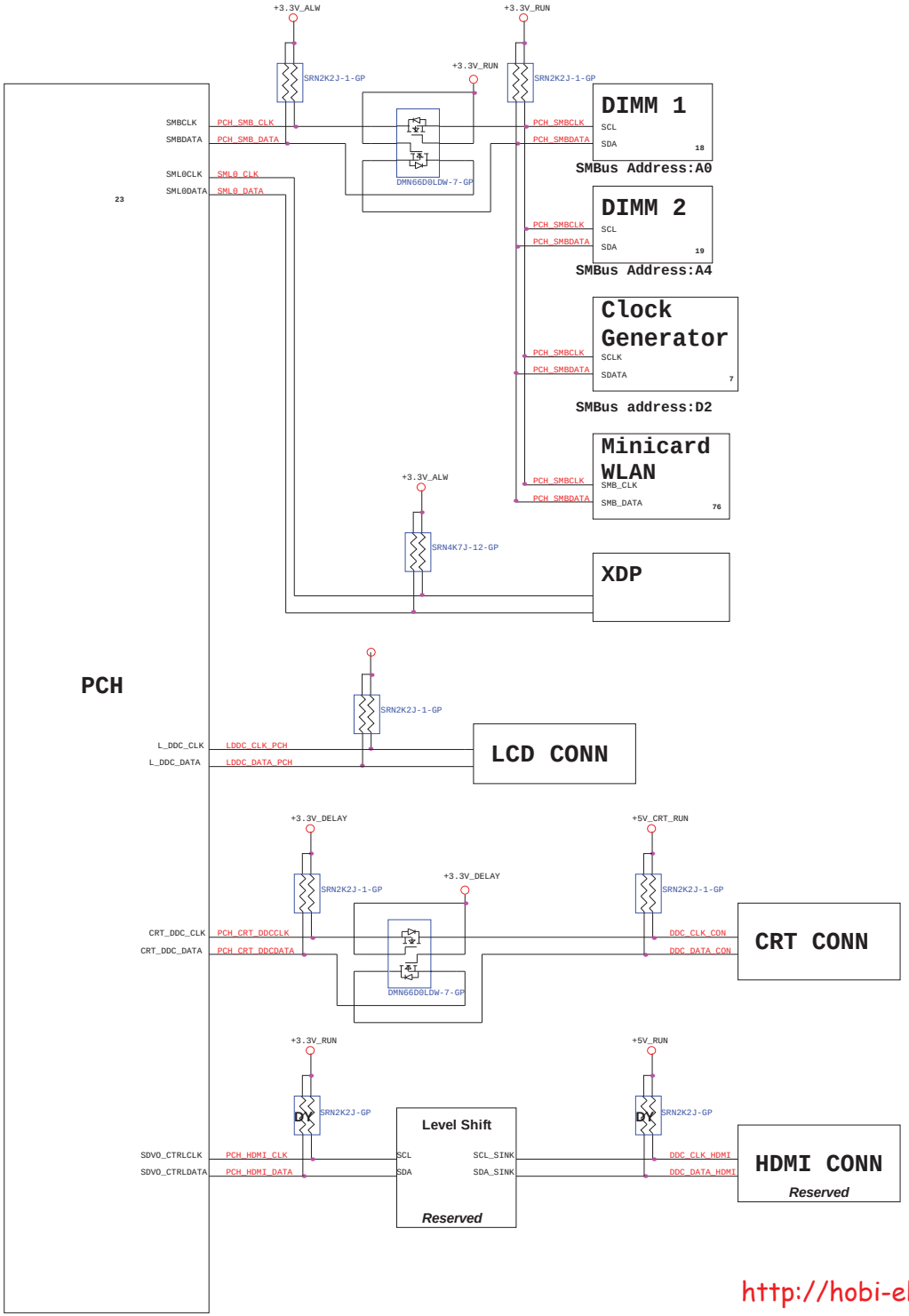
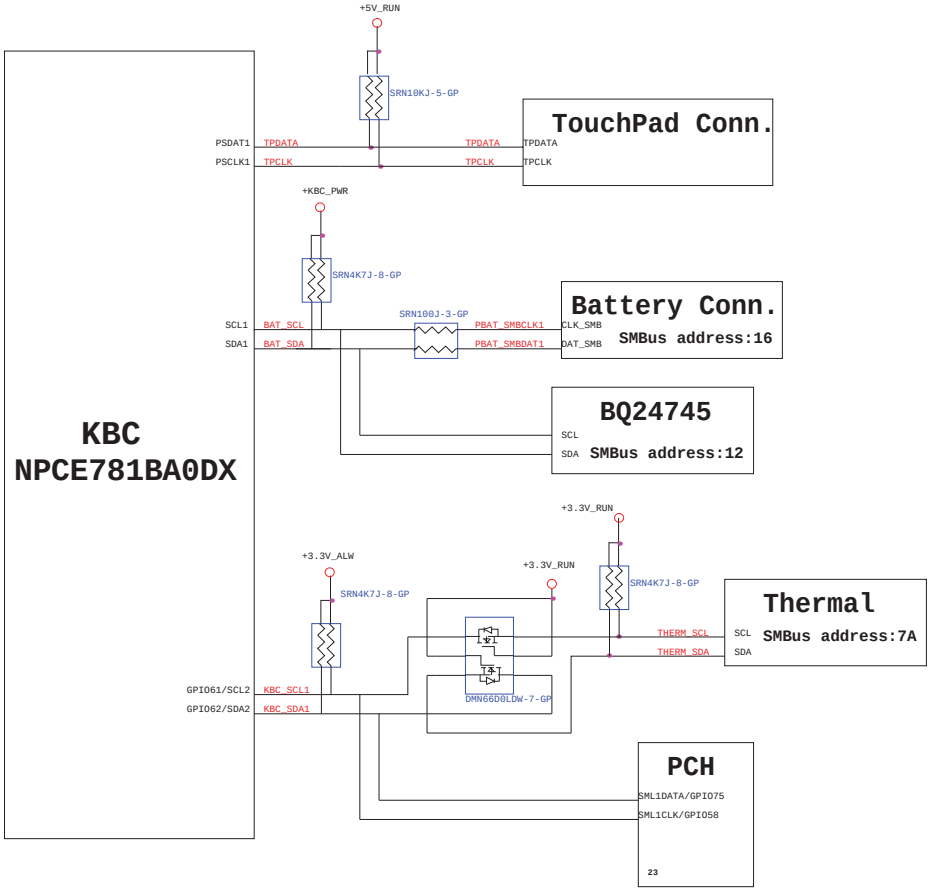
PCH SMBus Block Diagram



KBC SMBus Block Diagram



for 65 BOM

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Title: SMBUS Block Diagram

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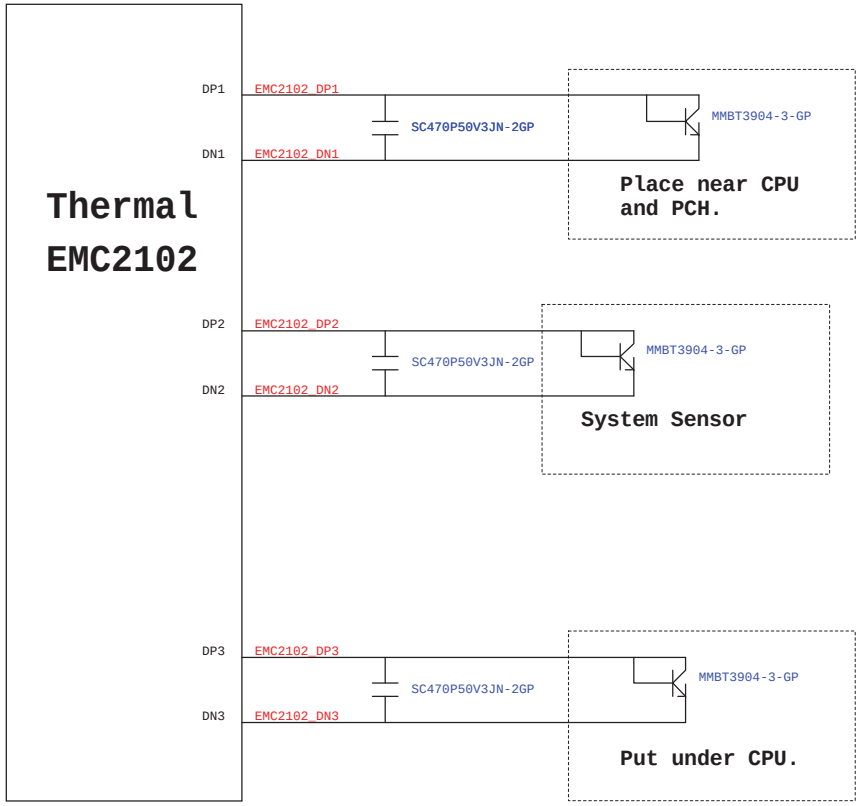
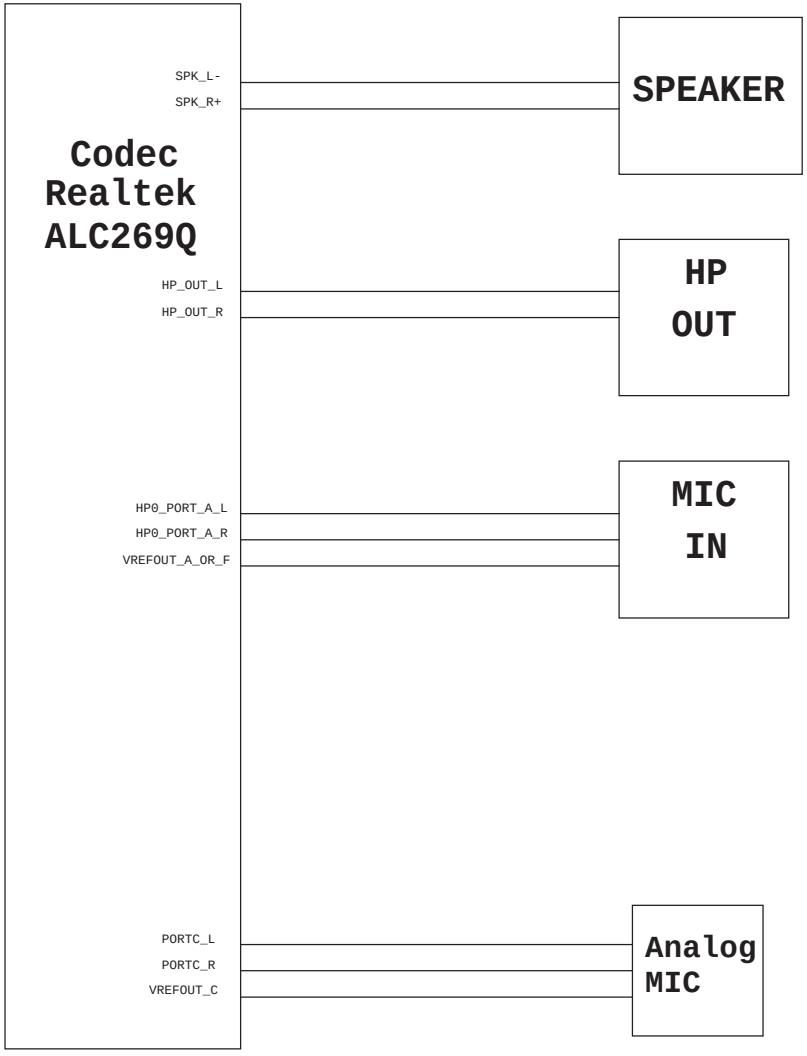
Thermal Block Diagram



Audio Block Diagram



for 65 BOM

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Title: Thermal/Audio Block Diagram		
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PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#/GPIO51	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN

USB Table

USB	
Pair	Device
0	USB0
1	X
2	USB2
3	USB3
4	X
5	WLAN
6	X
7	X
8	X
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X

for 65 BOM

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Title: Table of Content

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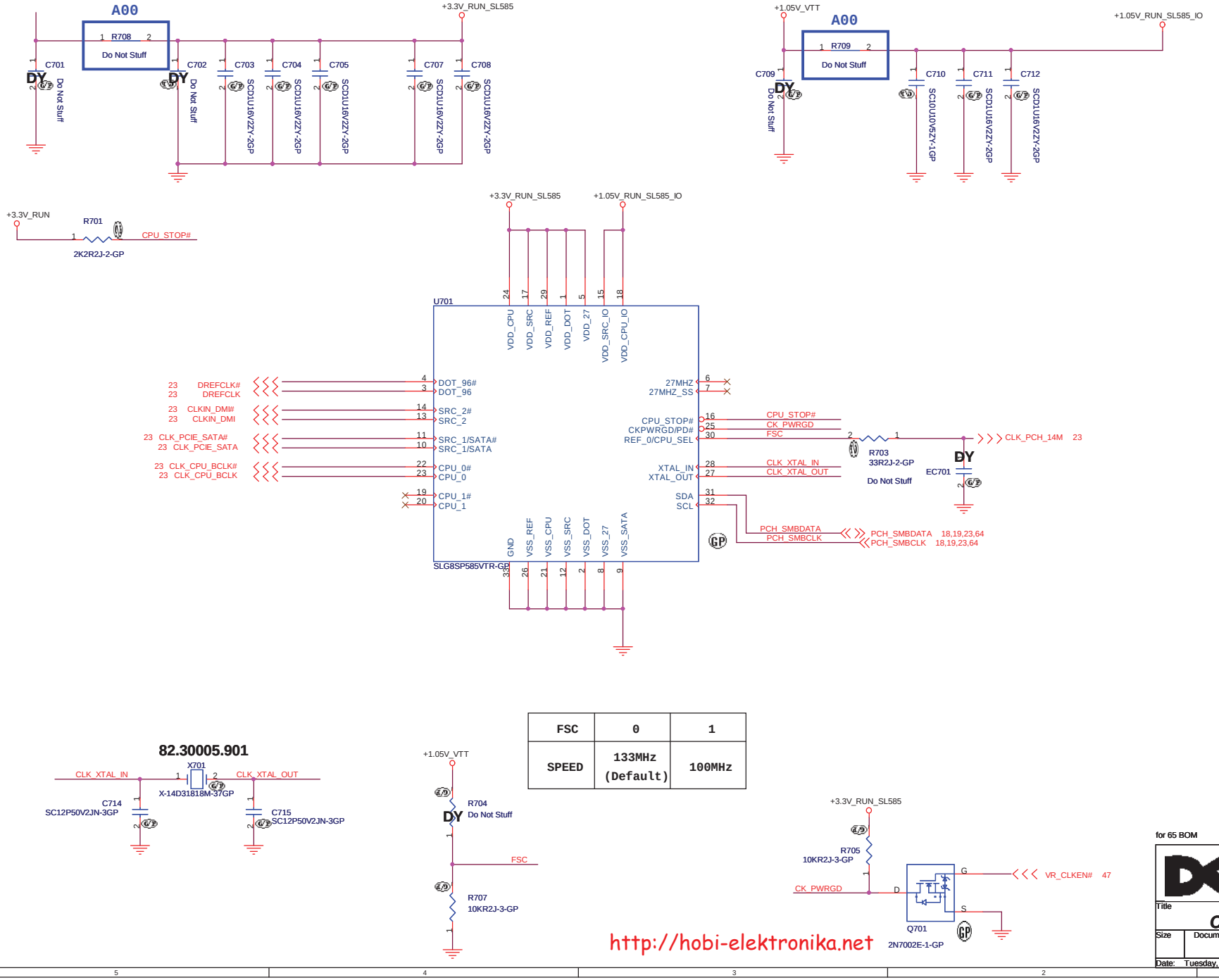
SSID = CLOCK



FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title	Clock Generator SLG8SP585	
Size	Document Number: DJ2 CP UMA	Rev: A00
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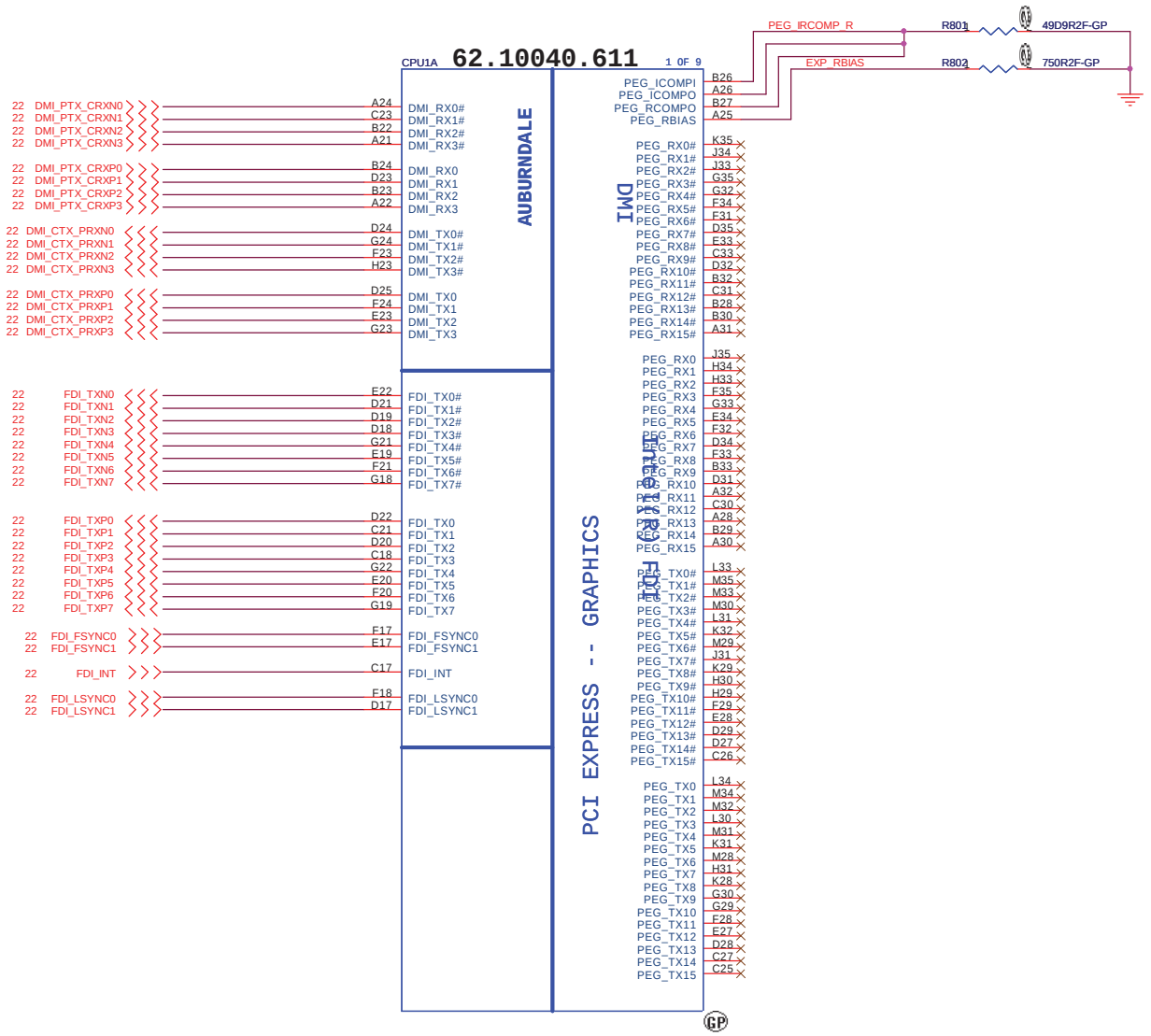
SSID = CPU



for 65 BOM

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Title: CPU (PCIE/DMI/FDI)

Size	Document Number	Rev
	DJ2 CP UMA	A00

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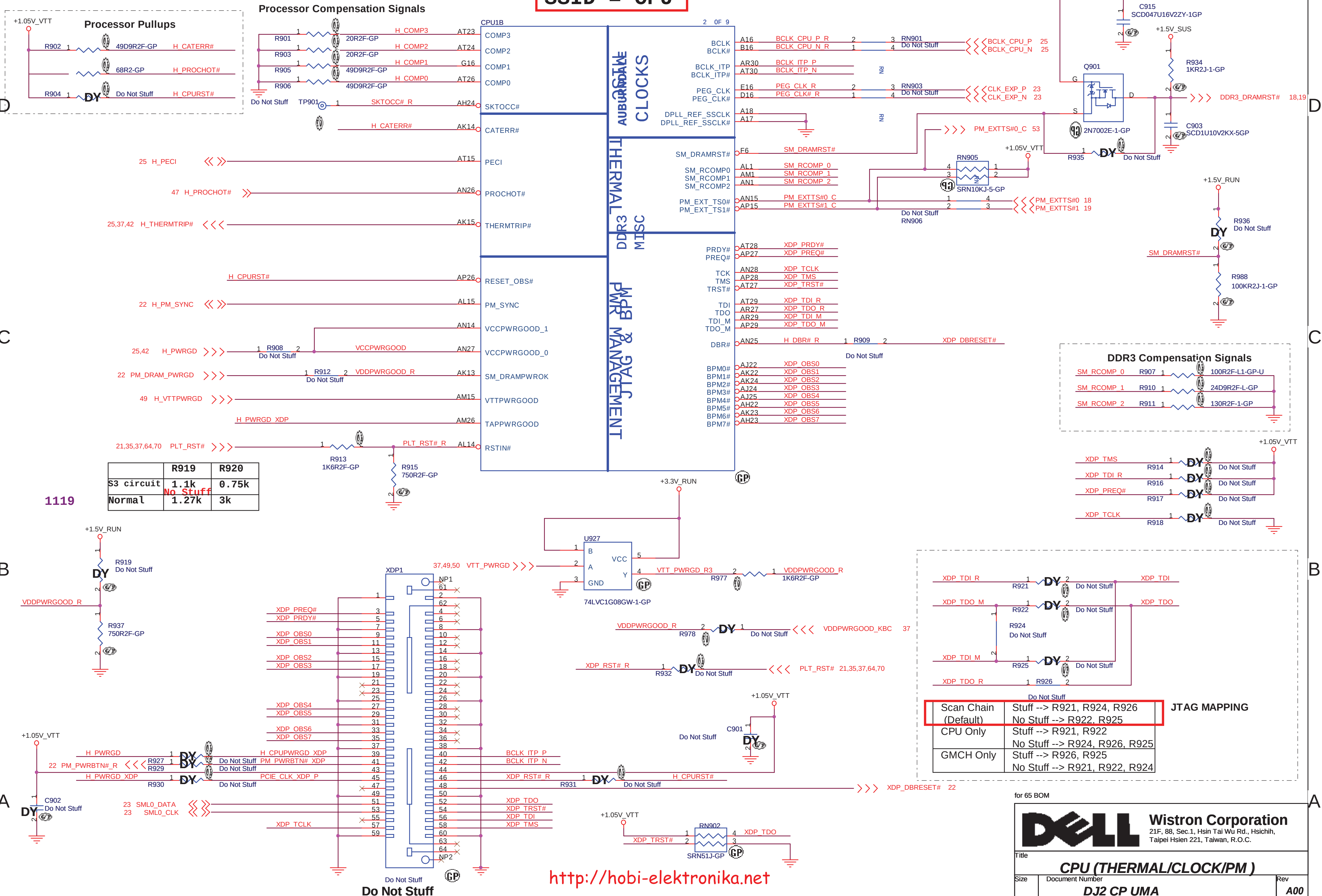
SSID = CPU



Processor Pullups
Processor Compensation Signals
+1.05V_VTT
R902 49D9R2F-GP H_CATERR#
68R2-GP H_PROCHOT#
R904 DY Do Not Stuff H_CPURST#
R901 20R2F-GP H_COMP3
R903 20R2F-GP H_COMP2
R905 49D9R2F-GP H_COMP1
R906 49D9R2F-GP H_COMP0
Do Not Stuff
TP901 SKTOCC#_R
H_CATERR#
CPU1B
2 OF 9
COMP3
COMP2
COMP1
COMP0
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
RESET_OBS#
PM_SYNC
VCCPWRGOOD_1
VCCPWRGOOD_0
SM_DRAMPWROK
VTTPWRGOOD
TAPPWRGOOD
RSTIN#
MISC
THERMAL
PWR MANAGEMENT
CLOCKS
DDR3 MISC
JTAG & BPM
BCLK
BCLK#
BCLK_ITP
BCLK_ITP#
PEG_CLK
PEG_CLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
SM_DRAMRST#
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
PM_EXT_TS0#
PM_EXT_TS1#
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
TDI_M
TDO_M
DBR#
BPM0#
BPM1#
BPM2#
BPM3#
BPM4#
BPM5#
BPM6#
BPM7#
25 H_PECI
47 H_PROCHOT#
25,37,42 H_THERMTRIP#
H_CPURST#
22 H_PM_SYNC
25,42 H_PWRGD
R908 Do Not Stuff
VCCPWRGOOD
22 PM_DRAM_PWRGD
R912 Do Not Stuff
VDDPWRGOOD_R
49 H_VTTPWRGD
H_PWRGD_XDP
21,35,37,64,70 PLT_RST#
R913 1K6R2F-GP
PLT_RST#_R
R915 750R2F-GP
BCLK_CPU_P_R
BCLK_CPU_N_R
RN901 Do Not Stuff
BCLK_CPU_P 25
BCLK_CPU_N 25
BCLK_ITP_P
BCLK_ITP_N
PEG_CLK_R
PEG_CLK#_R
RN903 Do Not Stuff
CLK_EXP_P 23
CLK_EXP_N 23
DDR_RST_GATE 25
C915 SCD047U16V2ZY-1GP
+1.5V_SUS
Q901
2N7002E-1-GP
R934 1KR2J-1-GP
DDR3_DRAMRST# 18,19
C903 SCD1U10V2KX-5GP
PM_EXTTS#0_C 53
+1.05V_VTT
R935 DY Do Not Stuff
SM_DRAMRST#
SM_RCOMP_0
SM_RCOMP_1
SM_RCOMP_2
RN905
SRN10KJ-5-GP
PM_EXTTS#0_C
PM_EXTTS#1_C
PM_EXTTS#0 18
PM_EXTTS#1 19
Do Not Stuff
RN906
+1.5V_RUN
R936 Do Not Stuff
SM_DRAMRST#
R988 100KR2J-1-GP
XDP_PRDY#
XDP_PREQ#
XDP_TCLK
XDP_TMS
XDP_TRST#
XDP_TDI_R
XDP_TDO_R
XDP_TDI_M
XDP_TDO_M
H_DBR#_R
R909 Do Not Stuff
XDP_DBRESET#
XDP_OBS0
XDP_OBS1
XDP_OBS2
XDP_OBS3
XDP_OBS4
XDP_OBS5
XDP_OBS6
XDP_OBS7
DDR3 Compensation Signals
SM_RCOMP_0 R907 100R2F-L1-GP-U
SM_RCOMP_1 R910 24D9R2F-L-GP
SM_RCOMP_2 R911 130R2F-1-GP
+1.05V_VTT
XDP_TMS R914 DY Do Not Stuff
XDP_TDI_R R916 DY Do Not Stuff
XDP_PREQ# R917 DY Do Not Stuff
XDP_TCLK R918 DY Do Not Stuff
+3.3V_RUN
U927
74LVC1G08GW-1-GP
37,49,50 VTT_PWRGD
VTT_PWRGD_R3
R977 1K6R2F-GP
VDDPWRGOOD_R
VDDPWRGOOD_R R978 DY Do Not Stuff VDDPWRGOOD_KBC 37
XDP_RST#_R R932 DY Do Not Stuff PLT_RST# 21,35,37,64,70
+1.05V_VTT
C901 DY Do Not Stuff
+1.5V_RUN
R919 DY Do Not Stuff
VDDPWRGOOD_R
R937 750R2F-GP
+1.05V_VTT
H_PWRGD R927
22 PM_PWRBTN#_R R929
H_PWRGD_XDP R930
H_CPUPWRGD_XDP
PM_PWRBTN#_XDP
PCIE_CLK_XDP_P
Do Not Stuff
C902 DY Do Not Stuff
23 SML0_DATA
23 SML0_CLK
XDP_TCLK
XDP1
XDP_PREQ#
XDP_PRDY#
XDP_OBS0
XDP_OBS1
XDP_OBS2
XDP_OBS3
XDP_OBS4
XDP_OBS5
XDP_OBS6
XDP_OBS7
BCLK_ITP_P
BCLK_ITP_N
XDP_RST#_R
R931 DY Do Not Stuff
H_CPURST#
XDP_DBRESET# 22
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS
Do Not Stuff
+1.05V_VTT
RN902
SRN51J-GP
XDP_TRST#
XDP_TDO
XDP_TDI_R R921 DY Do Not Stuff XDP_TDI
XDP_TDO_M R922 DY Do Not Stuff XDP_TDO
R924 Do Not Stuff
XDP_TDI_M R925 DY Do Not Stuff
XDP_TDO_R R926 Do Not Stuff
JTAG MAPPING

	R919	R920
S3 circuit	1.1k No Stuff	0.75k
Normal	1.27k	3k

1119

Scan Chain (Default)	Stuff --> R921, R924, R926 No Stuff --> R922, R925
CPU Only	Stuff --> R921, R922 No Stuff --> R924, R926, R925
GMCH Only	Stuff --> R926, R925 No Stuff --> R921, R922, R924

Do Not Stuff

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for 65 BOM

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Title: CPU (THERMAL/CLOCK/PM)

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SSID = CPU

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AUBURNDALE

DDR SYSTEM MEMORY A

18 M_A_DQ[63..0]

M_A_DQ0 A10 SA_DQ0
M_A_DQ1 C10 SA_DQ1
M_A_DQ2 C7 SA_DQ2
M_A_DQ3 A7 SA_DQ3
M_A_DQ4 B10 SA_DQ4
M_A_DQ5 D10 SA_DQ5
M_A_DQ6 E10 SA_DQ6
M_A_DQ7 A8 SA_DQ7
M_A_DQ8 D8 SA_DQ8
M_A_DQ9 F10 SA_DQ9
M_A_DQ10 E6 SA_DQ10
M_A_DQ11 F7 SA_DQ11
M_A_DQ12 E9 SA_DQ12
M_A_DQ13 B7 SA_DQ13
M_A_DQ14 E7 SA_DQ14
M_A_DQ15 C6 SA_DQ15
M_A_DQ16 H10 SA_DQ16
M_A_DQ17 G8 SA_DQ17
M_A_DQ18 K7 SA_DQ18
M_A_DQ19 J8 SA_DQ19
M_A_DQ20 G7 SA_DQ20
M_A_DQ21 G10 SA_DQ21
M_A_DQ22 J7 SA_DQ22
M_A_DQ23 J10 SA_DQ23
M_A_DQ24 L7 SA_DQ24
M_A_DQ25 M6 SA_DQ25
M_A_DQ26 M8 SA_DQ26
M_A_DQ27 L9 SA_DQ27
M_A_DQ28 L6 SA_DQ28
M_A_DQ29 K8 SA_DQ29
M_A_DQ30 N8 SA_DQ30
M_A_DQ31 P9 SA_DQ31
M_A_DQ32 AH5 SA_DQ32
M_A_DQ33 AE5 SA_DQ33
M_A_DQ34 AK6 SA_DQ34
M_A_DQ35 AK7 SA_DQ35
M_A_DQ36 AF6 SA_DQ36
M_A_DQ37 AG5 SA_DQ37
M_A_DQ38 AJ7 SA_DQ38
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M_A_DQ40 AJ10 SA_DQ40
M_A_DQ41 AJ9 SA_DQ41
M_A_DQ42 AL10 SA_DQ42
M_A_DQ43 AK12 SA_DQ43
M_A_DQ44 AK8 SA_DQ44
M_A_DQ45 AL7 SA_DQ45
M_A_DQ46 AK11 SA_DQ46
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M_A_DQ53 AN9 SA_DQ53
M_A_DQ54 AT11 SA_DQ54
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M_A_DQ60 AT12 SA_DQ60
M_A_DQ61 AL13 SA_DQ61
M_A_DQ62 AR14 SA_DQ62
M_A_DQ63 AP14 SA_DQ63

18 M_A_BS0 AC3 SA_BS0
18 M_A_BS1 AB2 SA_BS1
18 M_A_BS2 U7 SA_BS2

18 M_A_CAS# AE1 SA_CAS#
18 M_A_RAS# AB3 SA_RAS#
18 M_A_WE# AE9 SA_WE#

SA_CK0 AA6 M_CLK_DDR0 18
SA_CK0# AA7 M_CLK_DDR#0 18
SA_CKE0 P7 M_CKE0 18

SA_CK1 Y6 M_CLK_DDR1 18
SA_CK1# Y5 M_CLK_DDR#1 18
SA_CKE1 P6 M_CKE1 18

SA_CS0# AE2 M_CS#0 18
SA_CS1# AE8 M_CS#1 18

SA_ODT0 AD8 M_ODT0 18
SA_ODT1 AF9 M_ODT1 18

SA_DM0 B9 M_A_DM0
SA_DM1 D7 M_A_DM1
SA_DM2 H7 M_A_DM2
SA_DM3 M7 M_A_DM3
SA_DM4 AG6 M_A_DM4
SA_DM5 AM7 M_A_DM5
SA_DM6 AN10 M_A_DM6
SA_DM7 AN13 M_A_DM7

M_A_DM[7..0] 18
M_A_DQS#[7..0] 18
M_A_DQS[7..0] 18
M_A_A[15..0] 18

SA_DQS0# C9 M_A_DQS#0
SA_DQS1# F8 M_A_DQS#1
SA_DQS2# J9 M_A_DQS#2
SA_DQS3# N9 M_A_DQS#3
SA_DQS4# AH7 M_A_DQS#4
SA_DQS5# AK9 M_A_DQS#5
SA_DQS6# AP11 M_A_DQS#6
SA_DQS7# AT13 M_A_DQS#7

SA_DQS0 C8 M_A_DQS0
SA_DQS1 F9 M_A_DQS1
SA_DQS2 H9 M_A_DQS2
SA_DQS3 M9 M_A_DQS3
SA_DQS4 AH8 M_A_DQS4
SA_DQS5 AK10 M_A_DQS5
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SA_DQS7 AR13 M_A_DQS7

SA_MA0 Y3 M_A_A0
SA_MA1 W1 M_A_A1
SA_MA2 AA8 M_A_A2
SA_MA3 AA3 M_A_A3
SA_MA4 V1 M_A_A4
SA_MA5 AA9 M_A_A5
SA_MA6 V8 M_A_A6
SA_MA7 T1 M_A_A7
SA_MA8 Y9 M_A_A8
SA_MA9 U6 M_A_A9
SA_MA10 AD4 M_A_A10
SA_MA11 T2 M_A_A11
SA_MA12 U3 M_A_A12
SA_MA13 AG8 M_A_A13
SA_MA14 T3 M_A_A14
SA_MA15 V9 M_A_A15

19 M_B_DQ[63..0]

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AUBURNDALE

DDR SYSTEM MEMORY - B

M_B_DQ0 B5 SB_DQ0
M_B_DQ1 A5 SB_DQ1
M_B_DQ2 C3 SB_DQ2
M_B_DQ3 B3 SB_DQ3
M_B_DQ4 E4 SB_DQ4
M_B_DQ5 A6 SB_DQ5
M_B_DQ6 A4 SB_DQ6
M_B_DQ7 C4 SB_DQ7
M_B_DQ8 D1 SB_DQ8
M_B_DQ9 D2 SB_DQ9
M_B_DQ10 E2 SB_DQ10
M_B_DQ11 F1 SB_DQ11
M_B_DQ12 C2 SB_DQ12
M_B_DQ13 E5 SB_DQ13
M_B_DQ14 F3 SB_DQ14
M_B_DQ15 G4 SB_DQ15
M_B_DQ16 H6 SB_DQ16
M_B_DQ17 G2 SB_DQ17
M_B_DQ18 J6 SB_DQ18
M_B_DQ19 J3 SB_DQ19
M_B_DQ20 G1 SB_DQ20
M_B_DQ21 G5 SB_DQ21
M_B_DQ22 J2 SB_DQ22
M_B_DQ23 J1 SB_DQ23
M_B_DQ24 J5 SB_DQ24
M_B_DQ25 K2 SB_DQ25
M_B_DQ26 L3 SB_DQ26
M_B_DQ27 M1 SB_DQ27
M_B_DQ28 K5 SB_DQ28
M_B_DQ29 K4 SB_DQ29
M_B_DQ30 M4 SB_DQ30
M_B_DQ31 N5 SB_DQ31
M_B_DQ32 AF3 SB_DQ32
M_B_DQ33 AG1 SB_DQ33
M_B_DQ34 AJ3 SB_DQ34
M_B_DQ35 AK1 SB_DQ35
M_B_DQ36 AG4 SB_DQ36
M_B_DQ37 AG3 SB_DQ37
M_B_DQ38 AJ4 SB_DQ38
M_B_DQ39 AH4 SB_DQ39
M_B_DQ40 AK3 SB_DQ40
M_B_DQ41 AK4 SB_DQ41
M_B_DQ42 AM6 SB_DQ42
M_B_DQ43 AN2 SB_DQ43
M_B_DQ44 AK5 SB_DQ44
M_B_DQ45 AK2 SB_DQ45
M_B_DQ46 AM4 SB_DQ46
M_B_DQ47 AM3 SB_DQ47
M_B_DQ48 AP3 SB_DQ48
M_B_DQ49 AN5 SB_DQ49
M_B_DQ50 AT4 SB_DQ50
M_B_DQ51 AN6 SB_DQ51
M_B_DQ52 AN4 SB_DQ52
M_B_DQ53 AN3 SB_DQ53
M_B_DQ54 AT5 SB_DQ54
M_B_DQ55 AT6 SB_DQ55
M_B_DQ56 AM7 SB_DQ56
M_B_DQ57 AP6 SB_DQ57
M_B_DQ58 AP8 SB_DQ58
M_B_DQ59 AT9 SB_DQ59
M_B_DQ60 AT7 SB_DQ60
M_B_DQ61 AP9 SB_DQ61
M_B_DQ62 AR10 SB_DQ62
M_B_DQ63 AT10 SB_DQ63

19 M_B_BS0 AB1 SB_BS0
19 M_B_BS1 W5 SB_BS1
19 M_B_BS2 R7 SB_BS2

19 M_B_CAS# AC5 SB_CAS#
19 M_B_RAS# Y7 SB_RAS#
19 M_B_WE# AC6 SB_WE#

SB_CK0 W8 M_CLK_DDR2 19
SB_CK0# W9 M_CLK_DDR#2 19
SB_CKE0 M3 M_CKE2 19

SB_CK1 V7 M_CLK_DDR3 19
SB_CK1# V6 M_CLK_DDR#3 19
SB_CKE1 M2 M_CKE3 19

SB_CS0# AB8 M_CS#2 19
SB_CS1# AD6 M_CS#3 19

SB_ODT0 AC7 M_ODT2 19
SB_ODT1 AD1 M_ODT3 19

SB_DM0 D4 M_B_DM0
SB_DM1 E1 M_B_DM1
SB_DM2 H3 M_B_DM2
SB_DM3 K1 M_B_DM3
SB_DM4 AH1 M_B_DM4
SB_DM5 AL2 M_B_DM5
SB_DM6 AR4 M_B_DM6
SB_DM7 AT8 M_B_DM7

M_B_DM[7..0] 19
M_B_DQS#[7..0] 19
M_B_DQS[7..0] 19
M_B_A[15..0] 19

SB_DQS0# D5 M_B_DQS#0
SB_DQS1# F4 M_B_DQS#1
SB_DQS2# J4 M_B_DQS#2
SB_DQS3# L4 M_B_DQS#3
SB_DQS4# AH2 M_B_DQS#4
SB_DQS5# AL4 M_B_DQS#5
SB_DQS6# AR5 M_B_DQS#6
SB_DQS7# AR8 M_B_DQS#7

SB_DQS0 C5 M_B_DQS0
SB_DQS1 E3 M_B_DQS1
SB_DQS2 H4 M_B_DQS2
SB_DQS3 M5 M_B_DQS3
SB_DQS4 AG2 M_B_DQS4
SB_DQS5 AL5 M_B_DQS5
SB_DQS6 AP5 M_B_DQS6
SB_DQS7 AR7 M_B_DQS7

SB_MA0 U5 M_B_A0
SB_MA1 V2 M_B_A1
SB_MA2 T5 M_B_A2
SB_MA3 V3 M_B_A3
SB_MA4 R1 M_B_A4
SB_MA5 T8 M_B_A5
SB_MA6 R2 M_B_A6
SB_MA7 R6 M_B_A7
SB_MA8 R4 M_B_A8
SB_MA9 R5 M_B_A9
SB_MA10 AB5 M_B_A10
SB_MA11 P3 M_B_A11
SB_MA12 R3 M_B_A12
SB_MA13 AF7 M_B_A13
SB_MA14 P5 M_B_A14
SB_MA15 N1 M_B_A15

for 65 BOM

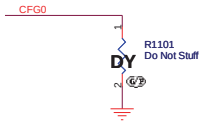
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR)

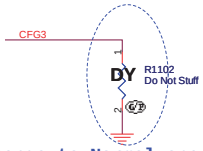
Size | Document Number: DJ2 CP UMA | Rev: A00

Date: Tuesday, May 18, 2010 Sheet 10 of 95

SSID = CPU

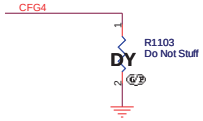


PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

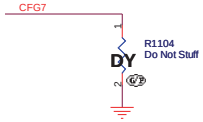


Change to Normal operation
20100202

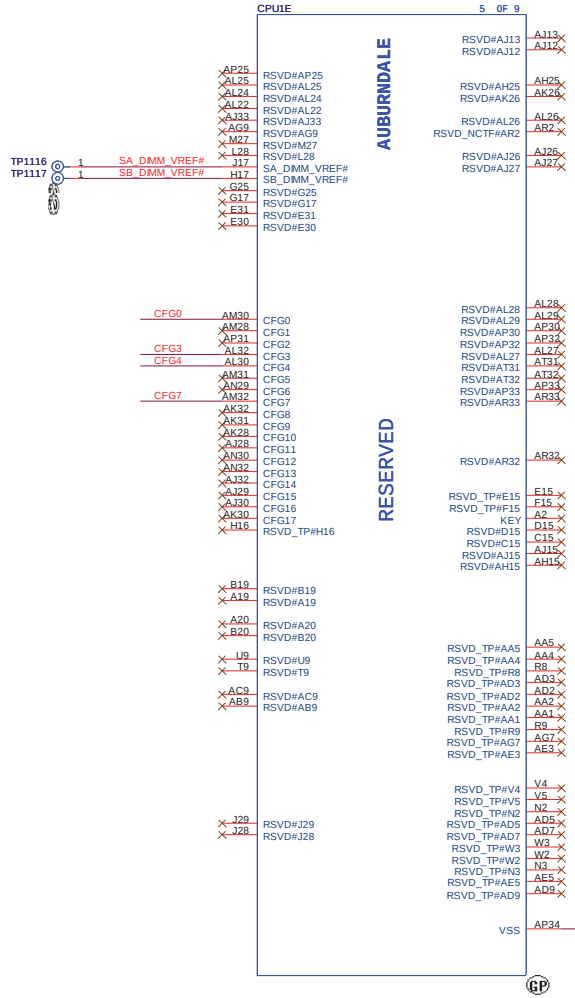
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU (RESERVED)		
Size	Document Number: DJ2 CP UMA	Rev: A00
Date: Tuesday, May 18, 2010	Sheet 11 of 95	

SSID = CPU

PROCESSOR CORE POWER

48A

+VCC_CORE

CPU1F

6 OF 9

AUBURNDALE

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

+1.05V_VTT

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V

for 65 BOM

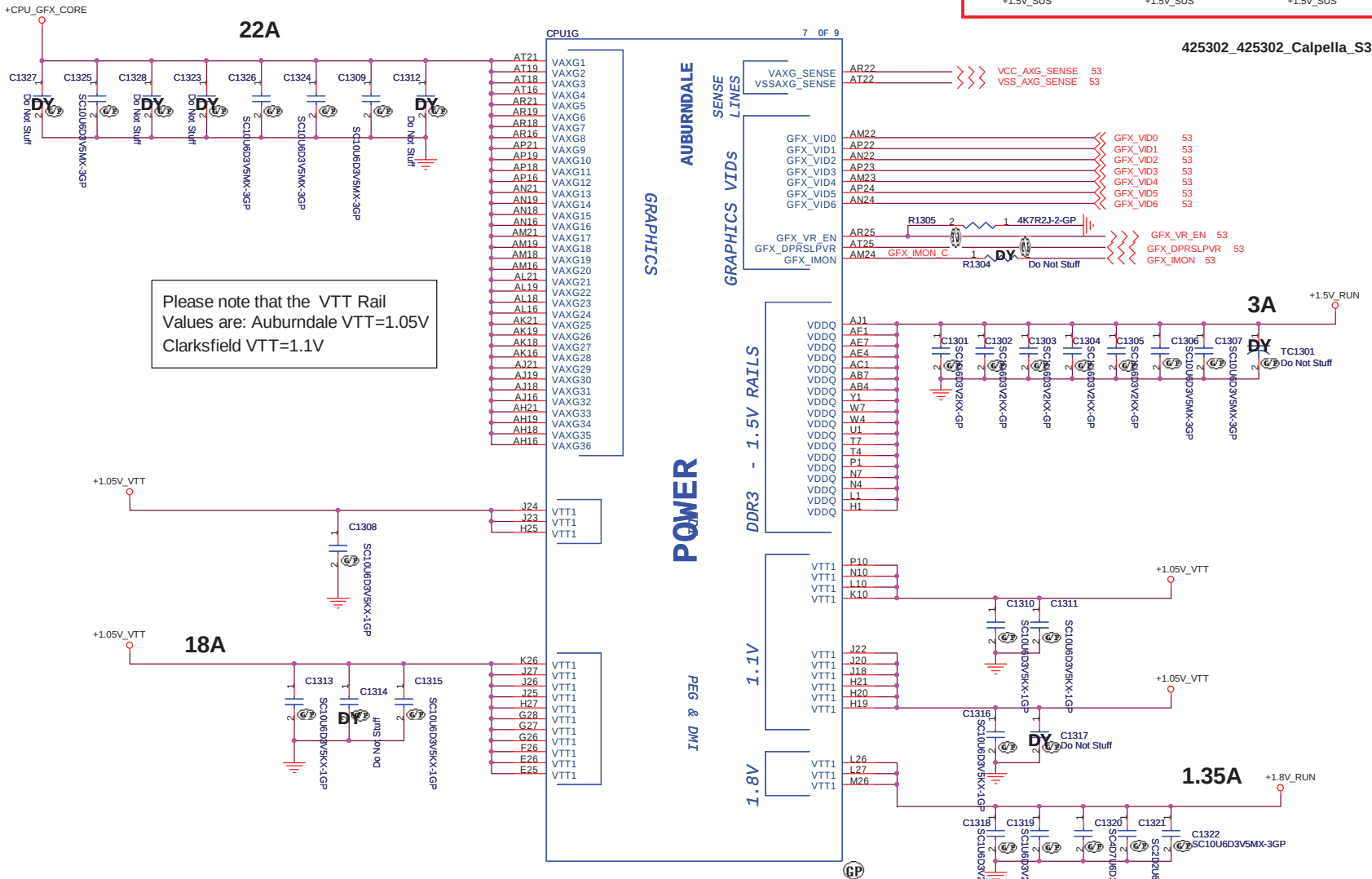
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

Size | Document Number: DJ2 CP UMA | Rev: A00

Date: Tuesday, May 18, 2010 | Sheet 12 of 95

SSID = CPU



425302_425302_Calpella_S3PowerReduction_WhitePape

Revision 0.7

for 65 BOM

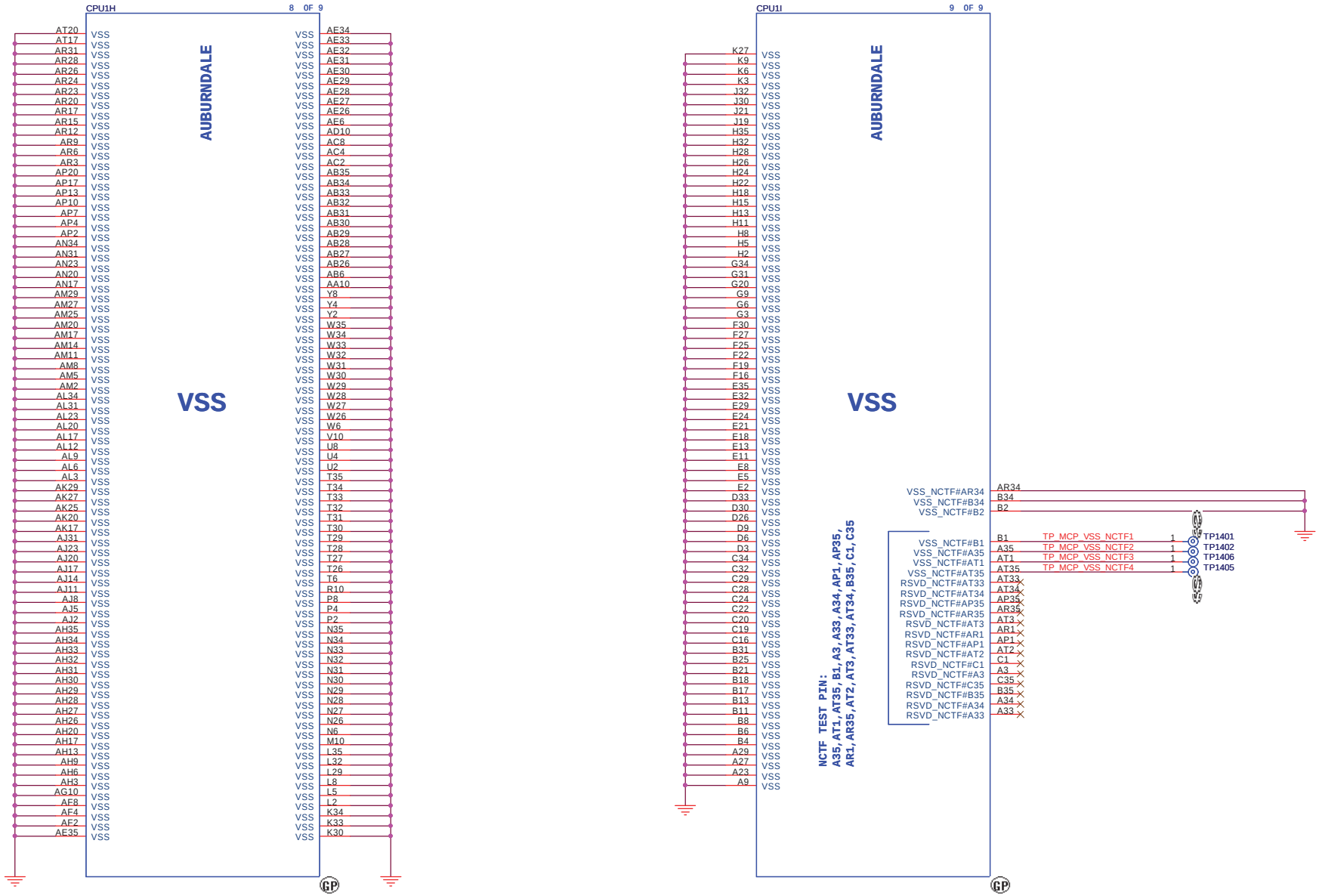
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_GFXCORE)

Size | Document Number: DJ2 CP UMA | Rev: A00

Date: Tuesday, May 18, 2010 | Sheet 13 of 95

SSID = CPU



for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)		
Size	Document Number: DJ2 CP UMA	Rev: A00
Date: Tuesday, May 18, 2010	Sheet 14 of 95	

(Blanking)

for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ2 CP UMA*	*A00*

Date: Tuesday, May 18, 2010 Sheet 15 of 95

(Blanking)

for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ2 CP UMA*	*A00*

Date: Tuesday, May 18, 2010 Sheet 16 of 95

(Blanking)

for 65 BOM

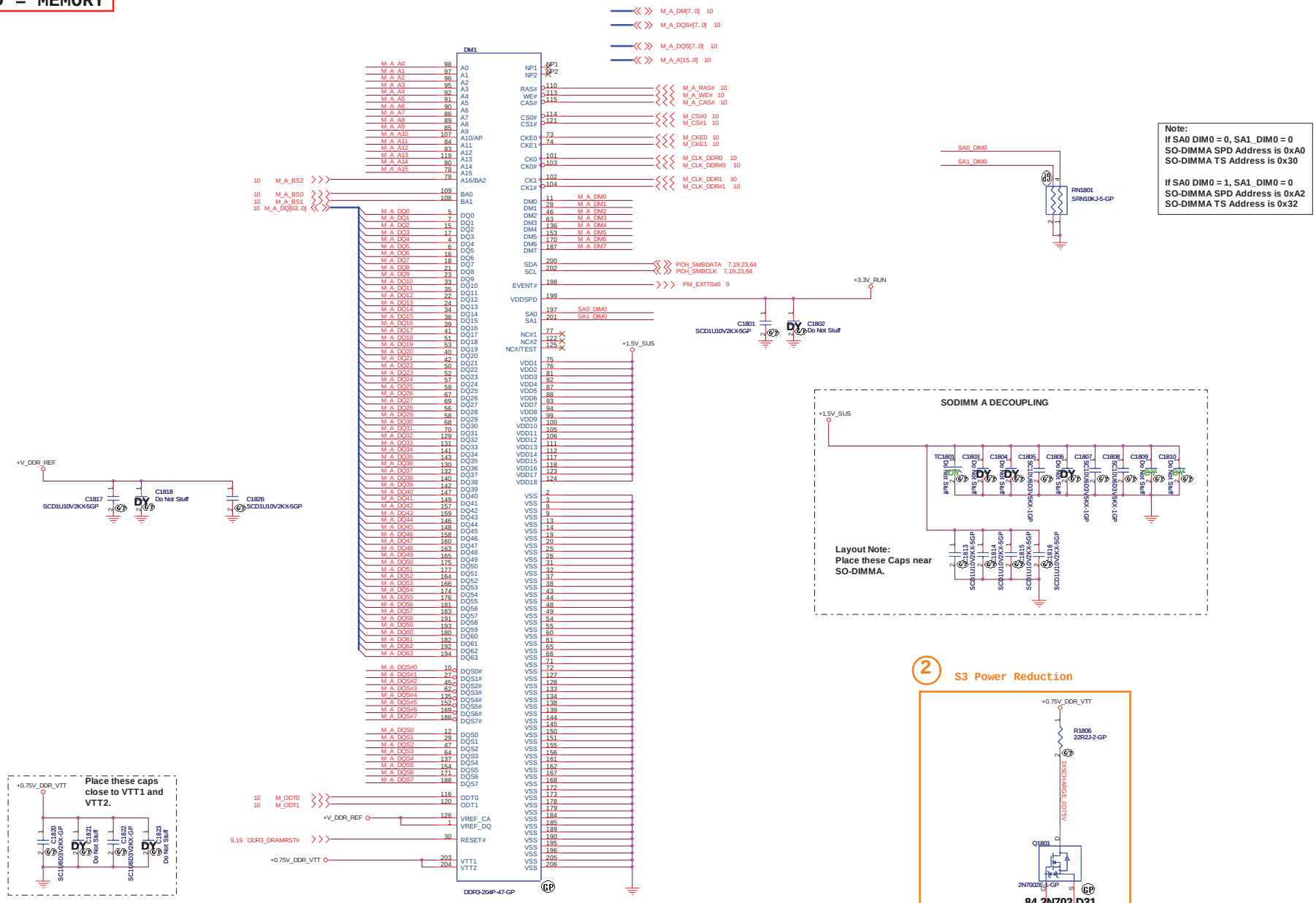
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: DJ2 CP UMA | Rev: A00

Date: Tuesday, May 18, 2010 | Sheet 17 of 95

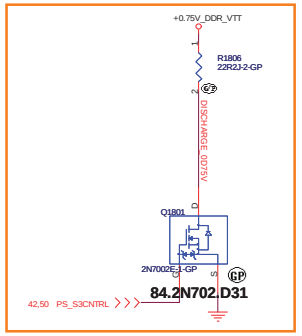
SSID = MEMORY



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

2 **S3 Power Reduction**



for 65 BOM

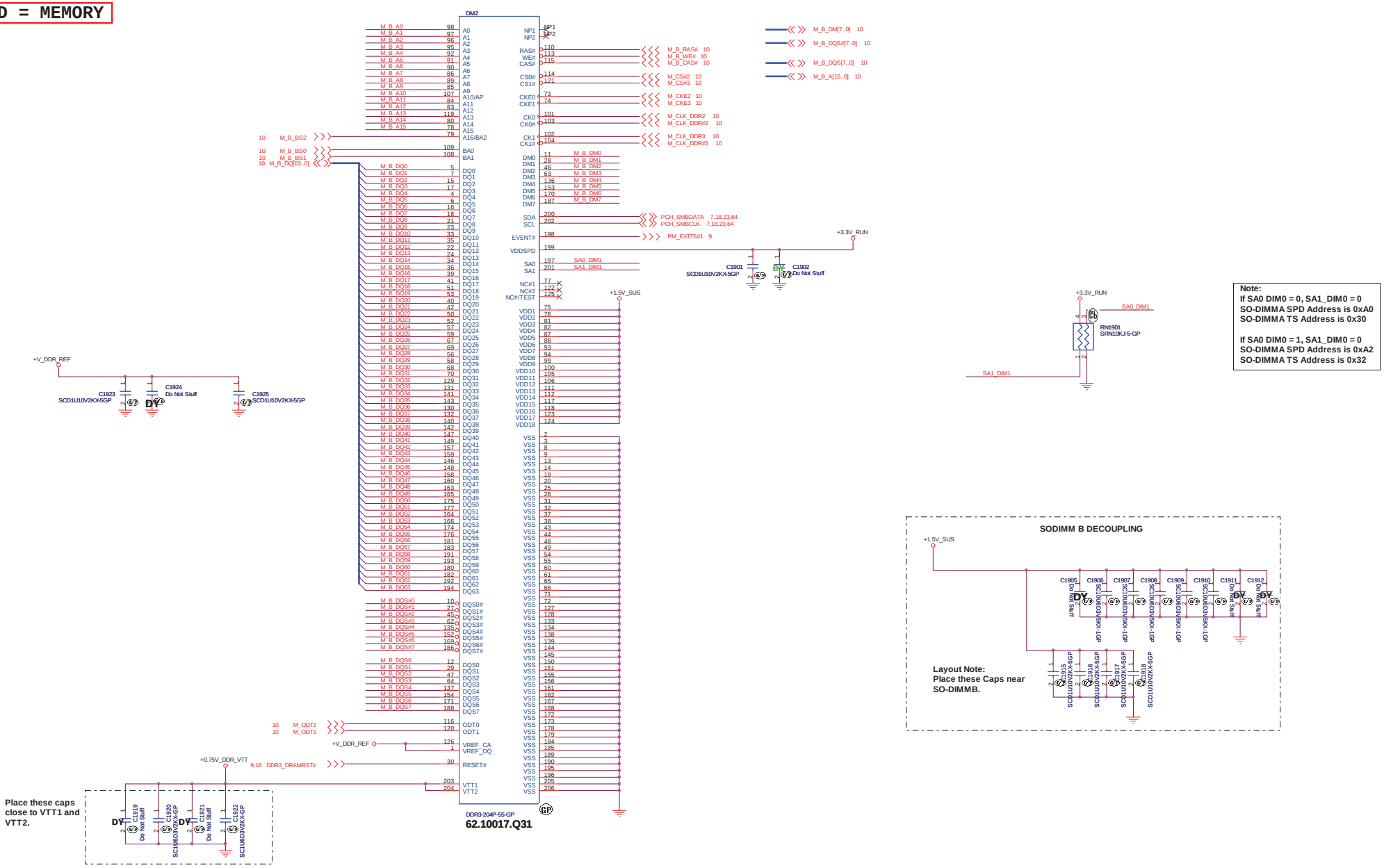
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size	Document Number	Rev
	DJ2 CP UMA	A00

Date: Tuesday, May 18, 2010 Sheet 18 of 95

SSID = MEMORY



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

for 65 BOM

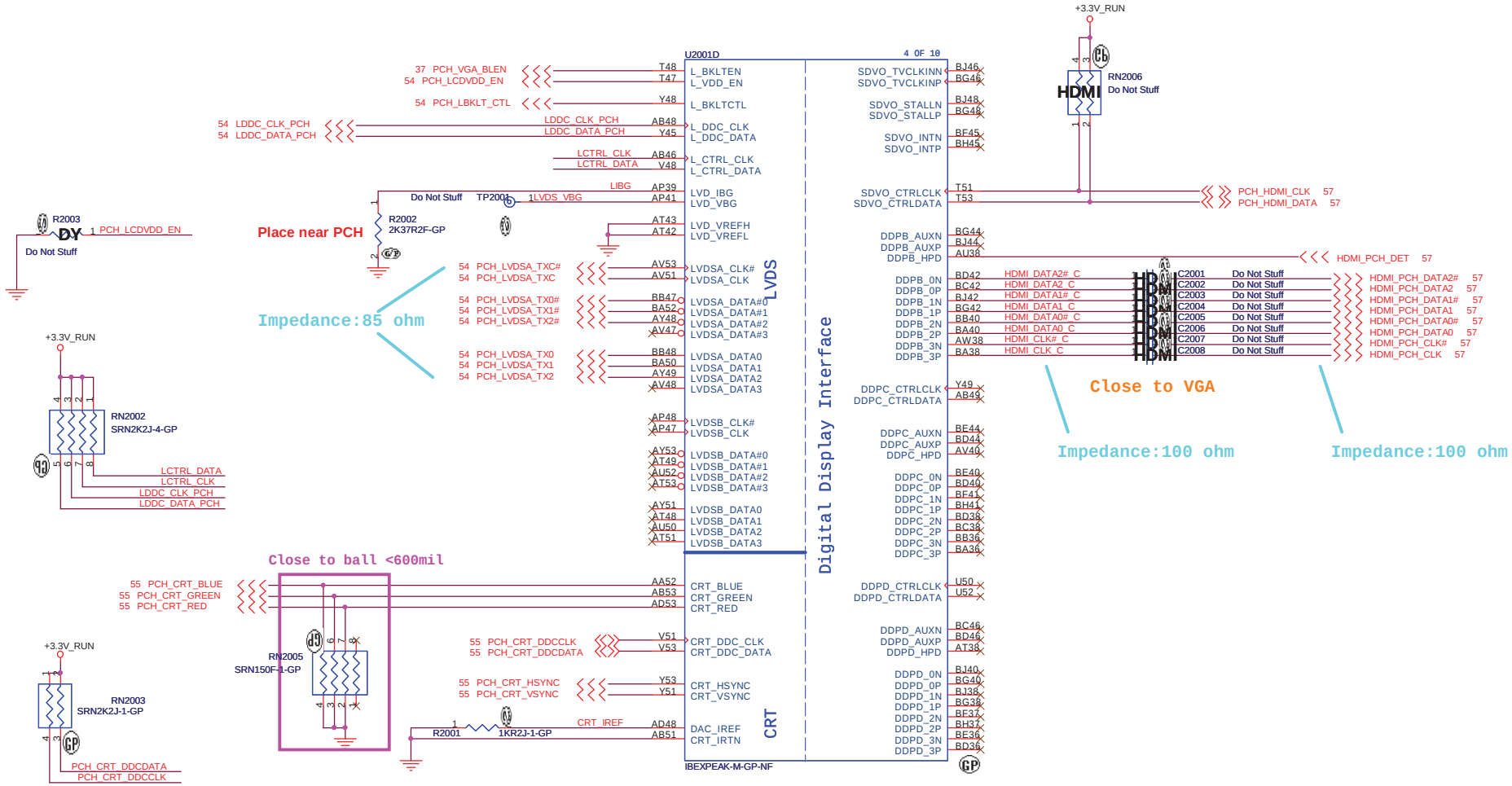
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
	DJ2 CP UMA	A00

Date: Tuesday, May 18, 2010 Sheet 19 of 95

SSID = PCH



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for 65 BOM

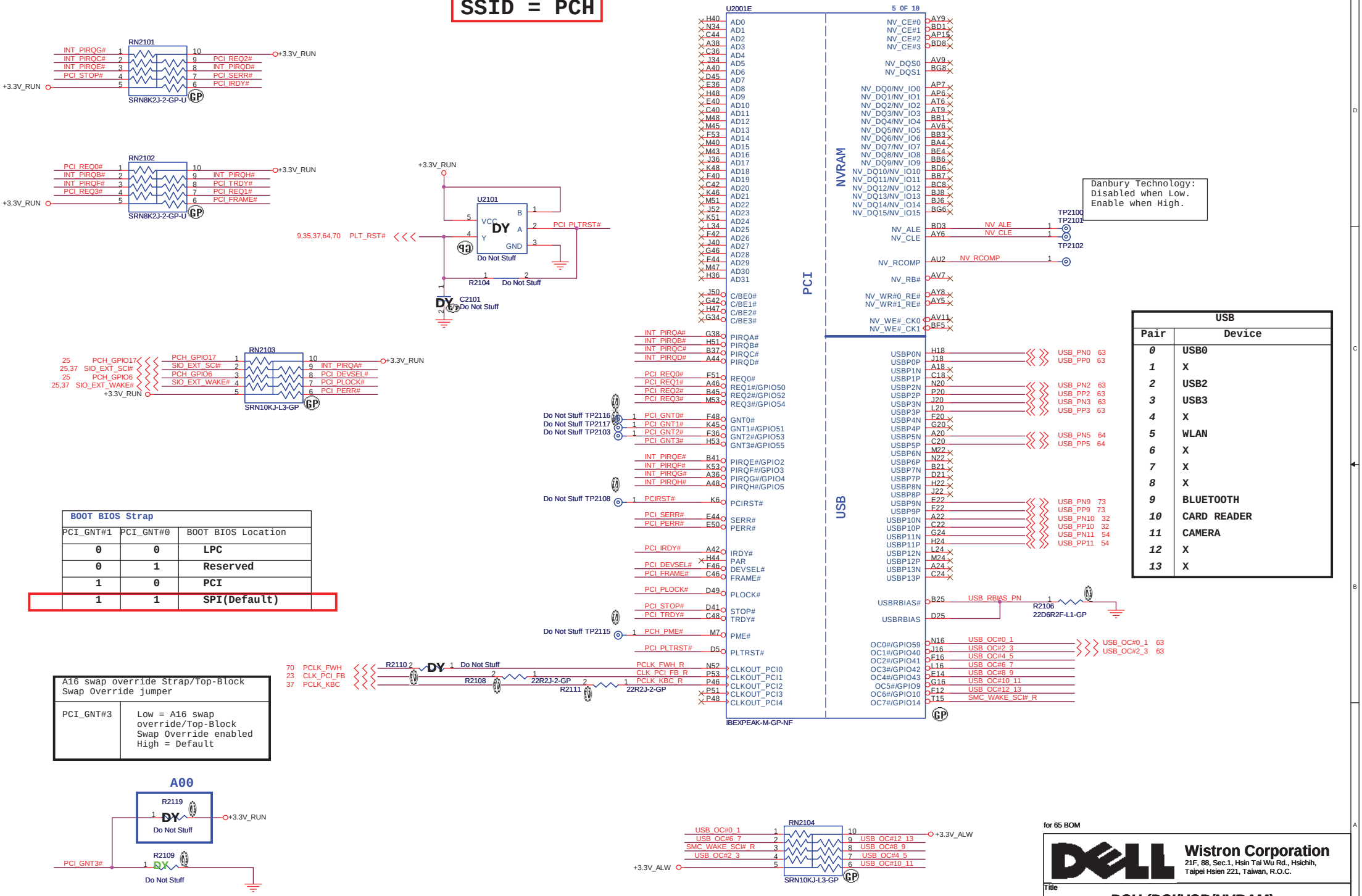
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size | Document Number: DJ2 CP UMA | Rev: A00

Date: Tuesday, May 18, 2010 | Sheet 20 of 95

SSID = PCH



USB	
Pair	Device
0	USB0
1	X
2	USB2
3	USB3
4	X
5	WLAN
6	X
7	X
8	X
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X

BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

for 65 BOM

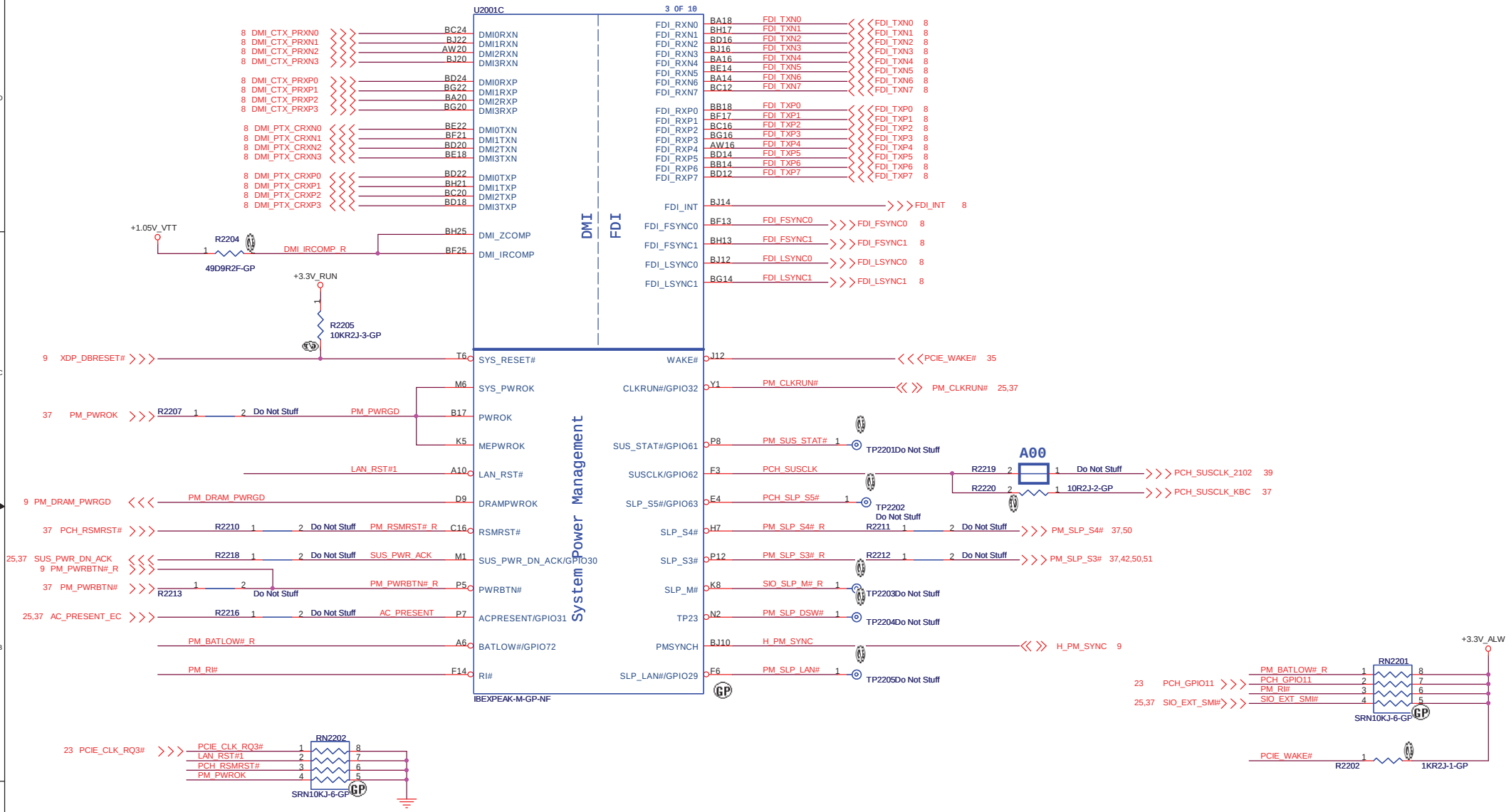
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)

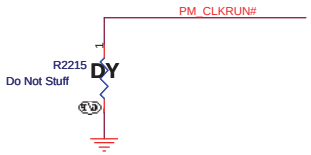
Size | Document Number: DJ2 CP UMA | Rev: A00

Date: Tuesday, May 18, 2010 | Sheet 21 of 95

SSID = PCH



Option to " Disable " clkrun.
Pulling it down will keep the clks running.



for 65 BOM

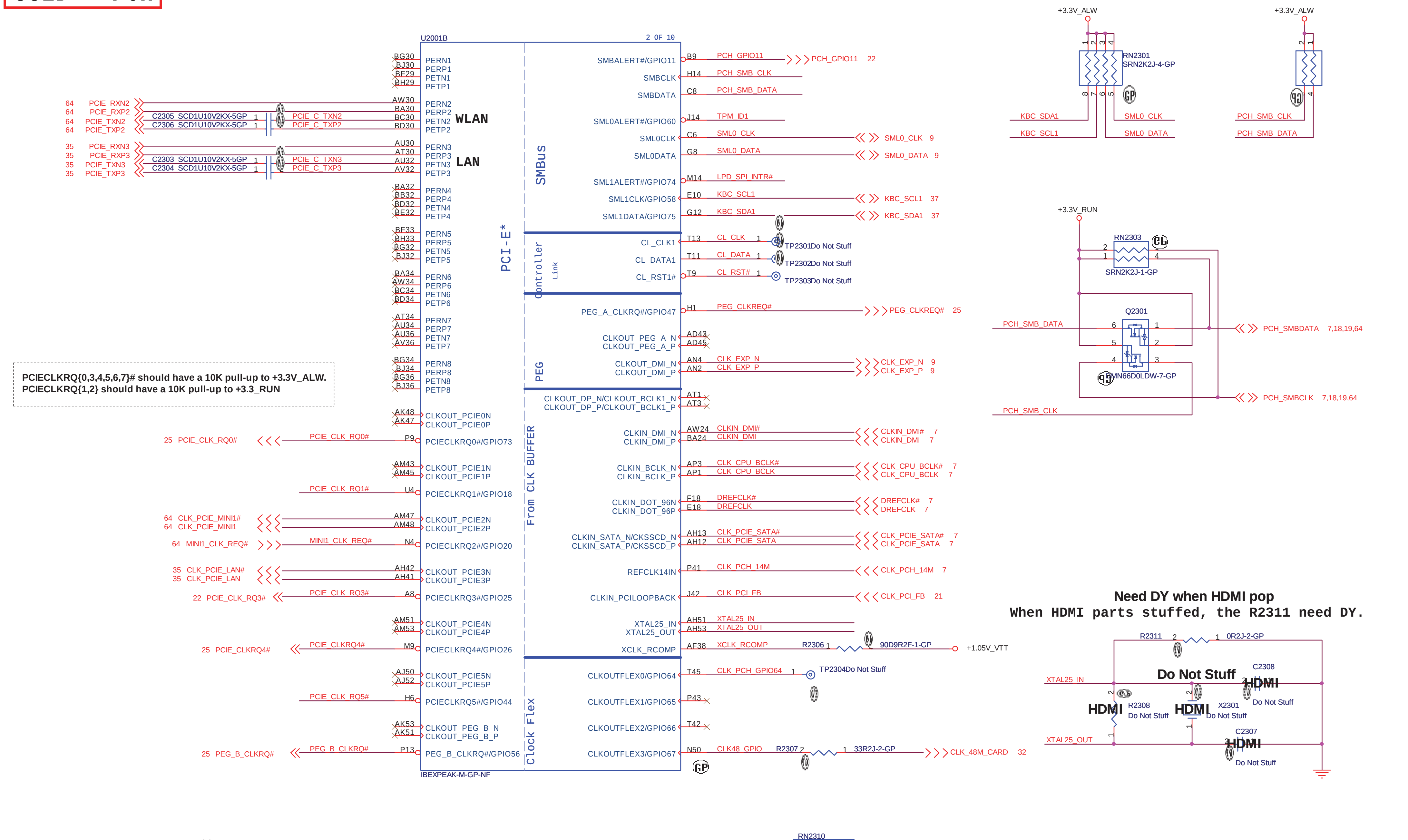
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)

Size	Document Number	Rev
	DJ2 CP UMA	A00

Date: Tuesday, May 18, 2010 Sheet 22 of 95

SSID = PCH



PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN

Need DY when HDMI pop

When HDMI parts stuffed, the R2311 need DY.

for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (PCI-E/SMBUS/CLOCK/CL)**

Size	Document Number	Rev
	DJ2 CP UMA	A00

Date: Tuesday, May 18, 2010 Sheet 23 of 95

SSID = PCH

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

+RTC_CELL
RN2402 SRN20KJ-GP-U
SRTCRST#
PCH_RTCRST#
C2401 SC1U10V3KX-3GP
R2401 10MR2J-L-GP
PCH_RTCX1
PCH_RTCX2
X2401 X-32D768KHZ-40GPU
C2402 SC18P50V2JN-1-GP
C2403 SC18P50V2JN-1-GP
X01
X01
82.30001.841
C2404 SC1U10V3KX-3GP
G2401 Do Not Stuff
R2406 1MR2J-1-GP
R2404 330KR2F-L-GP
SM_INTRUDER#
PCH_INTVRMEN

RN2401 SRN33J-7-GP
30 PCH_AZ_CODEC_RST#
30 PCH_AZ_CODEC_BITCLK
30 PCH_AZ_CODEC_SYNC
30 PCH_SDOUT_CODEC
ACZ_RST#_R
ACZ_BIT_CLK
ACZ_SYNC_R
ACZ_SDATAOUT_R

NO REBOOT STRAP
+3.3V_RUN
R2410 0Y Do Not Stuff
ACZ_SPKR

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

R2411 10KR2J-3-GP
CLK_SATA_OE#
CLK_SATA_OE# 25

U2001A 1 OF 10

RTC: RTCX1 B13, RTCX2 D13, RTCRST# C14, SRTCRST# D17, INTRUDER# A16, INTVRMEN A14
IHDA: HDA_BCLK A30, HDA_SYNC D29, HDA_SPKR P1, HDA_RST# C30, HDA_SDIN0 G30, HDA_SDIN1 F30, HDA_SDIN2 E32, HDA_SDIN3 F32, HDA_SDO B29, HDA_DOCK_EN#/GPIO33 H32, HDA_DOCK_RST#/GPIO13 J30
JTAG: JTAG_TCK M3, JTAG_TMS K3, JTAG_TDI K1, JTAG_TDO J2, TRST# J4
SPI: SPI_CLK BA2, SPI_CS0# AV3, SPI_CS1# AY3, SPI_MOSI AY1, SPI_MISO AV1
LPC: FWH0/LAD0 D33, FWH1/LAD1 B33, FWH2/LAD2 C32, FWH3/LAD3 A32, FWH4/LFRAME# C34, LDRQ0# A34, LDRQ1#/GPIO23 F34, SERIRQ AB9
SATA: SATA0RXN AK7, SATA0RXP AK6, SATA0TXN AK11, SATA0TXP AK9, SATA1RXN AH6, SATA1RXP AH5, SATA1TXN AH9, SATA1TXP AH8, SATA2RXN AF11, SATA2RXP AF9, SATA2TXN AF7, SATA2TXP AF6, SATA3RXN AH3, SATA3RXP AH1, SATA3TXN AF3, SATA3TXP AF1, SATA4RXN AD9, SATA4RXP AD8, SATA4TXN AD6, SATA4TXP AD5, SATA5RXN AD3, SATA5RXP AD1, SATA5TXN AB3, SATA5TXP AB1, SATAICOMPO AF16, SATAICOMPI AF15, SATALED# T3, SATA0GP/GPIO21 Y9, SATA1GP/GPIO19 V1

IBEXPEAK-M-GP-NF

LPC_LAD[0..3] 37,70
LPC_LFRAME# 37,70
INT_SERIRQ 25,37

HDD: SATA_TXN0_C C2405, SATA_TXP0_C C2406, SCD01U16V2KX-3GP; SATA_RXN0_C 59, SATA_RXP0_C 59, SATA_TXN0 59, SATA_TXP0 59
ODD: SATA_TXN1_C C2407, SATA_TXP1_C C2408, SCD01U16V2KX-3GP; SATA_RXN1_C 59, SATA_RXP1_C 59, SATA_TXN1 59, SATA_TXP1 59

SATAICOMP R2412 37D4R2F-GP +1.05V_VTT
SATA_LED# 66
SATA_DET#0_R 25
SATA_DET#1_R 25

30 ACZ_SPKR
30 PCH_SDIN_CODEC
37 ME_UNLOCK#

Do Not Stuff TP2404 PCH_JTAG_TCK
Do Not Stuff TP2405 PCH_JTAG_TMS
Do Not Stuff TP2406 PCH_JTAG_TDI
Do Not Stuff TP2407 PCH_JTAG_TDO
Do Not Stuff TP2408 PCH_JTAG_RST#

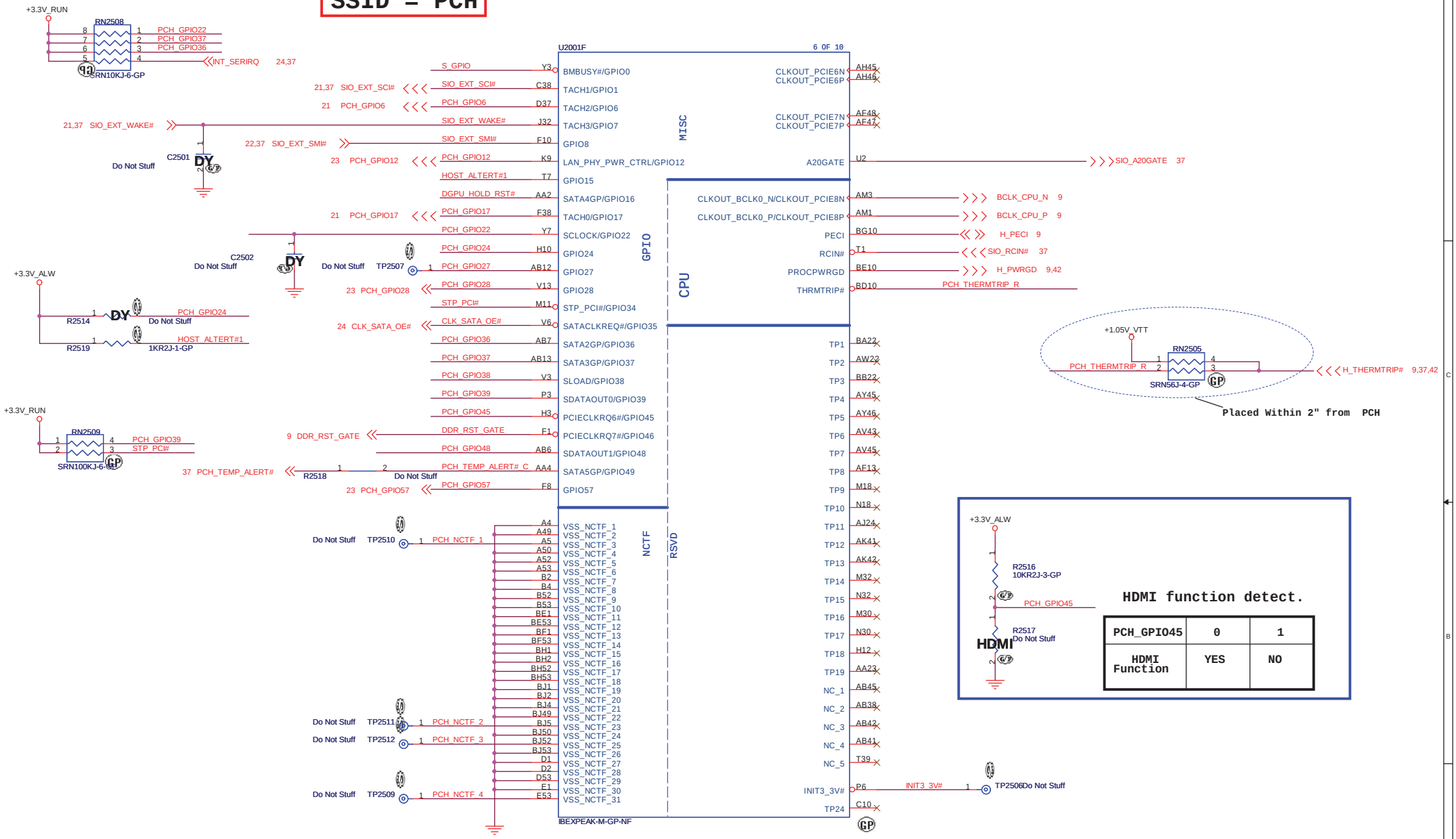
62 PCH_SPI_CLK R2413 15R2J-GP SPI_CLK_R
62 PCH_SPI_CS0# R2414 15R2J-GP SPI_CS#0_R
62 PCH_SPI_DO R2415 15R2J-GP SPI_MOSI_R
62 PCH_SPI_DI

for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size: Document Number: DJ2 CP UMA Rev: A00
Date: Tuesday, May 18, 2010 Sheet 24 of 95

SSID = PCH



HDMI function detect.

PCH_GPIO45	0	1
HDMI Function	YES	NO

for 65 BOM

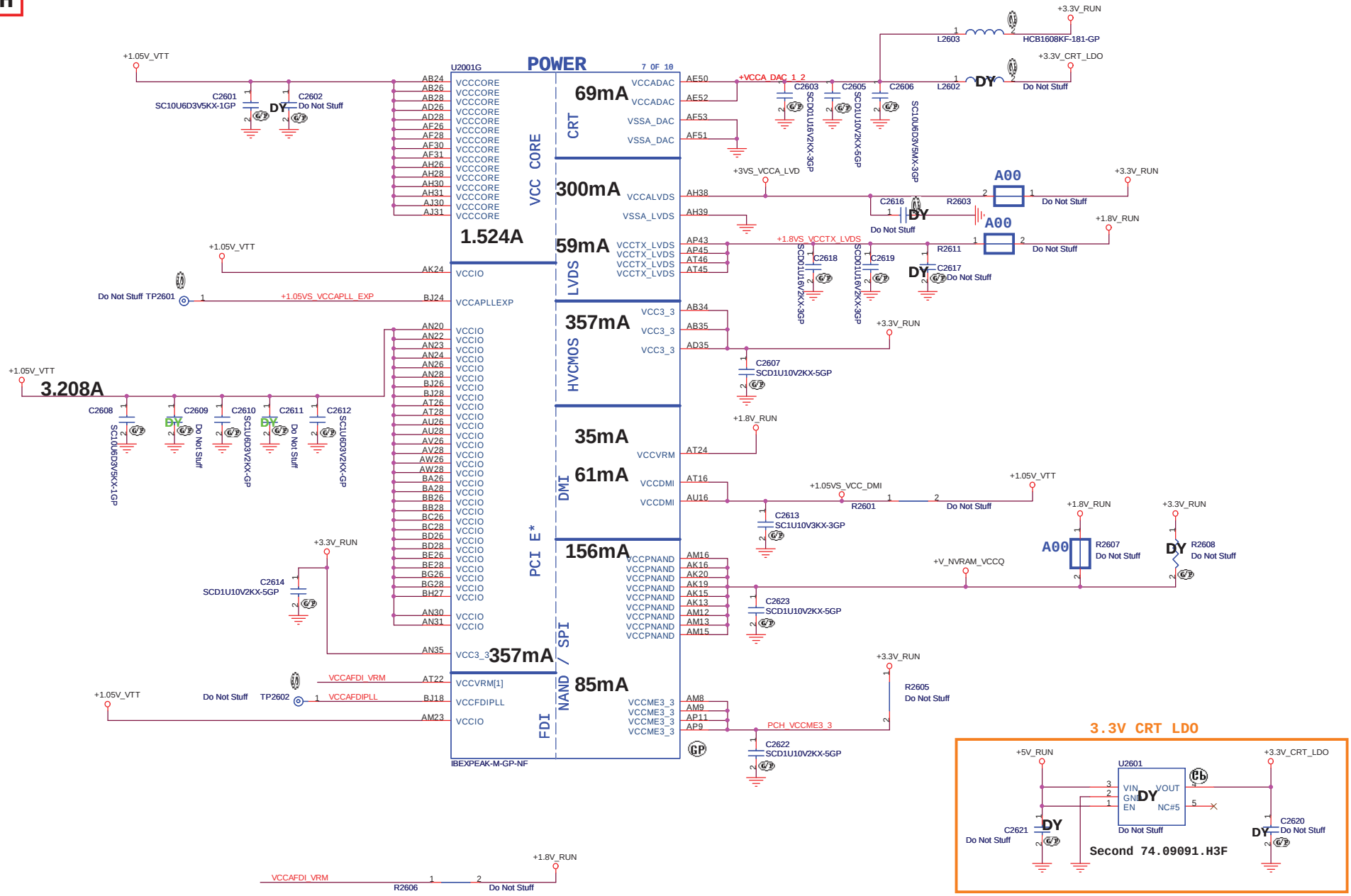
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (GPIO/CPU)**

Size	Document Number	Rev
	DJ2 CP UMA	A00

Date: Tuesday, May 18, 2010 Sheet 25 of 95

SSID = PCH



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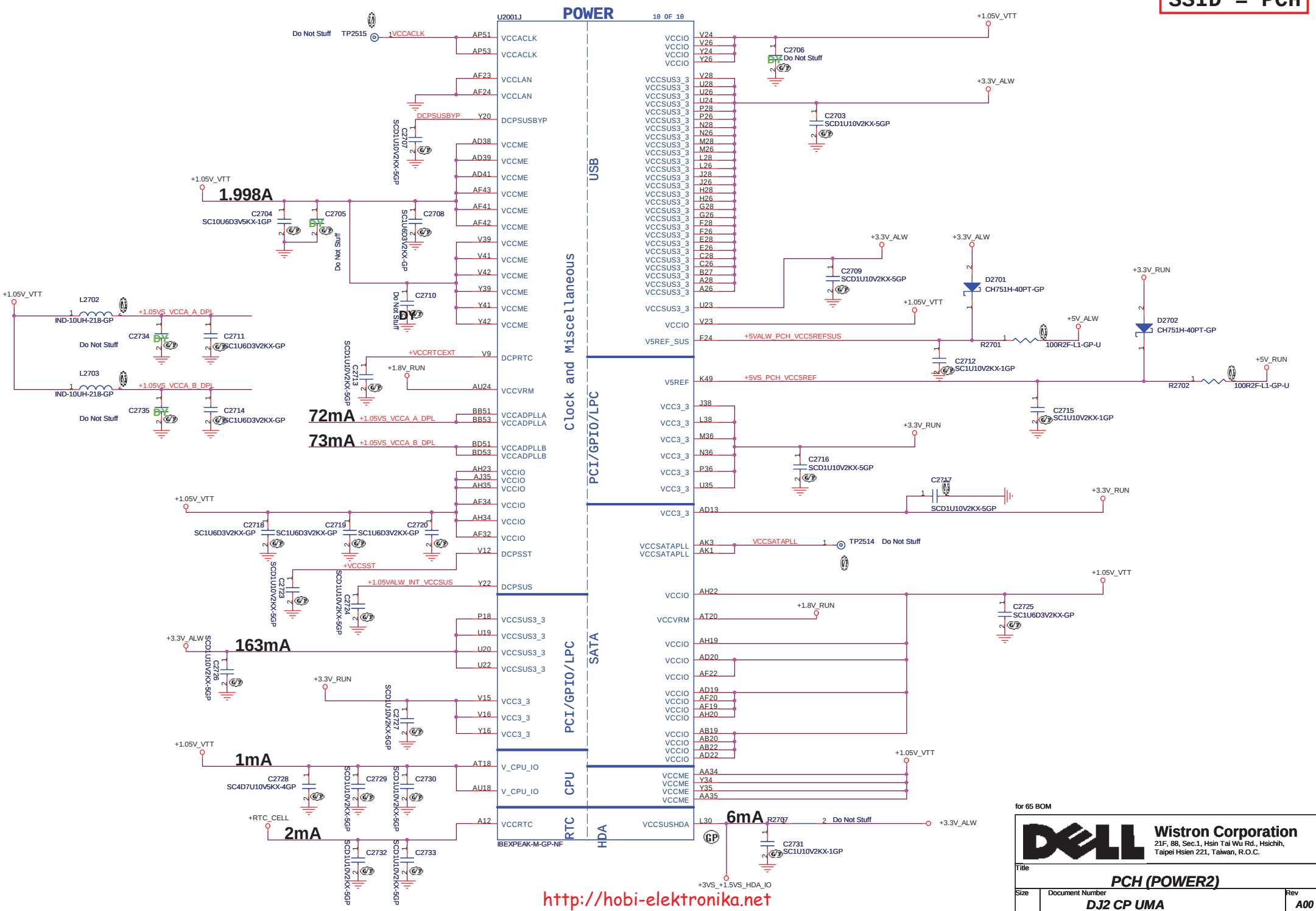
for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
PCH (POWER1)		
Size	Document Number	Rev
	DJ2 CP UMA	A00
Date: Tuesday, May 18, 2010	Sheet 26 of 95	

SSID = PCH



for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (POWER2)	
Size	Document Number: DJ2 CP UMA	Rev: A00
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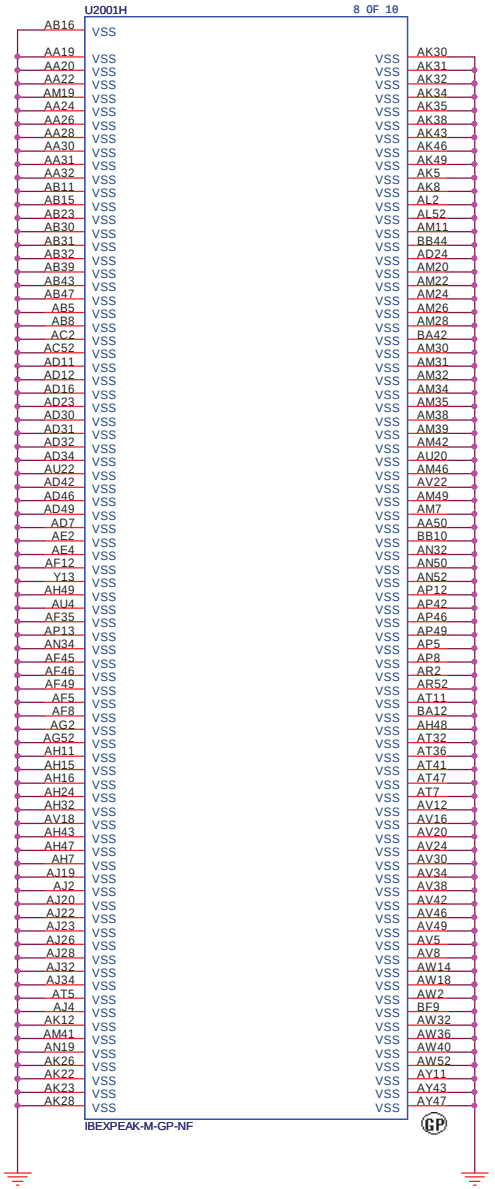
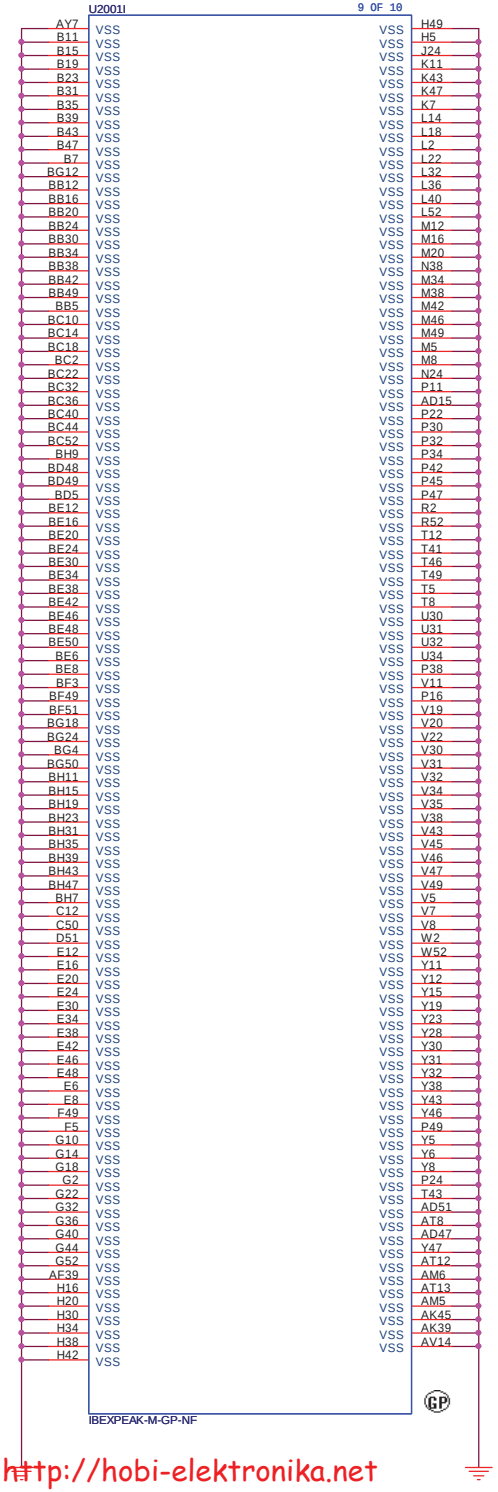
SSID = PCH





for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (VSS)

Size | Document Number: DJ2 CP UMA | Rev: A00

Date: Tuesday, May 18, 2010 | Sheet 28 of 95

(Blanking)

for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: DJ2 CP UMA | Rev: A00

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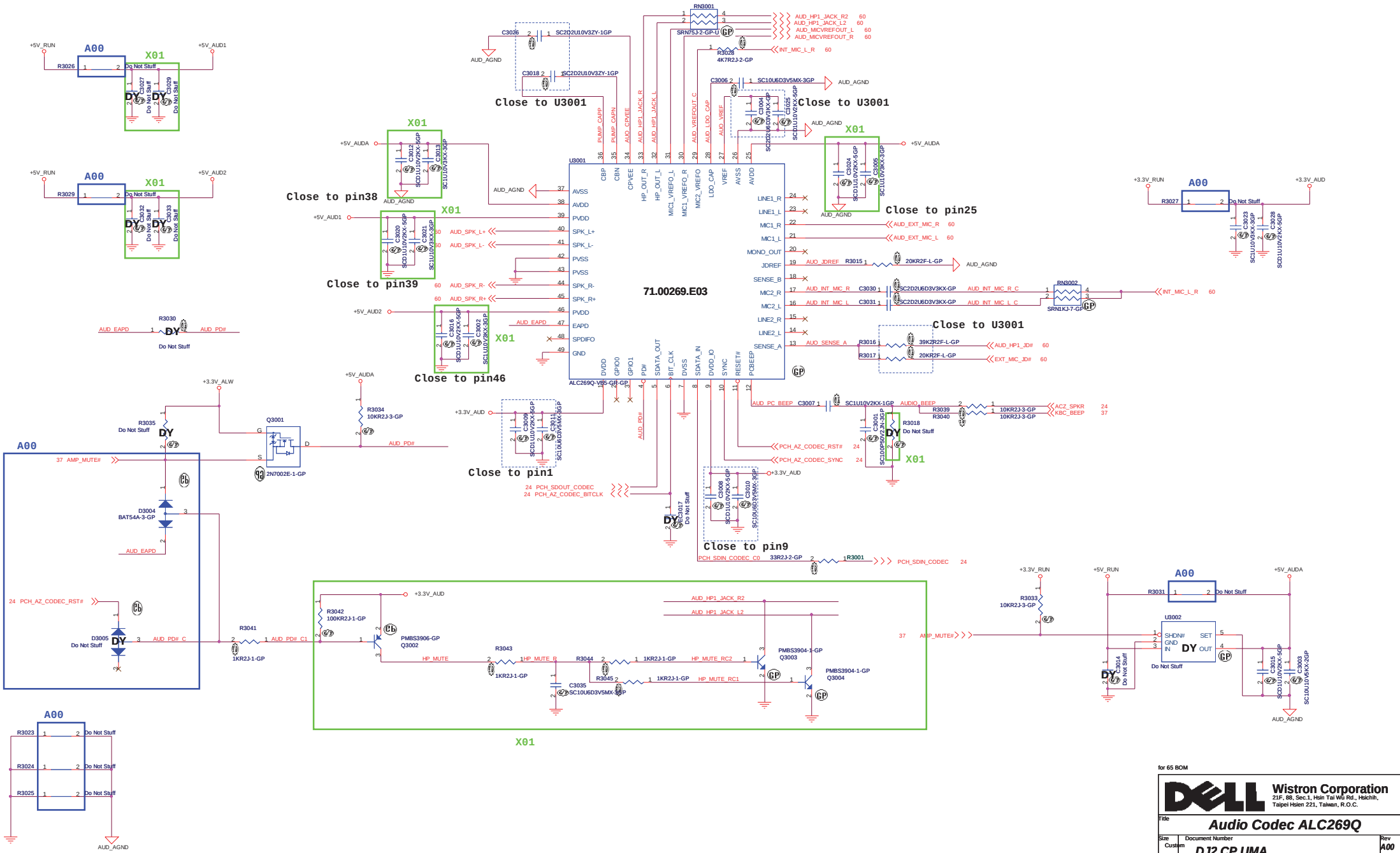
SSID = AUDIO



(Blanking)

for 65 BOM

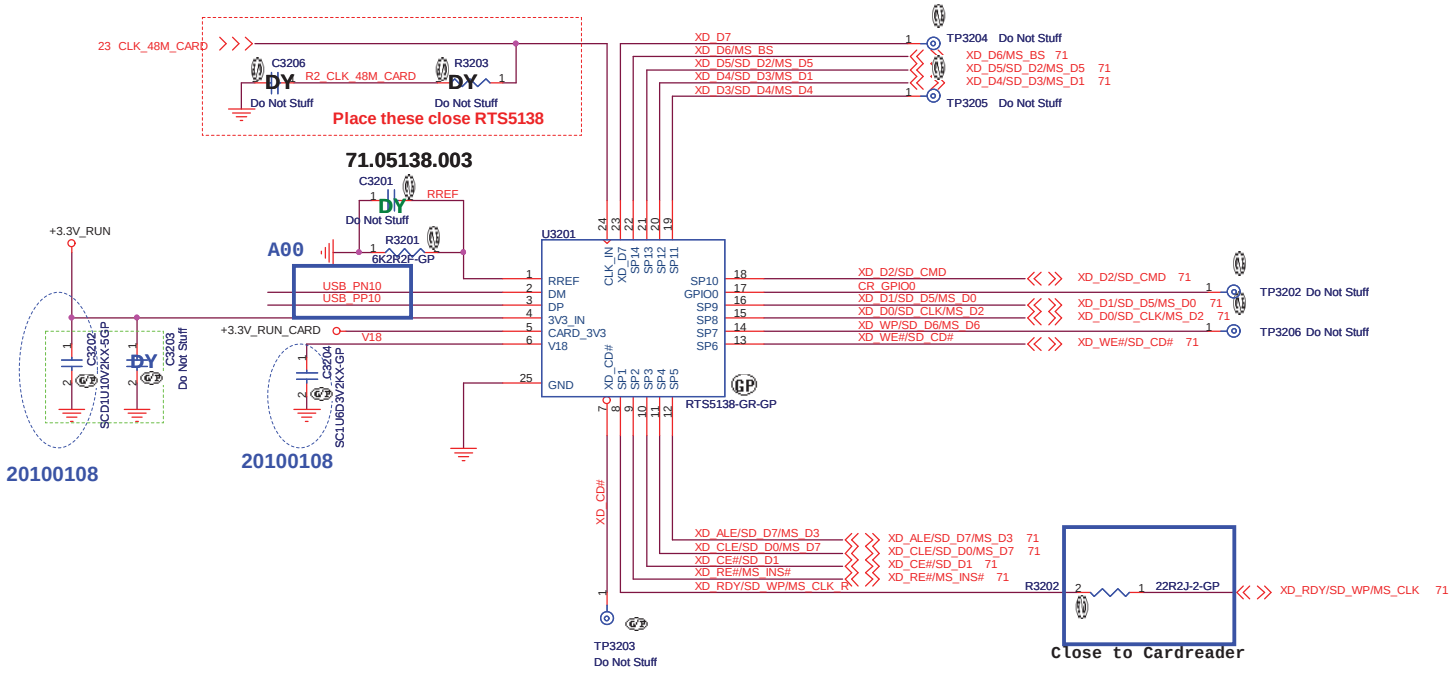
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

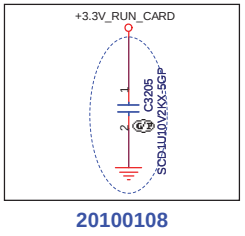
Title: Reserved

Size: A3 | Document Number: DJ2 CP UMA | Rev: A00

Date: Tuesday, May 18, 2010 | Sheet 31 of 95

SSID = SDIO





for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5138

Size	Document Number	Rev
Custom	DJ2 CP UMA	A00

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for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
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Date: Tuesday, May 18, 2010 Sheet 33 of 95

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for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: DJ2 CP UMA | Rev: A00

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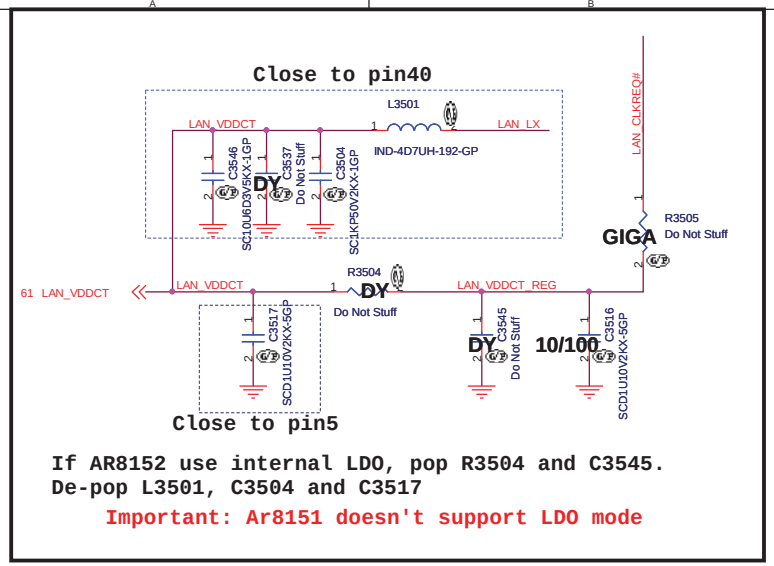
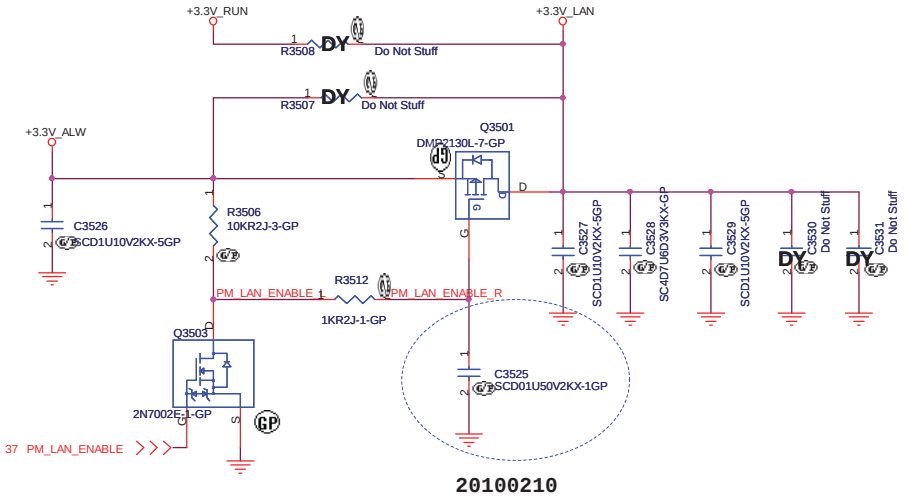
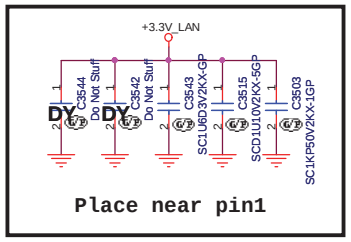
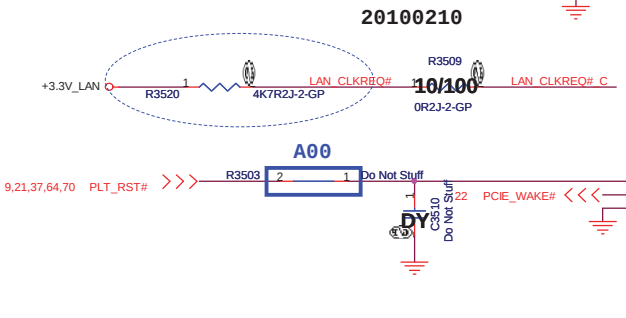
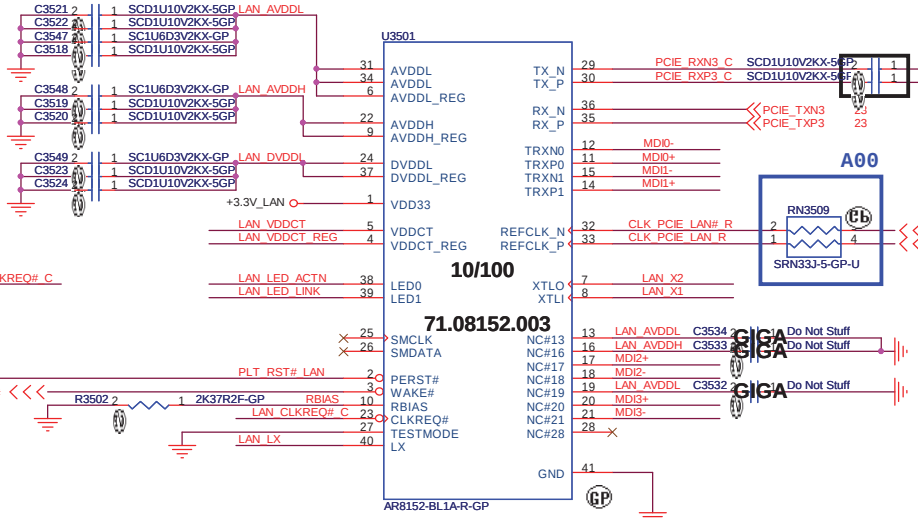


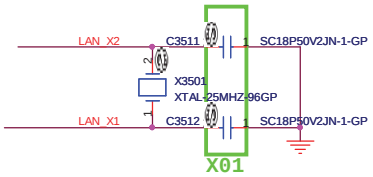


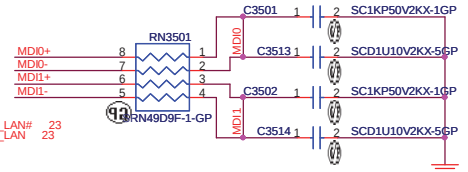
Pin6 is the AVDDL LDO output, 1uF+0.1uF(C3547 and C3518) close to Pin6;
C3522, C3521 close to Pin31, Pin34 respectively.
Pin9 is the AVDDH LDO output, 1uF+0.1uF(C3548 and C3519) close to Pin9;
C3520 close to Pin22.
Pin37 is the DVDDL LDO output, 1uF+0.1uF(C3549 and C3523) close to Pin37;
C3524 close to Pin24.

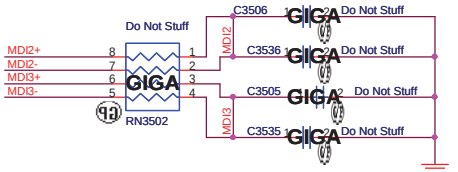




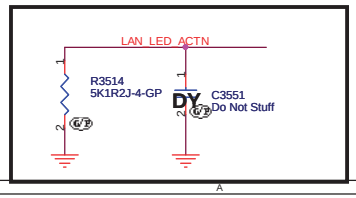




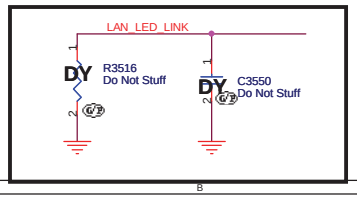




If overclocking, de-pop R3514



If use LDO mode, pop R3516



Giga LAN use 71.08151.A03

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for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AR8152/AR8151

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for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: DJ2 CP UMA | Rev: A00

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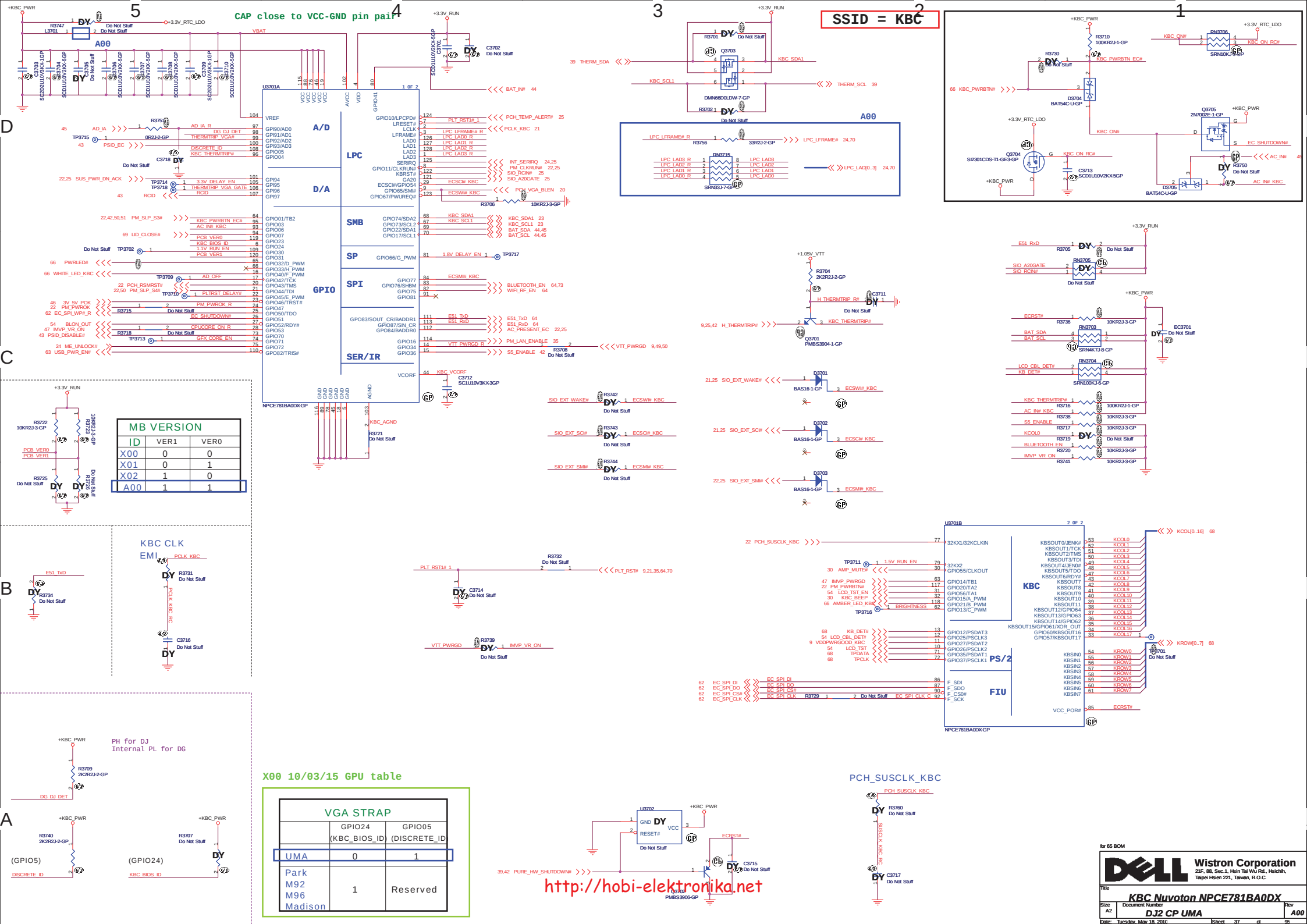
SSID = KBC
CAP close to VCC-GND pin pair
A00
MB VERSION
ID | VER1 | VER0
X00 | 0 | 0
X01 | 0 | 1
X02 | 1 | 0
A00 | 1 | 1
KBC CLK EMI
PH for DJ
Internal PL for DG
X00 10/03/15 GPU table
VGA STRAP
GPIO24 (KBC_BIOS_ID) | GPIO05 (DISCRETE_ID)
UMA | 0 | 1
Park M92 M96 Madison | 1 | Reserved
PCH_SUSCLK_KBC
U3701A
NPCE781BA0DX-GP
U3701B
KBC
PS/2
FIU
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
http://hobi-elektronika.net
Wistron Corporation
KBC Nuvoton NPCE781BA0DX
DJ2 CP UMA
A00

(Blanking)

for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *DJ2 CP UMA* | Rev: *A00*

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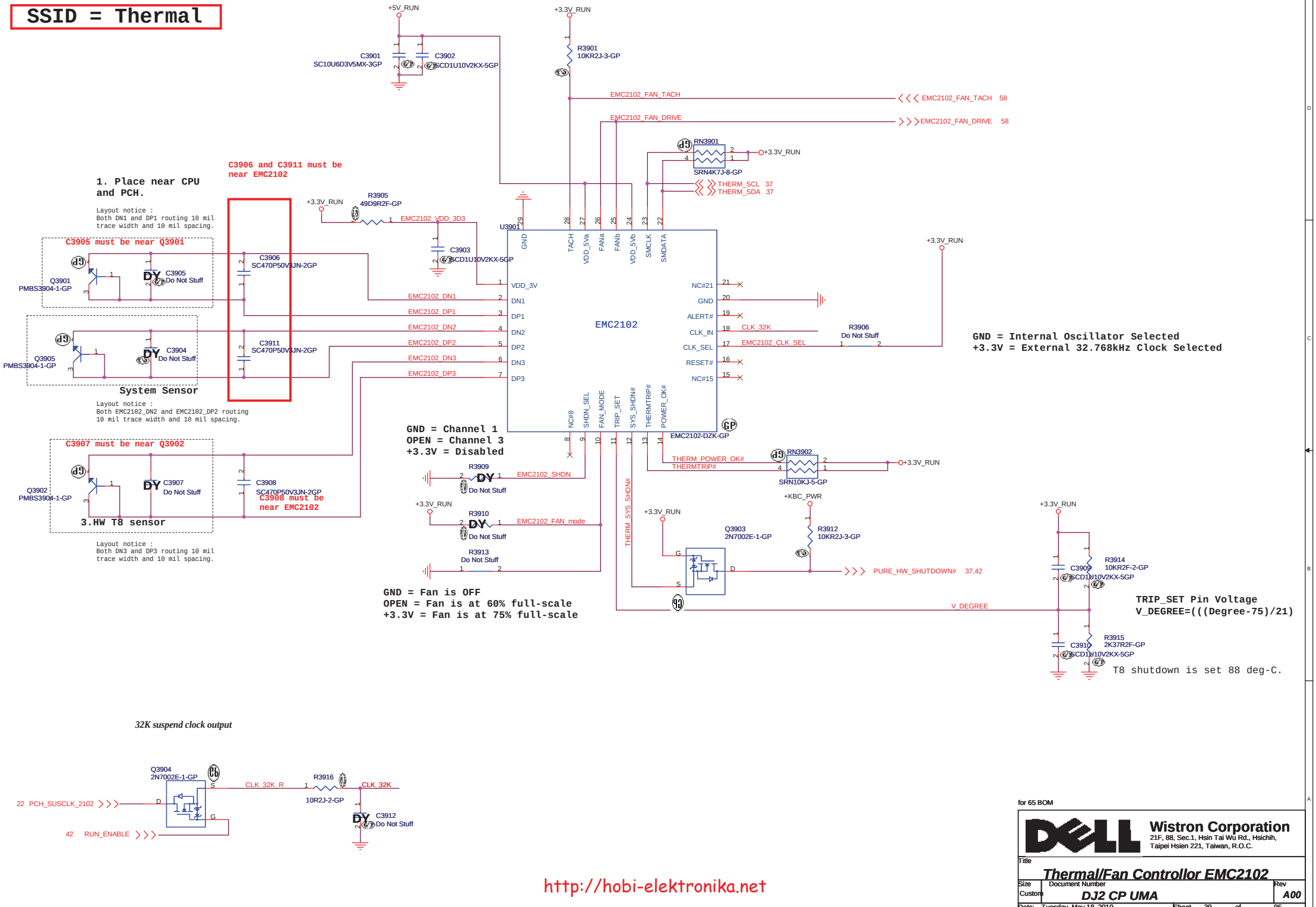
SSID = Thermal



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for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size	Document Number	Rev
Custom	DJ2 CP UMA	A00

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for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
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for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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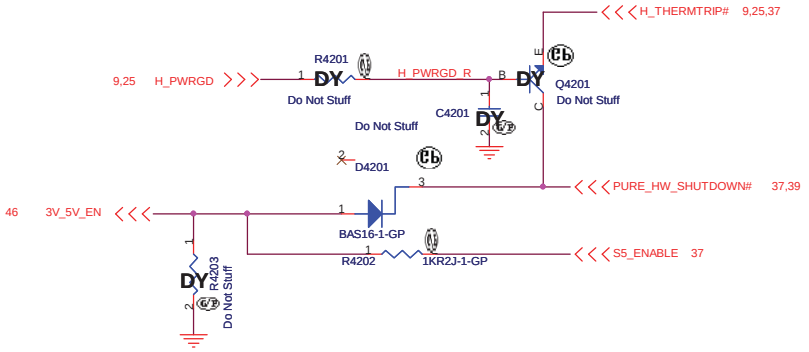
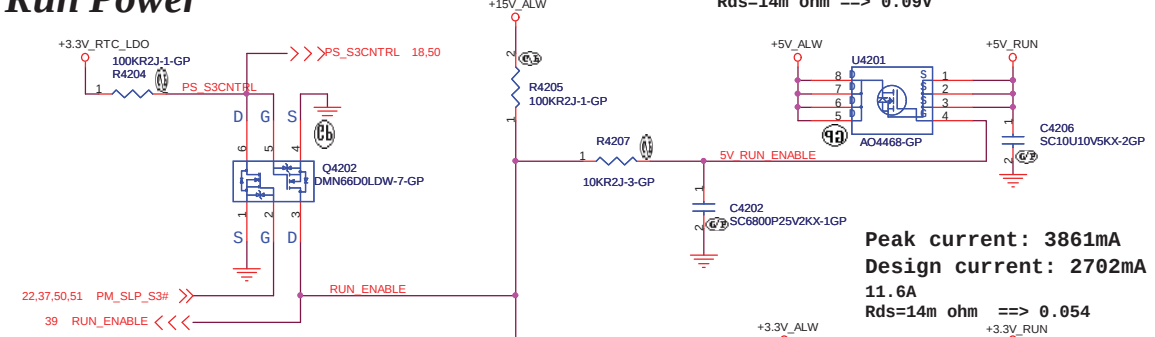
SSID = Reset.Suspend

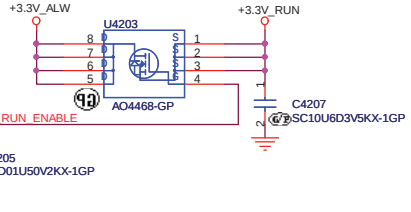


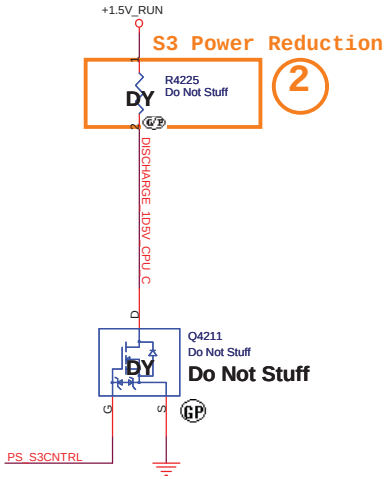
Run Power

Peak current: 6370mA (HD:1100 ODD:2500)
Design current: 4459 mA
11.6A
Rds=14m ohm ==> 0.09V



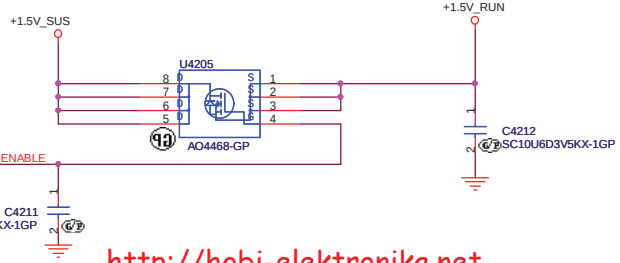
Peak current: 3861mA
Design current: 2702mA
11.6A
Rds=14m ohm ==> 0.054





+1.5V_RUN

MAX Current 3000 mA
Design Current 2100 mA



+1.5V_RUN_CPU Comsumption
Peak current 3A

+1.5V_RUN for Mini-Card Comsumption
Peak current 1A

Total= 4A

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Power Plane Enable*

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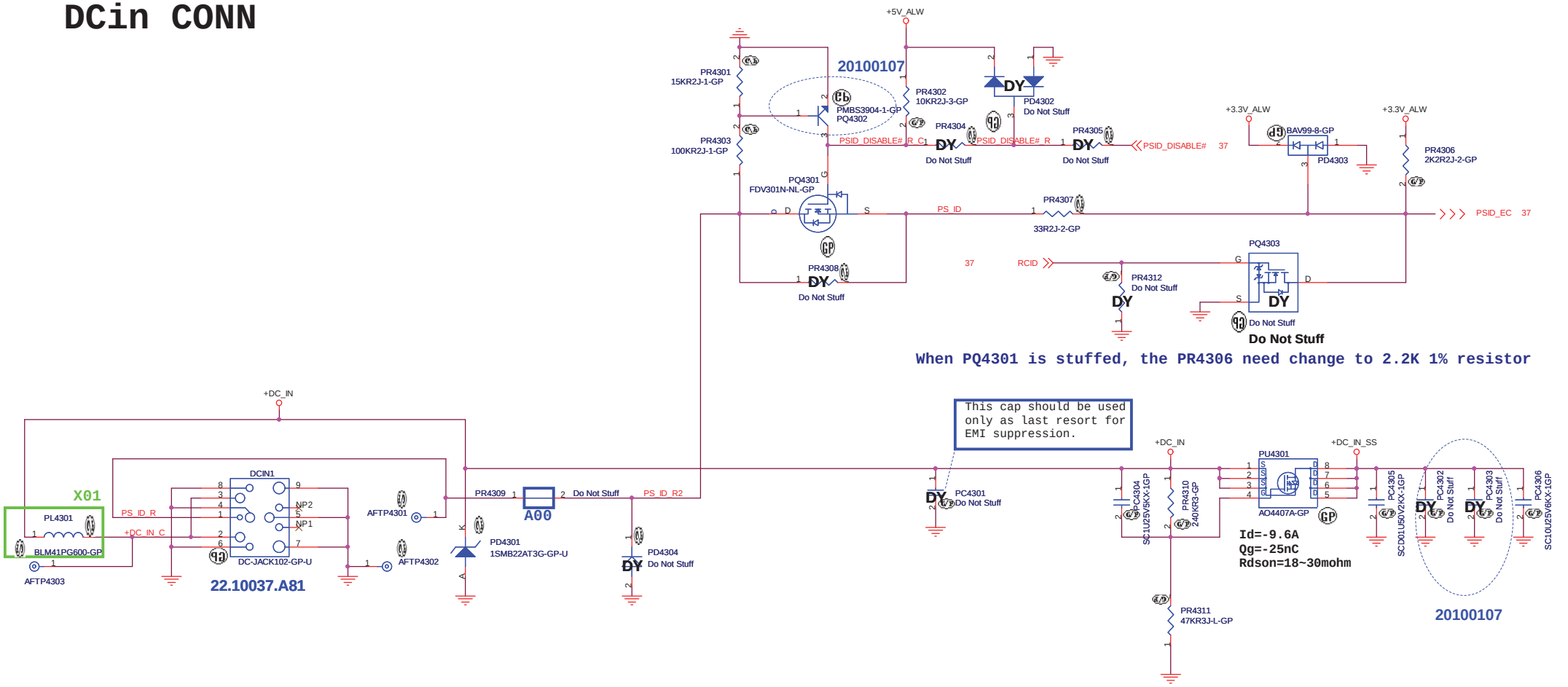
SSID = PWR.Support

DCin CONN



for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN Jack		
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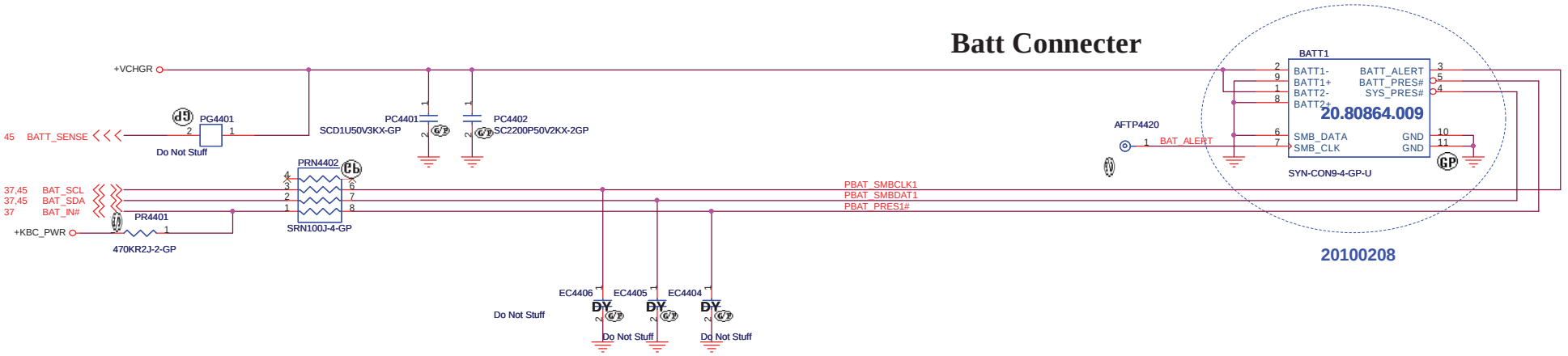
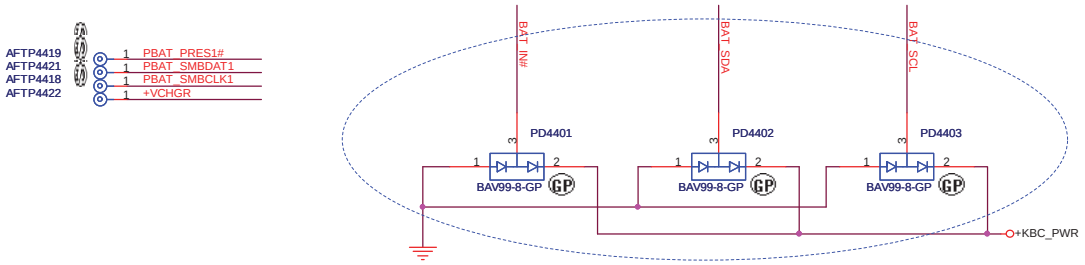
Batt Connecter



20100208

EC404,EC405,EC406 Close BATT1 Connector



20100107

for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT CONN	
Size: A3	Document Number: DJ2 CP UMA	Rev: A00
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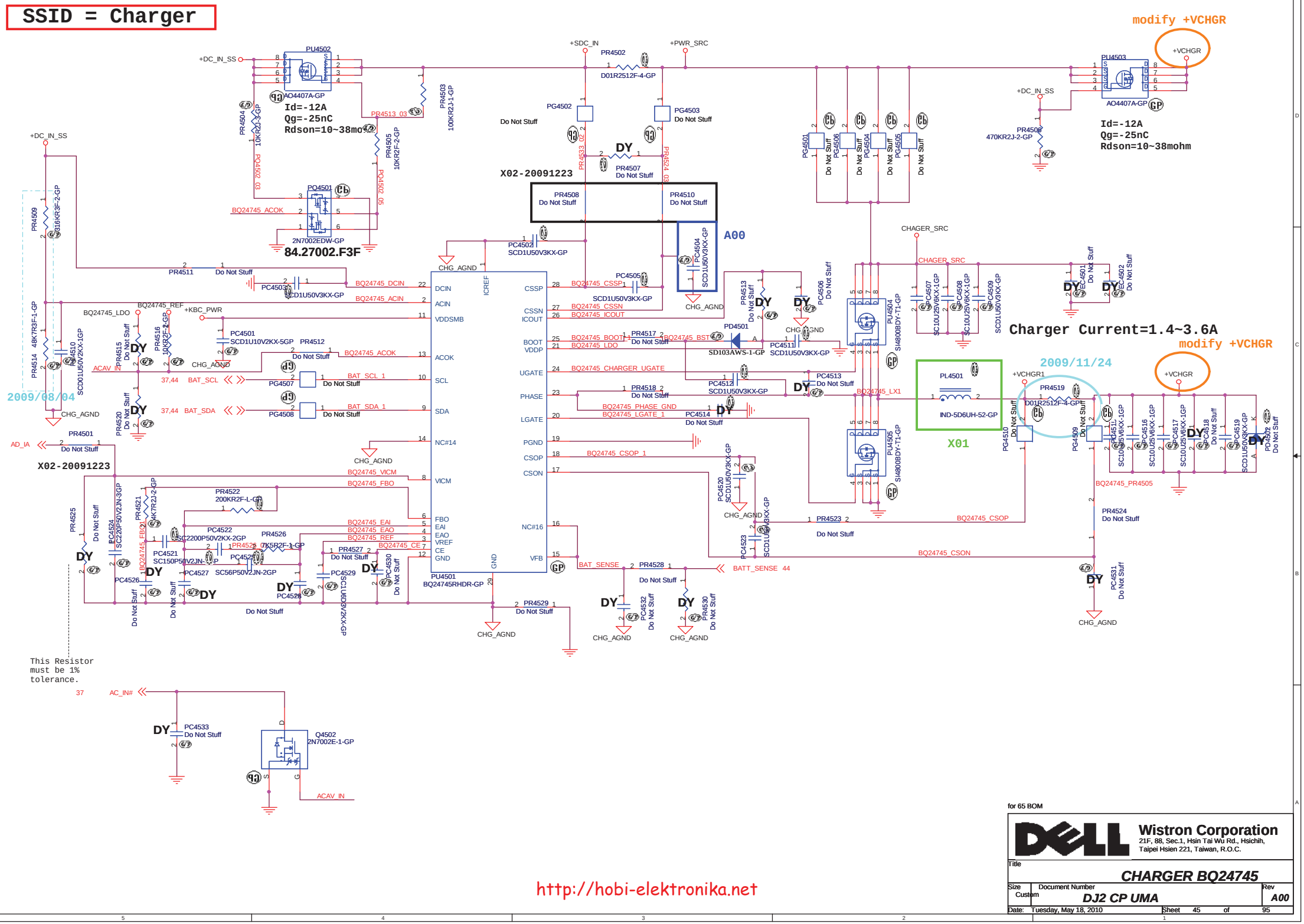
SSID = Charger
modify +VCHGR
+DC_IN_SS
+SDC_IN
+PWR_SRC
+VCHGR
PU4502
AO4407A-GP
Id=-12A
Qg=-25nC
Rdson=10~38mohm
PU4503
AO4407A-GP
Id=-12A
Qg=-25nC
Rdson=10~38mohm
PR4502
D01R2512F-4-GP
PR4503
100KR2J-1-GP
PR4504
10KR2J-3-GP
PR4505
10KR2F-2-GP
PR4508
470KR2J-2-GP
PG4501
PG4502
PG4503
PG4504
PG4505
PG4506
Do Not Stuff
PR4507
Do Not Stuff
X02-20091223
PR4508
Do Not Stuff
PR4510
Do Not Stuff
A00
PQ4501
2N7002EDW-GP
84.27002.F3F
BQ24745_ACOK
PR4511
Do Not Stuff
PC4502
SCD1U50V3KX-GP
PC4503
SCD1U50V3KX-GP
PC4504
SCD1U50V3KX-GP
PC4505
SCD1U50V3KX-GP
CHG_AGND
CHAGER_SRC
Charger Current=1.4~3.6A
2009/08/04
2009/11/24
PR4509
316KR3F-2-GP
PR4514
48K7R3F-1-GP
PC4510
SCD1U50V2KX-1GP
PR4515
Do Not Stuff
PR4516
10KR2F-3-GP
PC4501
SCD1U10V2KX-5GP
PR4512
Do Not Stuff
BQ24745_LDO
BQ24745_REF
+KBC_PWR
ACAV_IN
BQ24745_ACOK
37,44 BAT_SCL
37,44 BAT_SDA
PG4507
PG4508
BAT_SCL_1
BAT_SDA_1
Do Not Stuff
PR4520
Do Not Stuff
PR4501
Do Not Stuff
AD_IA
X02-20091223
PU4501
BQ24745RHDR-GP
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ICREF
BQ24745_DCIN
BQ24745_ACIN
BQ24745_CSSP
BQ24745_CSSN
BQ24745_ICOUT
BQ24745_BOOT
BQ24745_LDO
BQ24745_CHARGER_UGATE
BQ24745_PHASE_GND
BQ24745_LGATE_1
BQ24745_CSOP_1
BQ24745_VICM
BQ24745_FBO
BQ24745_EAI
BQ24745_EAO
BQ24745_REF
BQ24745_CE
BAT_SENSE
BATT_SENSE 44
PR4513
PR4517
PR4518
PR4519
PR4520
PR4521
PR4522
PR4523
PR4524
PR4525
PR4526
PR4527
PR4528
PR4529
PR4530
PR4531
PD4501
SD103AWS-1-GP
PC4511
SCD1U50V3KX-GP
PC4512
SCD1U50V3KX-GP
PC4513
Do Not Stuff
PC4514
Do Not Stuff
PU4504
SI4800BDY-T1-GP
PU4505
SI4800BDY-T1-GP
PL4501
IND-5D6UH-52-GP
X01
BQ24745_LX1
BQ24745_CSOP
BQ24745_CSON
BQ24745_PR4505
PR4524
Do Not Stuff
PC4507
SC10U25V6KX-1GP
PC4508
SC10U25V6KX-1GP
PC4509
SCD1U50V3KX-GP
PC4516
SC10U25V6KX-1GP
PC4517
SC10U25V6KX-1GP
PC4518
Do Not Stuff
PC4519
SCD1U50V3KX-GP
PC4531
Do Not Stuff
PD4502
Do Not Stuff
PC4501
Do Not Stuff
PC4502
Do Not Stuff
PC4506
Do Not Stuff
PC4507
SC10U25V6KX-1GP
PC4508
SC10U25V6KX-1GP
PC4509
SCD1U50V3KX-GP
PC4510
Do Not Stuff
PC4511
SC10U25V6KX-1GP
PC4512
SC10U25V6KX-1GP
PC4513
SC10U25V6KX-1GP
PC4514
SC10U25V6KX-1GP
PC4515
SC10U25V6KX-1GP
PC4516
SC10U25V6KX-1GP
PC4517
SC10U25V6KX-1GP
PC4518
Do Not Stuff
PC4519
SCD1U50V3KX-GP
PC4520
SCD1U50V3KX-GP
PC4521
SC150P50V2JN-1GP
PC4522
SC2200P50V2KX-2GP
PC4523
SCD1U50V3KX-GP
PC4524
SC220P50V2JN-3GP
PC4525
Do Not Stuff
PC4526
PC4527
SC56P50V2JN-2GP
PC4528
PC4529
SC1U6V2KX-5GP
PC4530
Do Not Stuff
PC4531
Do Not Stuff
PR4521
4K7R2J-2-GP
PR4522
200KR2F-L-GP
PR4523
Do Not Stuff
PR4524
Do Not Stuff
PR4525
Do Not Stuff
PR4526
7K5R2F-1-GP
PR4527
Do Not Stuff
PR4528
Do Not Stuff
PR4529
Do Not Stuff
PR4530
Do Not Stuff
This Resistor must be 1% tolerance.
37 AC_IN#
Q4502
2N7002E-1-GP
PC4533
Do Not Stuff
ACAV_IN
for 65 BOM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER BQ24745
Size Custom
Document Number
DJ2 CP UMA
Rev
A00
Date: Tuesday, May 18, 2010
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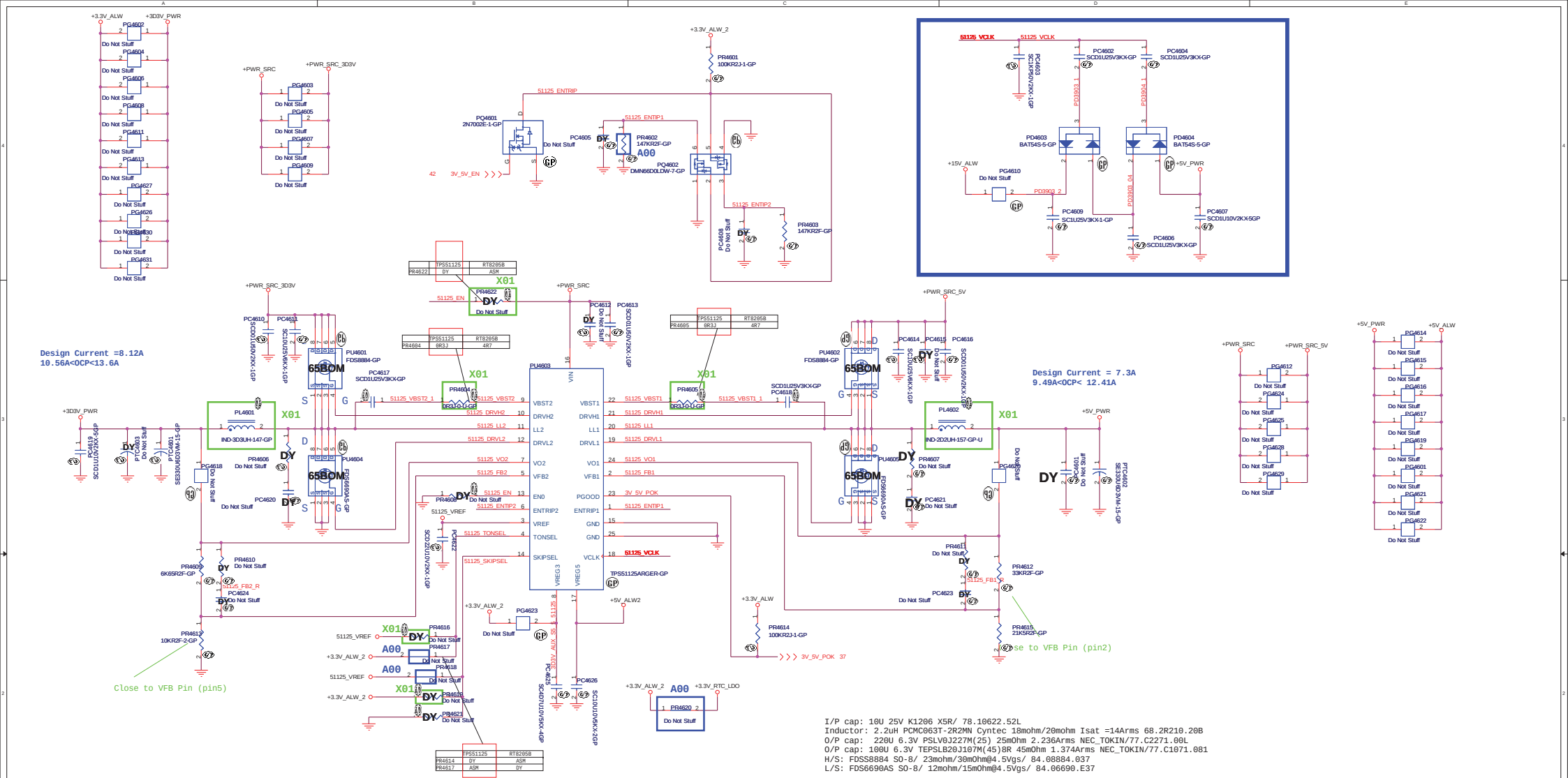


I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMB104T-3R3MS Cyntec 10.8mohm/11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

RT8205B:

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

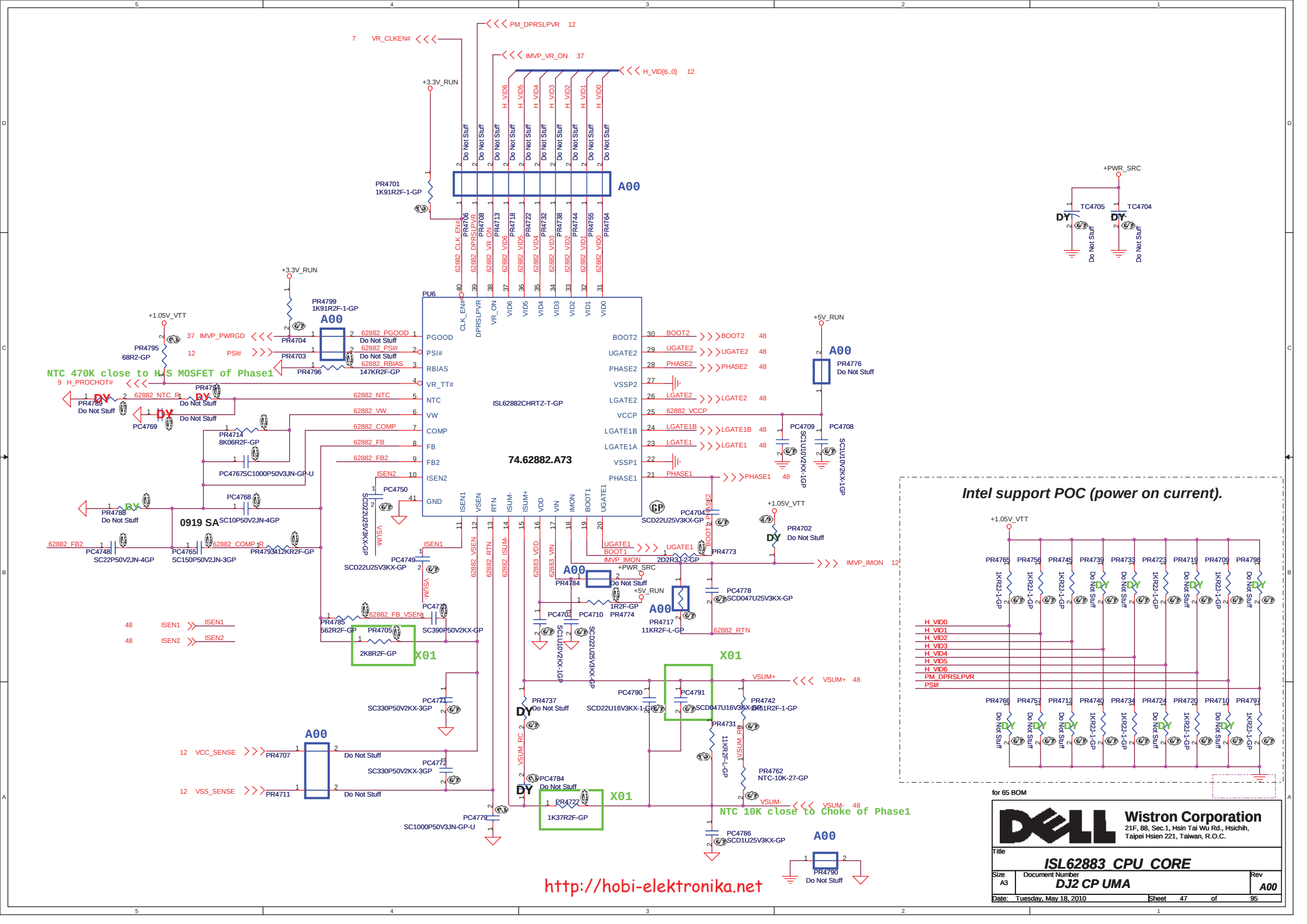
for 65 BOM

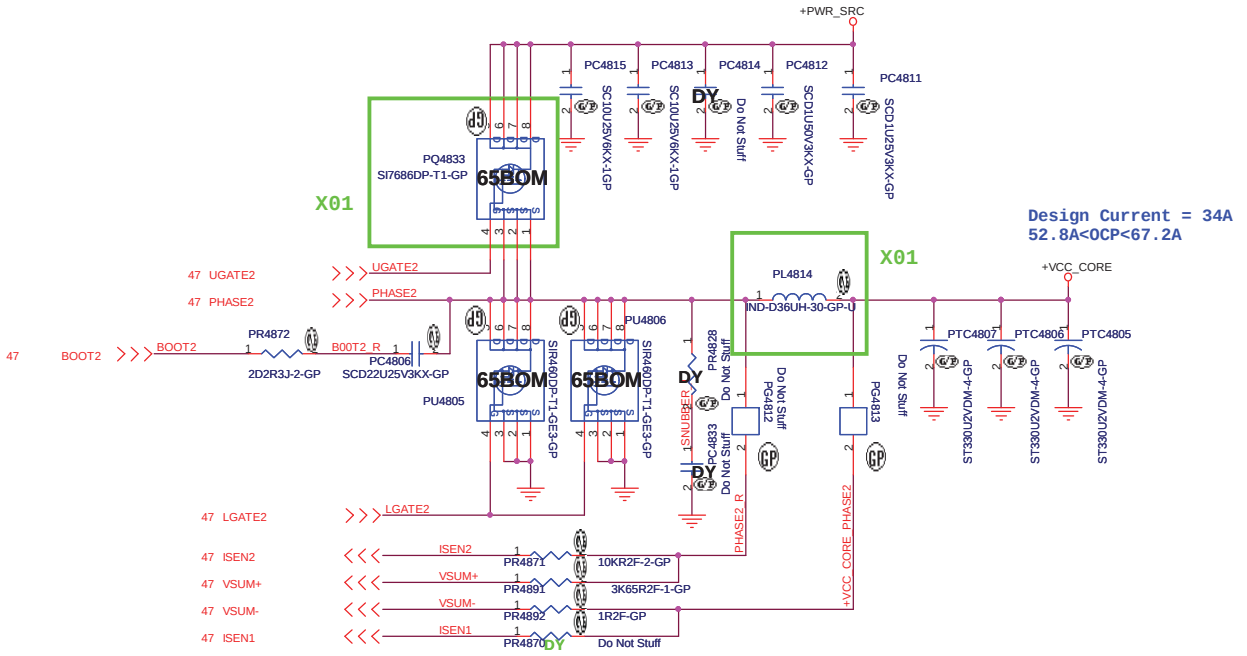
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

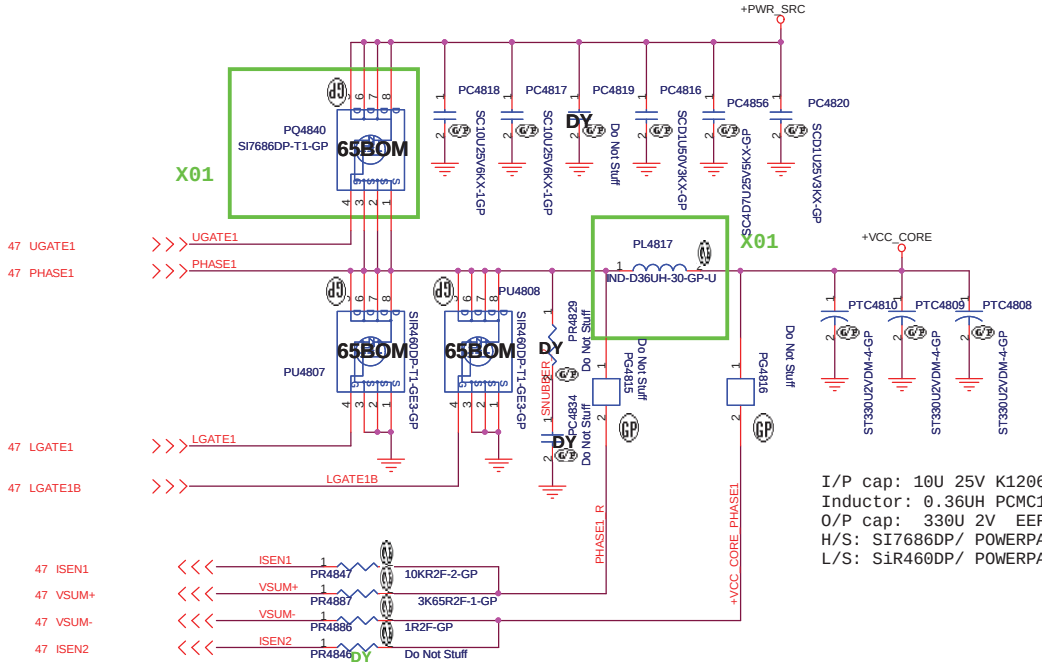
Title: TPS51125_5V/3D3V

Size: A2 | Document Number: DJ2 CP UMA | Rev: A00

Date: Tuesday, May 18, 2010 | Sheet 46 of 90


PM_DPRSLPVR 12
IMVP_VR_ON 37
H_VID[6..0] 12
VR_CLKEN# 7
+3.3V_RUN
PR4701 1K91R2F-1-GP
A00
Do Not Stuff
PU6
ISL62882CHRTZ-T-GP
74.62882.A73
PGOOD
PSI#
RBIAS
VR_TT#
NTC
VW
COMP
FB
FB2
ISEN2
GND
BOOT2
UGATE2
PHASE2
VSSP2
LGATE2
VCCP
LGATE1B
LGATE1A
VSSP1
PHASE1
ISEN1
VSEN
RTN
ISUM-
ISUM+
VDD
VIN
IMON
BOOT1
UGATE1
+1.05V_VTT
+5V_RUN
+PWR_SRC
NTC 470K close to H/S MOSFET of Phase1
NTC 10K close to Choke of Phase1
0919 SA
X01
IMVP_IMON 12
VSUM+ 48
VSUM- 48
VCC_SENSE 12
VSS_SENSE 12
ISEN1 48
ISEN2 48
Intel support POC (power on current).
for 65 BOM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62883_CPU_CORE
Size A3
Document Number DJ2 CP UMA
Rev A00
Date: Tuesday, May 18, 2010
Sheet 47 of 95
http://hobi-elektronika.net





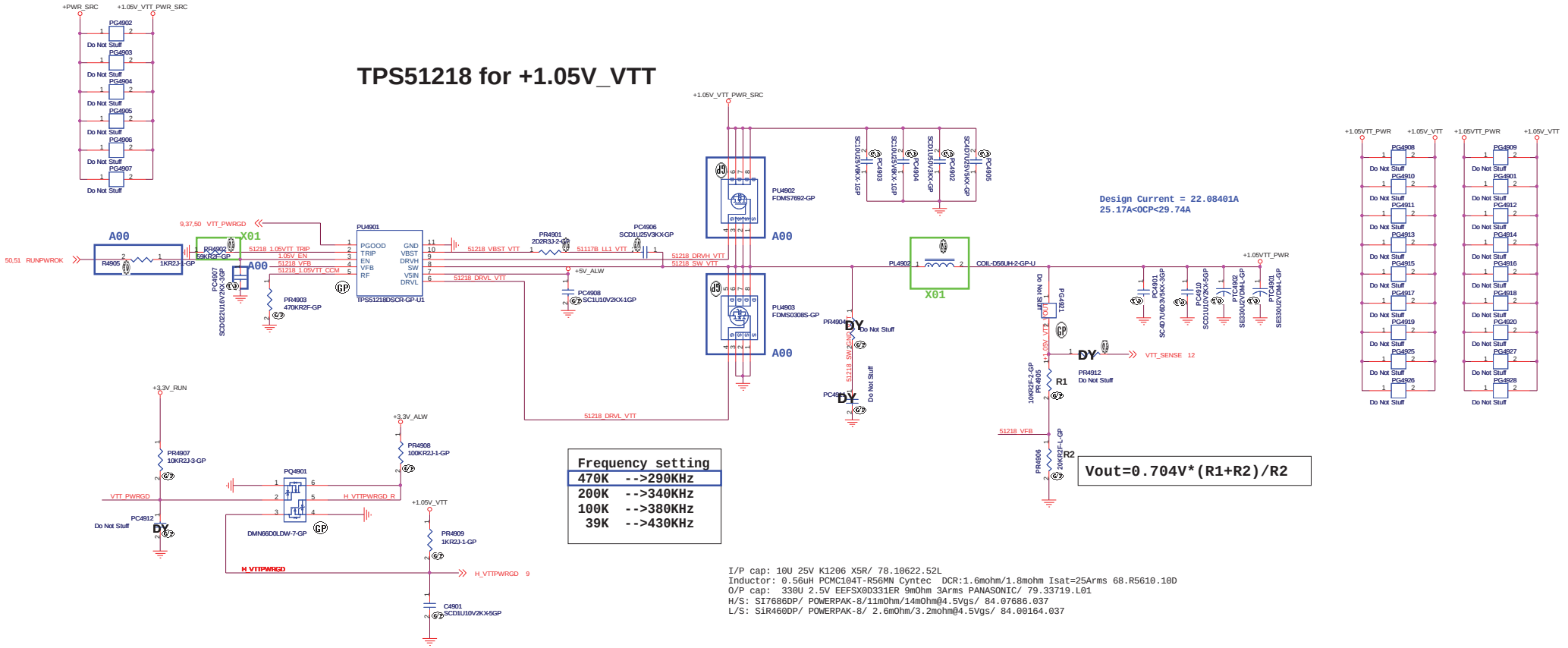
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J Cyntec 1.05mohm/ 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62883 CPU CORE
Size: A3 | Document Number: DJ2 CP UMA | Rev: A00
Date: Tuesday, May 18, 2010 | Sheet 48 of 95

TPS51218 for +1.05V_VTT



Frequency setting
470K -->290KHz
200K -->340KHz
100K -->380KHz
39K -->430KHz

Vout=0.704V*(R1+R2)/R2

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 2.6mOhm/3.2mohm@4.5Vgs/ 84.00164.037

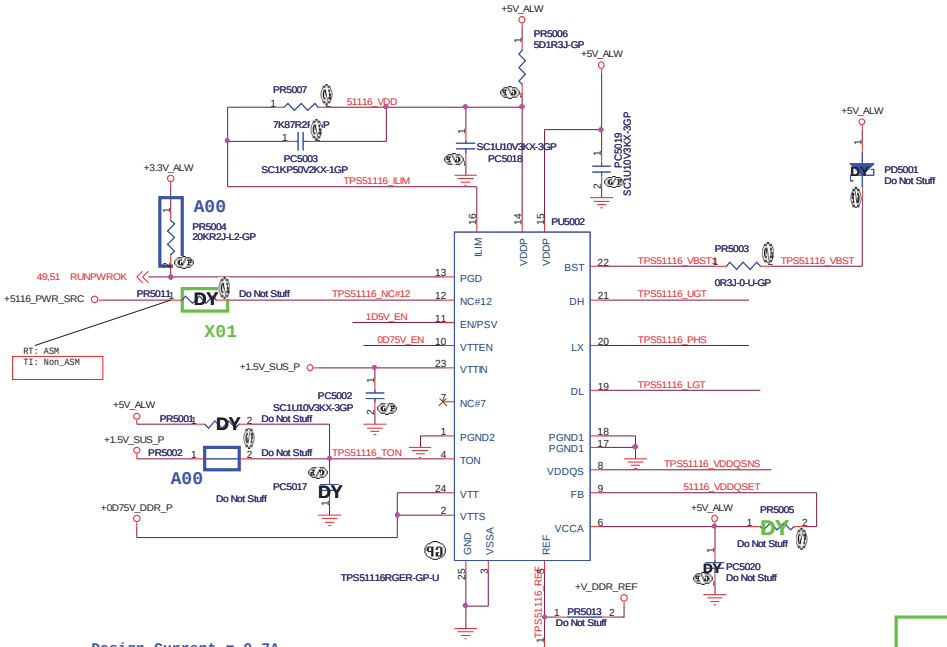
for 65 BOM

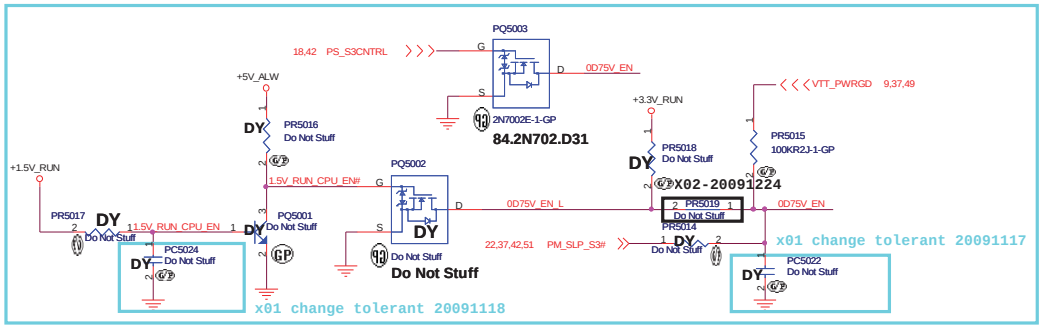
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

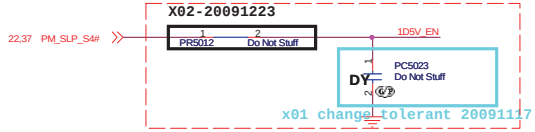
Title	TPS51218 +1.05V_VTT	
Size A2	Document Number DJ2 CP UMA	Rev A00
Date: Tuesday, May 18, 2010	Sheet 49 of 95	

SSID = PWR.Plane.Regulator_1p5v0p75v

5 S3 Power Reduction X01 20091111







Design Current = 0.7A

Design Current = 10.51A
13.66A<OCP< 17.88A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5uH PCMC104T-1R5 Cyntec DCR:3.8mohm Isat=33Arms 68.1R510.10J
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->400KHz

Close to VFB Pin (pin5)

for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

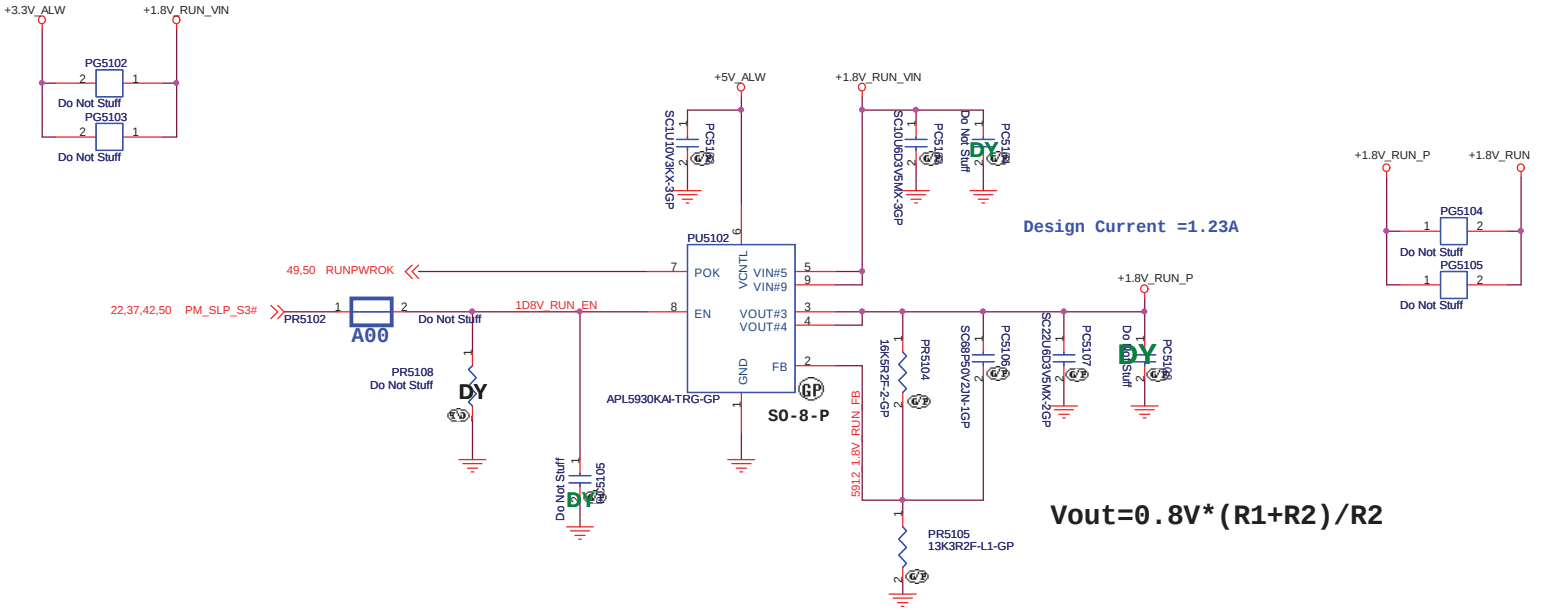
Title: TPS51116 +1.5V SUS

Size	Document Number	Rev
Custom	DJ2 CP UMA	A00

Date: Tuesday, May 18, 2010 Sheet 50 of 95

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



Vout=0.8V*(R1+R2)/R2

http://hobi-elektronika.net

for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	APL5930 +1.8V RUN	
Size: A3	Document Number: DJ2 CP UMA	Rev: A00
Date: Tuesday, May 18, 2010	Sheet 51 of 95	

(Blanking)

for 65 BOM

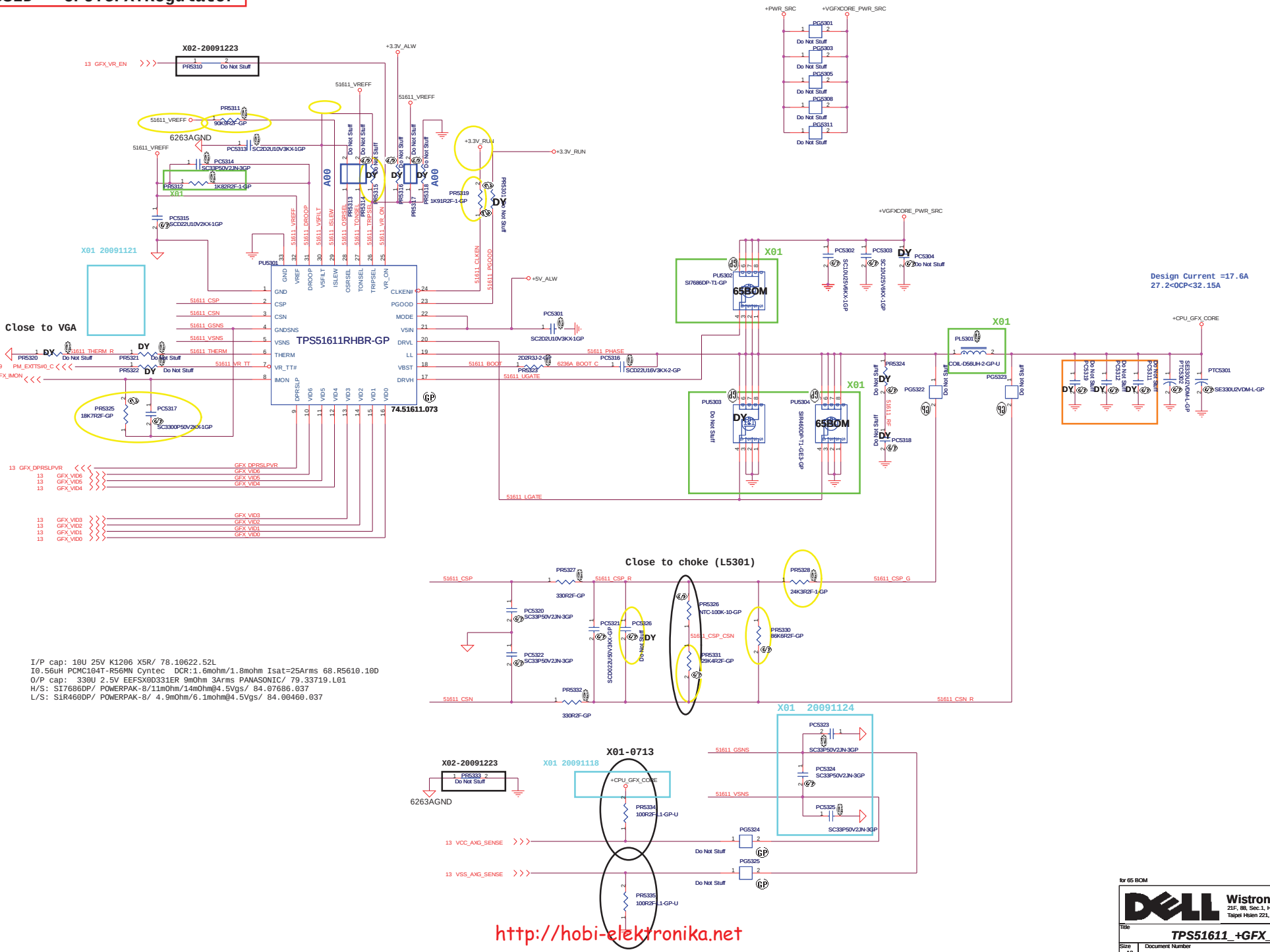
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ2 CP UMA*	*A00*

Date: Tuesday, May 18, 2010 Sheet 52 of 95

SSID = CPU.GFX.Regulator



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
I0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

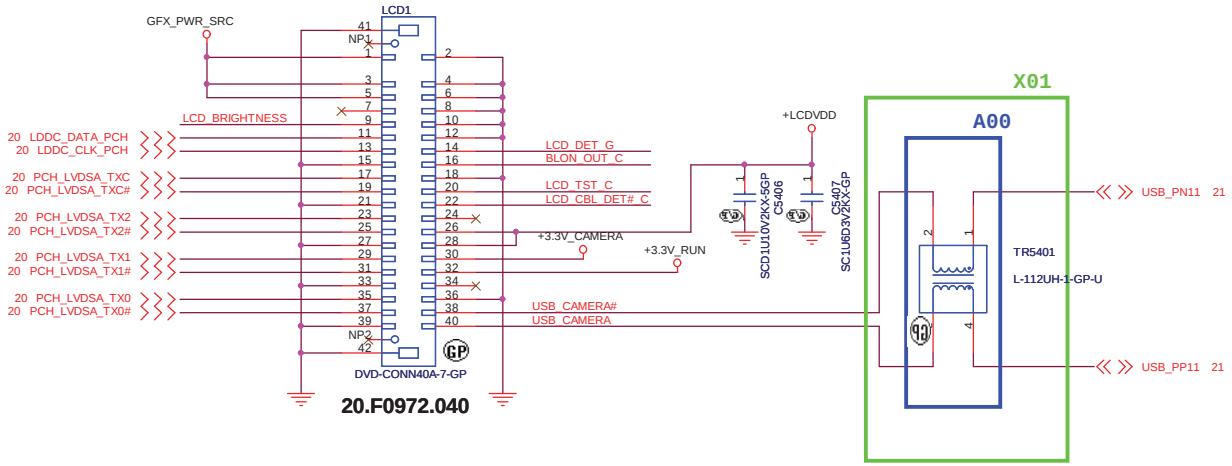
Title: TPS51611_+GFX_CORE

Size	Document Number	Rev
A2	DJ2 CP UMA	A00

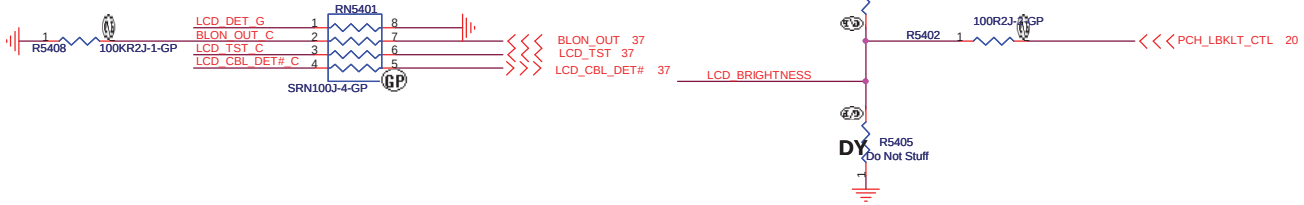
Date: Tuesday, May 18, 2010 Sheet 53 of 95

SSID = VIDEO

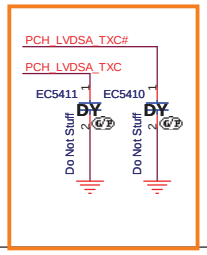
LVDS CONNECTOR

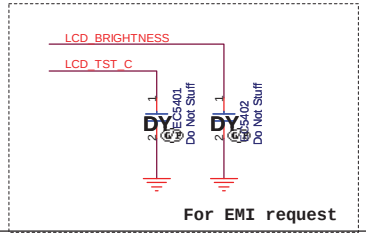


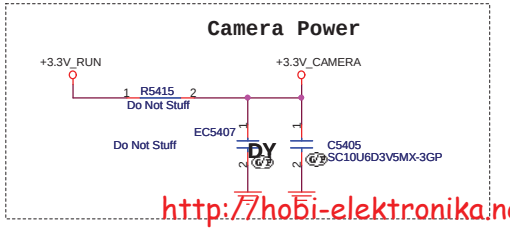
20.F0972.040



Close to LVDS connector

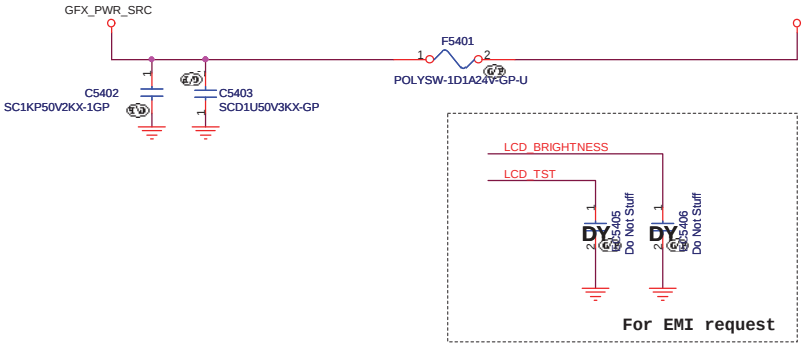






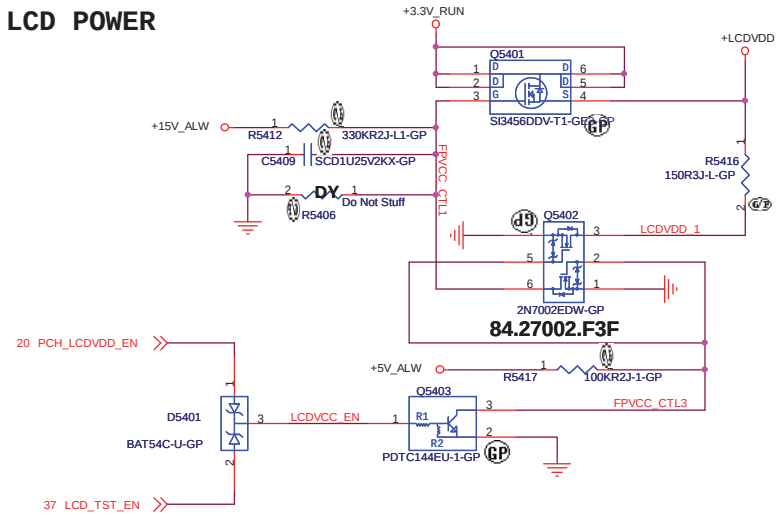
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER

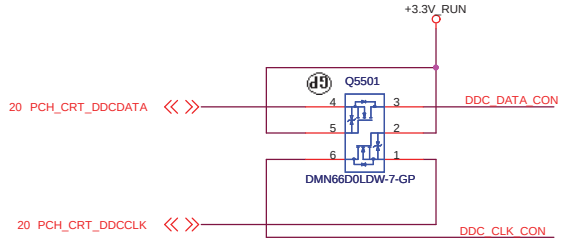


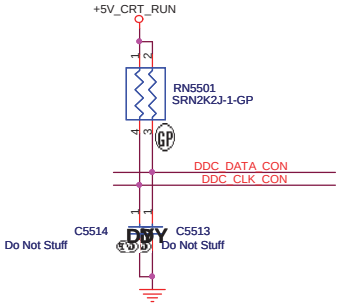
for 65 BOM

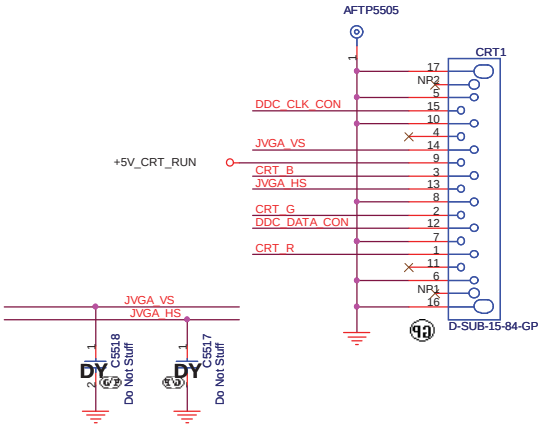
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector		
Size: A3	Document Number: DJ2 CP UMA	Rev: A00
Date: Tuesday, May 18, 2010	Sheet 54 of 95	

SSID = VIDEO

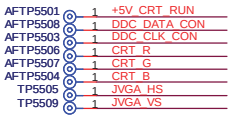


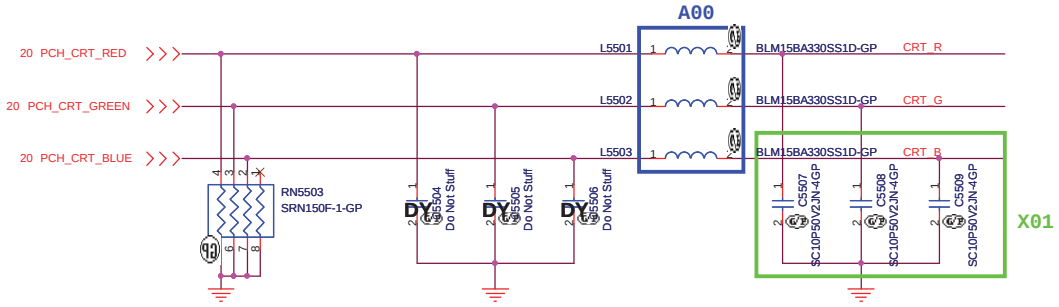


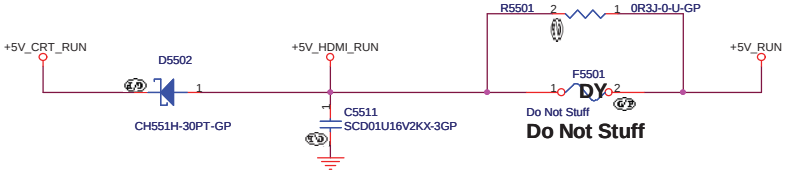


Layout Note:

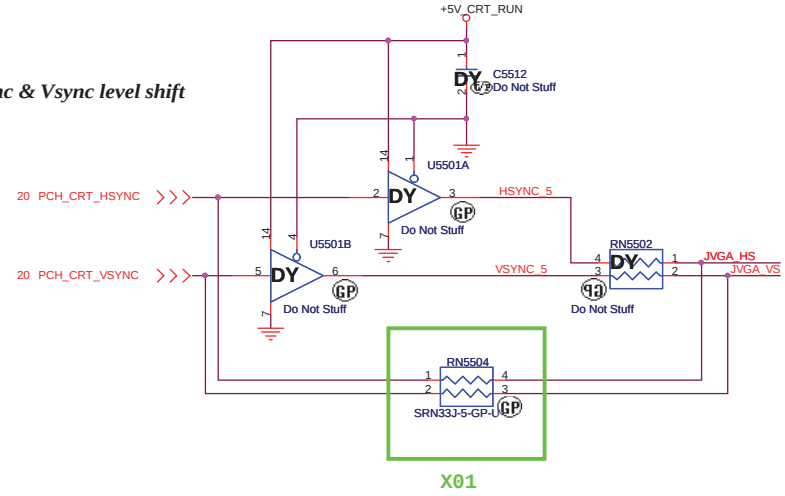
***Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.**
*** RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.**

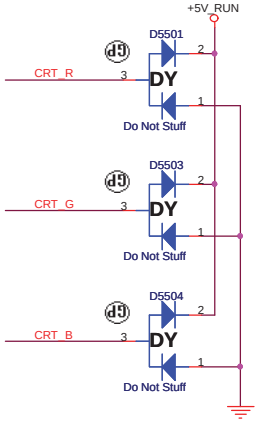


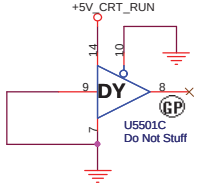


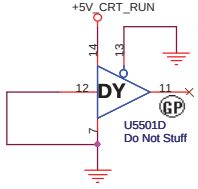


Hsync & Vsync level shift









for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT Connector	
Size	Document Number: DJ2 CP UMA	Rev: A00
Date: Tuesday, May 18, 2010	Sheet 55 of 95	

(Blanking)

for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

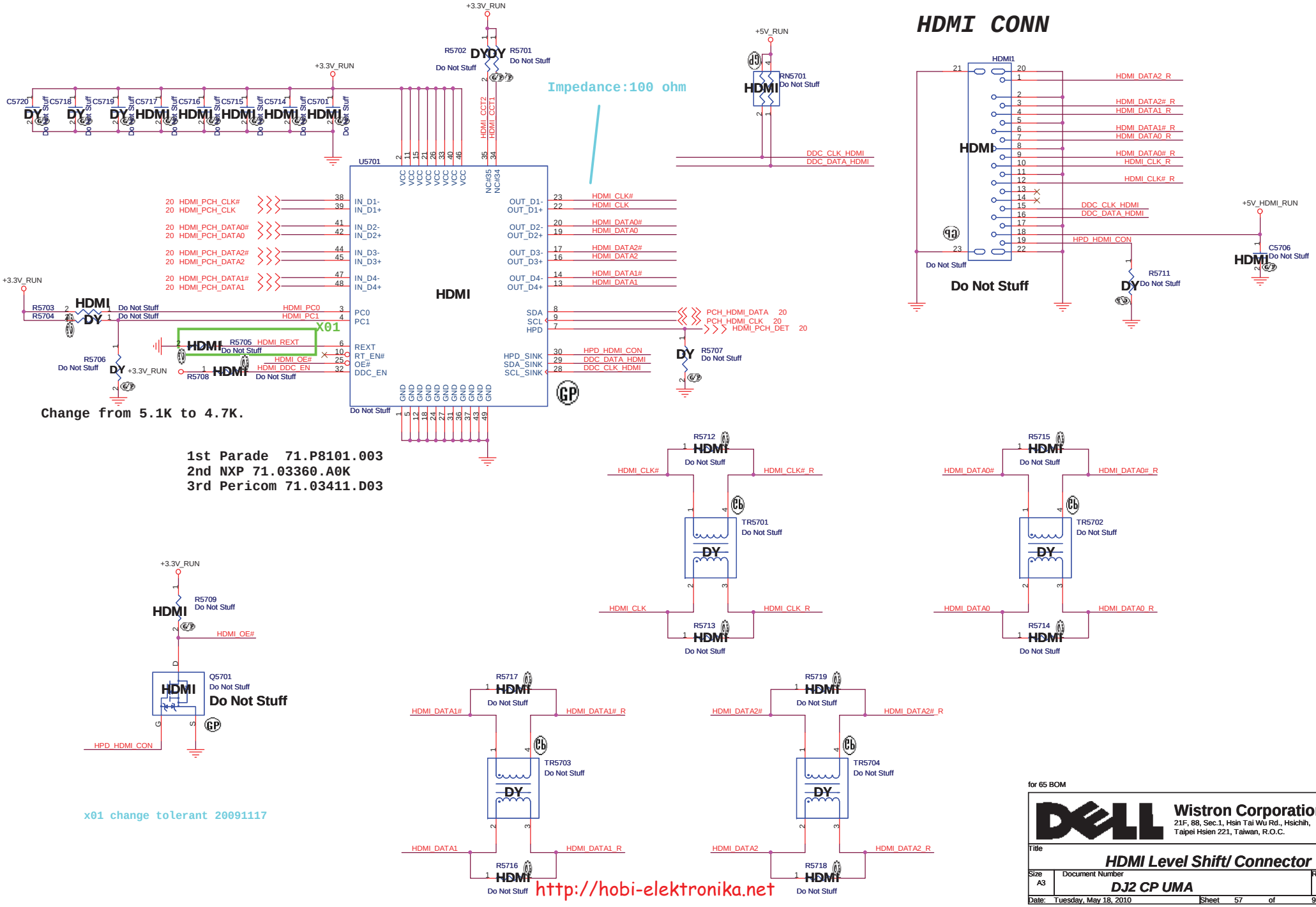
Title: Reserved

Size: A3 | Document Number: DJ2 CP UMA | Rev: A00

Date: Tuesday, May 18, 2010 | Sheet 56 of 95

SSID = VIDEO

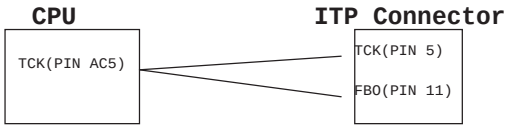
HDMI Level Shifter & CONNECTOR



SSID = User.Interface

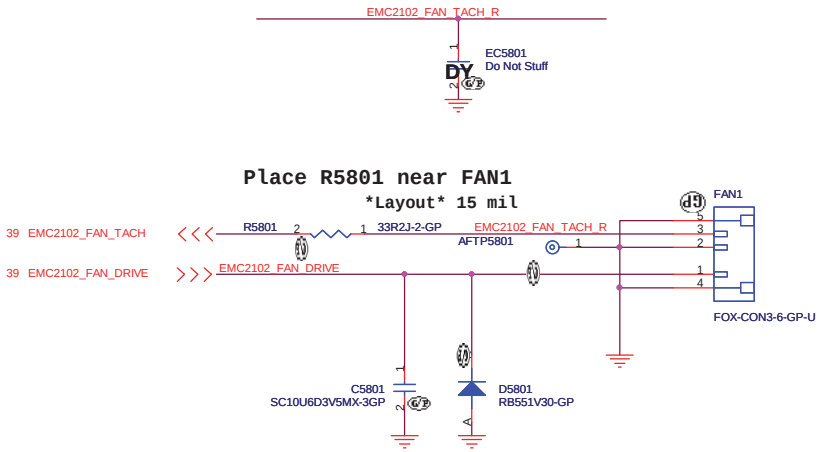
ITP Connector

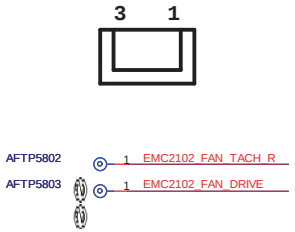
H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



SSID = Thermal

Fan Connector



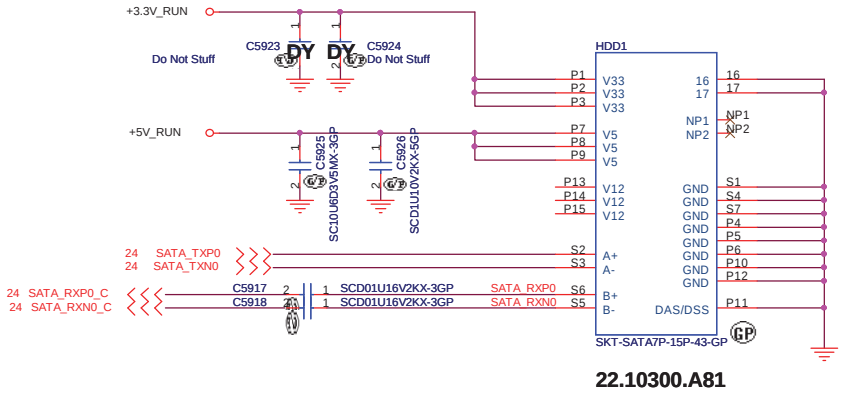


for 65 BOM

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ITP/Fan Connector		
Size: A3	Document Number: DJ2 CP UMA	Rev: A00
Date: Tuesday, May 18, 2010	Sheet 58 of 95	

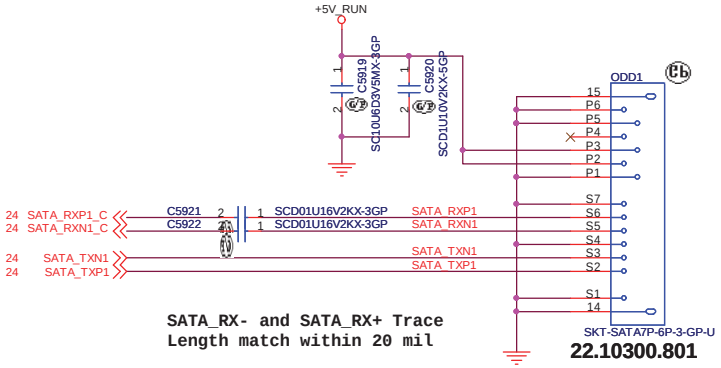
SSID = SATA

SATA HDD Connector



22.10300.A81

SATA ODD Connector



SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

22.10300.801

for 65 BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

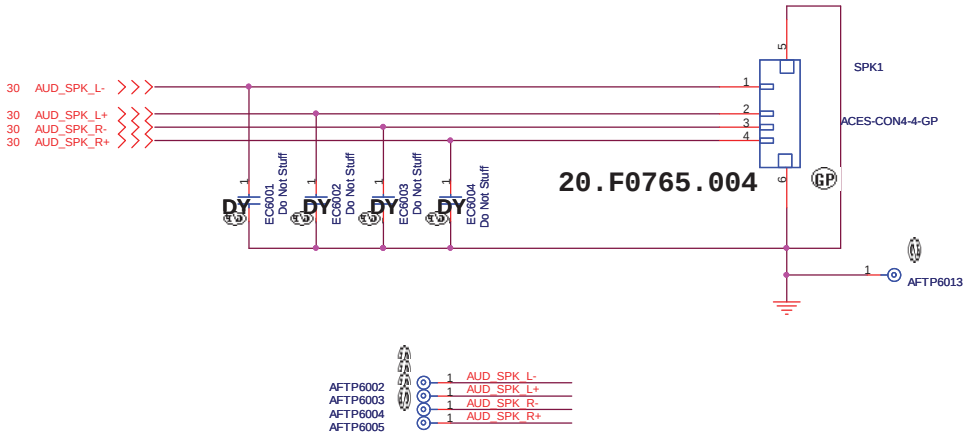
Title: HDD/ODD

Size	Document Number	Rev
A3	DJ2 CP UMA	A00

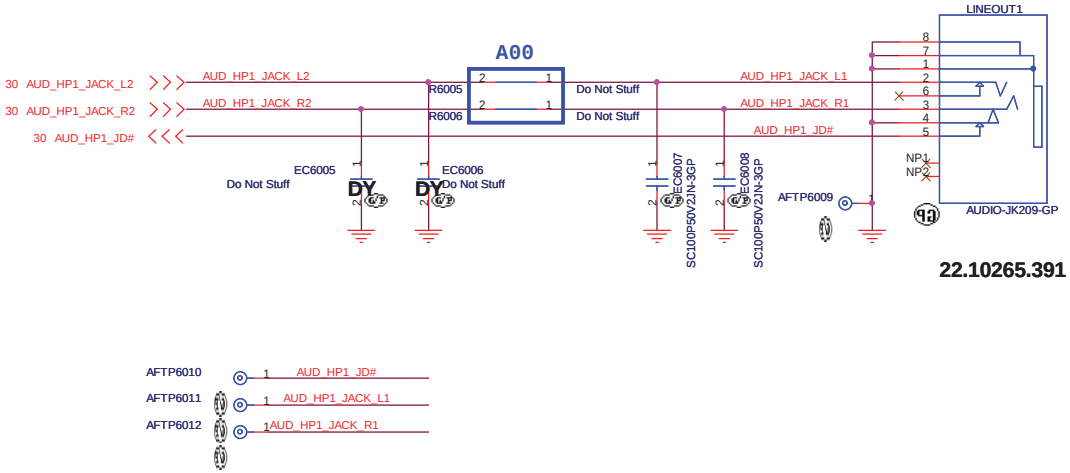
Date: Tuesday, May 18, 2010 Sheet 59 of 95

SSID = AUDIO

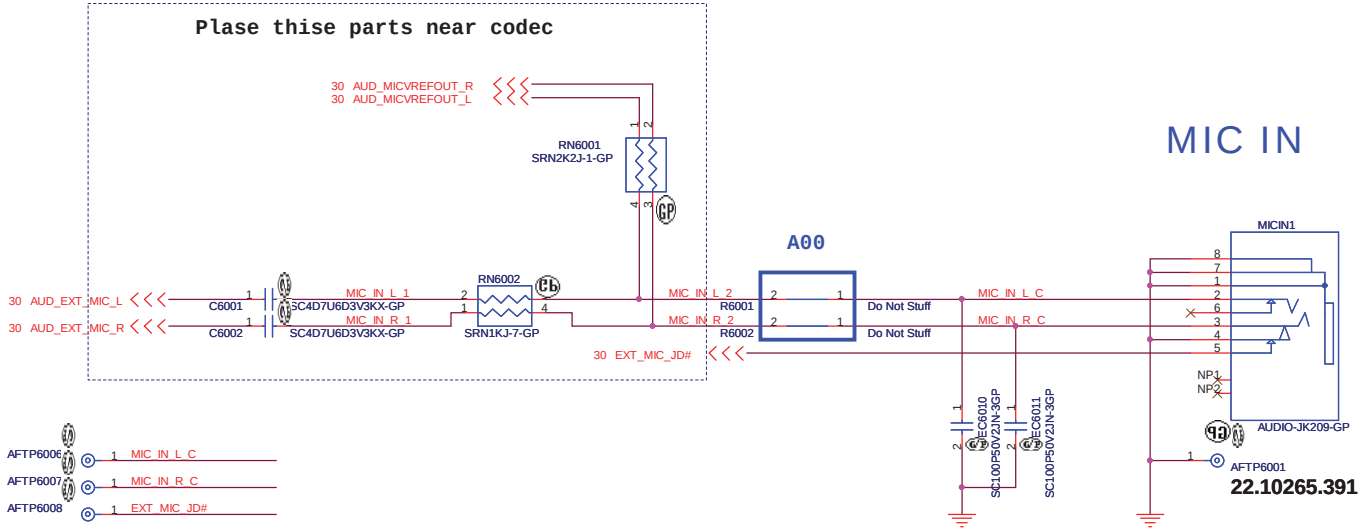
Speaker Connector



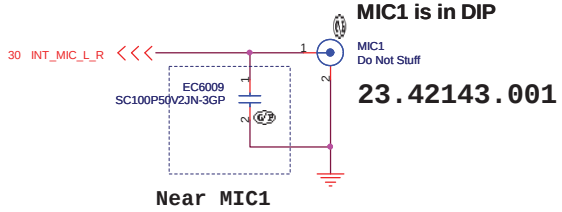
LINE1 OUT



MIC IN



Internal Microphone



for 65 BOM

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Title: **Audio Jack**

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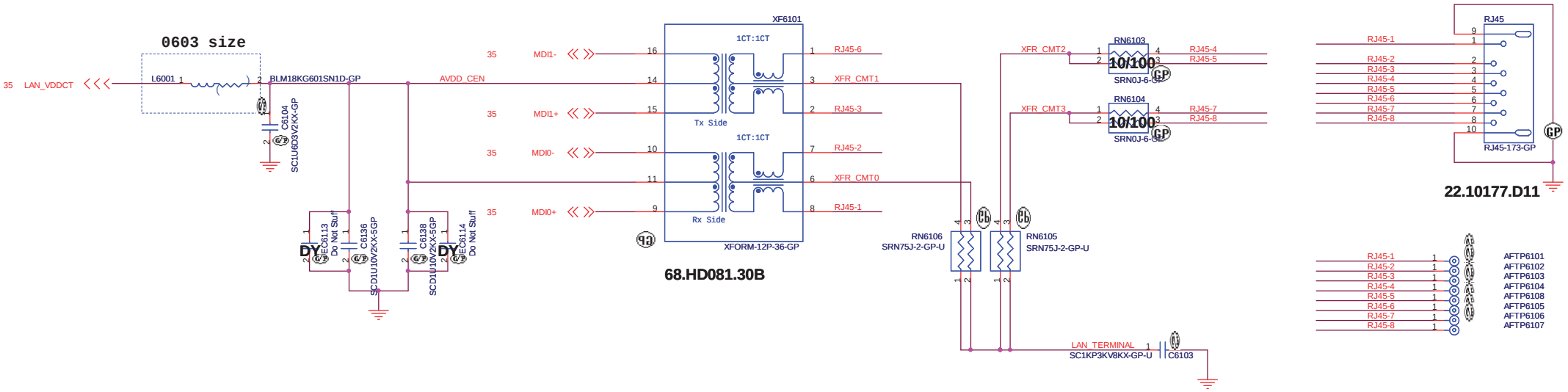
RJ45 Connector

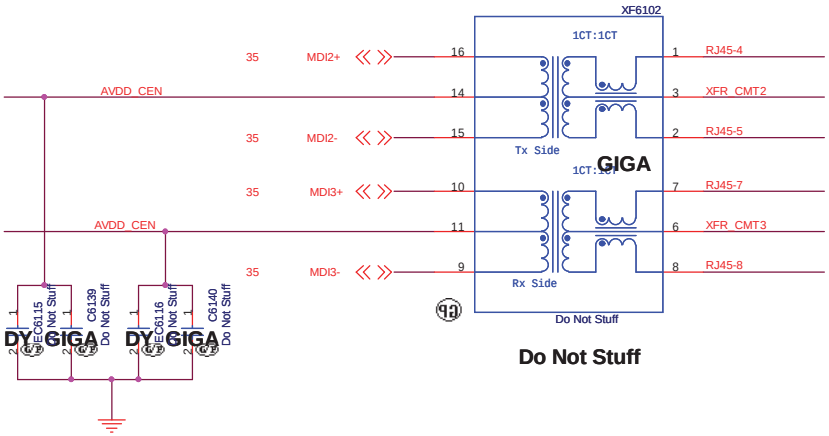
2009-10-1 Change MDI1+(XF601.16) to MDI1+(XF601.15)
Change MDI1-(XF601.15) to MDI1-(XF601.16)
Change MDI0+(XF601.10) to MDI0+(XF601.9)
Change MDI0-(XF601.9) to MDI0-(XF601.10)
Change RJ45-3(XF601.1) to RJ45-3(XF601.2)
Change RJ45-6(XF601.2) to RJ45-6(XF601.1)
Change RJ45-1(XF601.7) to RJ45-1(XF601.8)
Change RJ45-2(XF601.8) to RJ45-2(XF601.7)

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

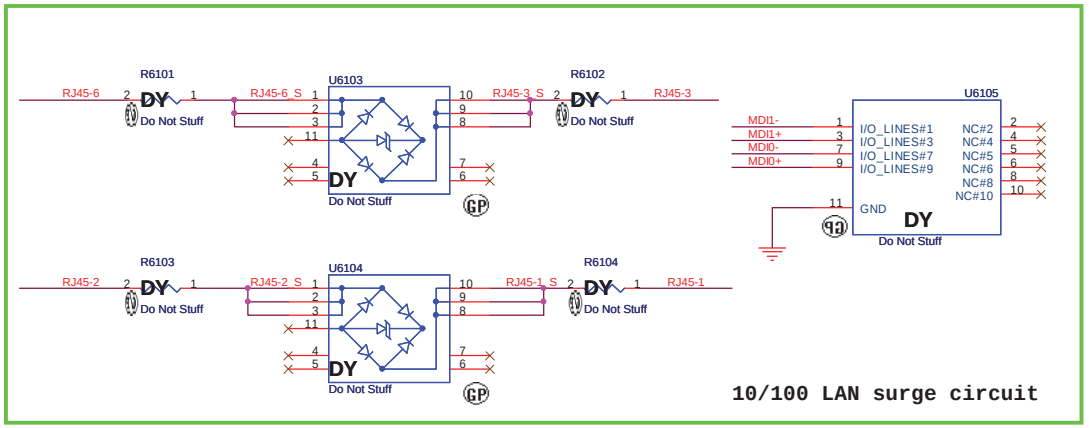
10/100M Lan Transformer



LAN differential signals use 100 Ohm impedance



Do Not Stuff



X01
for 65 BOM

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Title: XFORM/RJ45
Size: A3 | Document Number: DJ2 CP UMA | Rev: A00
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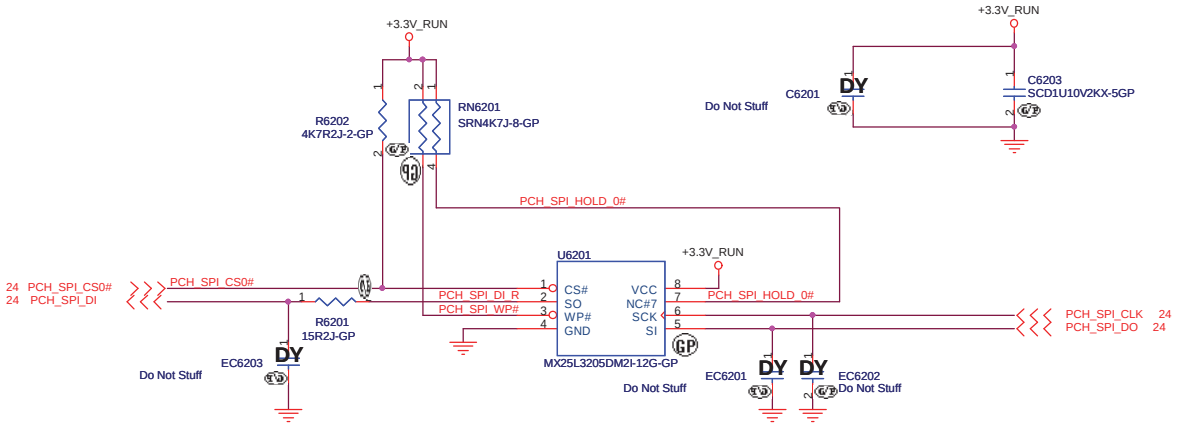
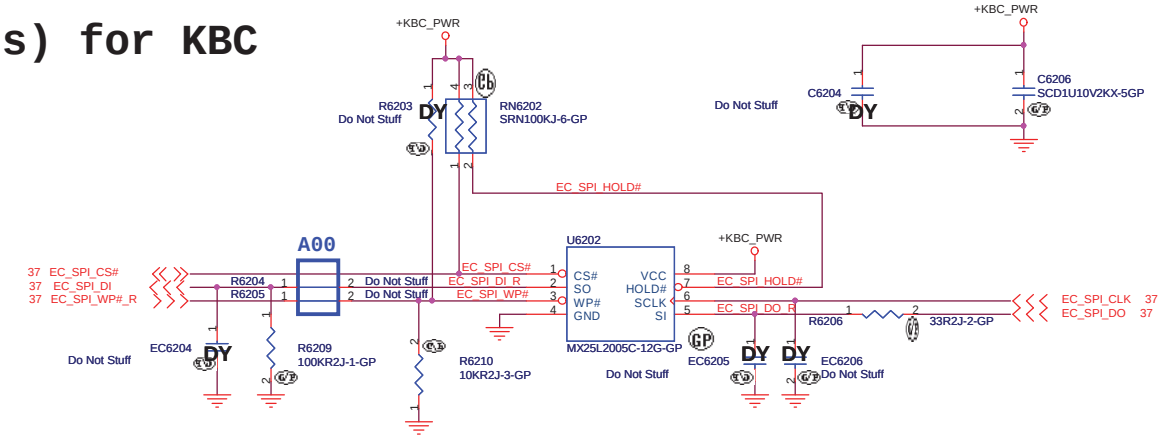
SSID = Flash.ROM

SPI FLASH ROM (32M bits) for PCH

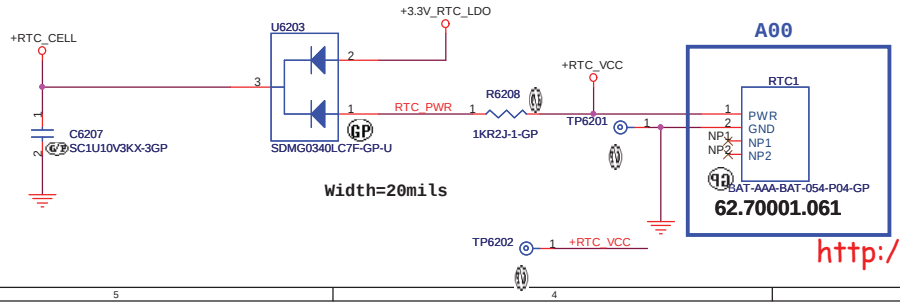


SPI FLASH ROM (2M bits) for KBC



SSID = RBATT

RTC Connector



for 65 BOM

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Title: Flash/RTC

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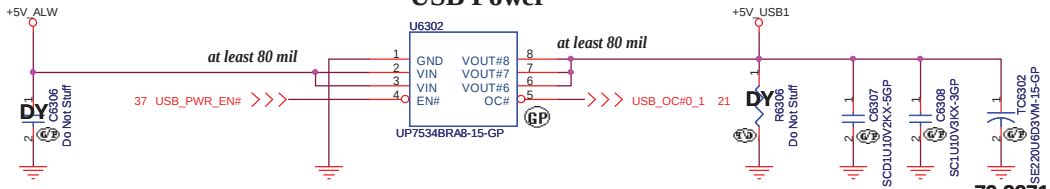
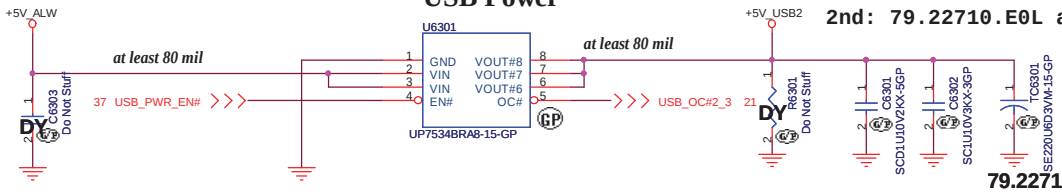
SSID = USB

USB Power



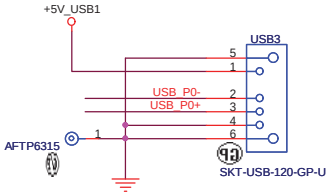
79.22710.3CL

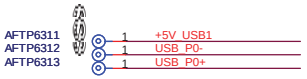


79.22710.3CL

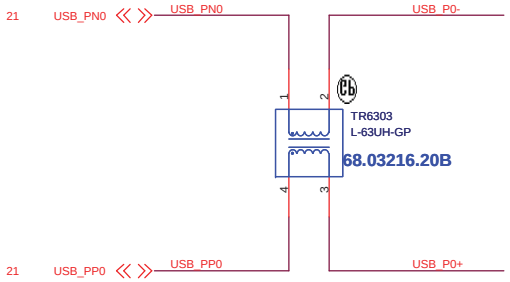
2nd: 79.22710.E0L and 77.92271.021

2nd: 79.22710.E0L and 77.92271.021

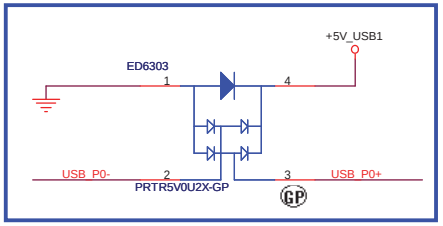


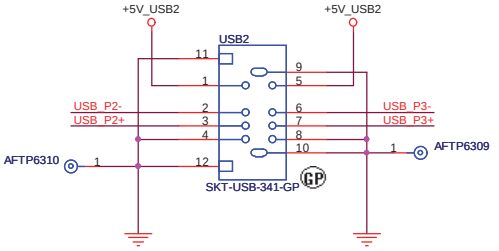


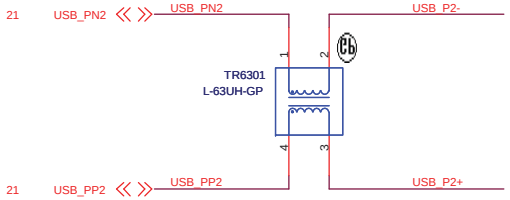
USB Socket

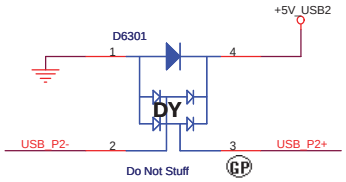


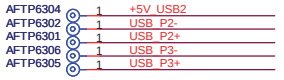
A00

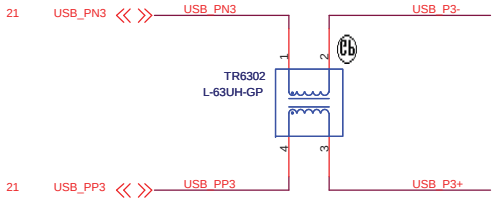


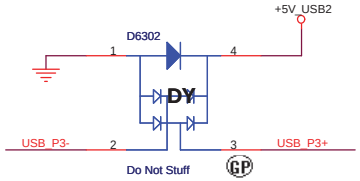












http://hobi-elektronika.net

for 65 BOM

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Title: USB		
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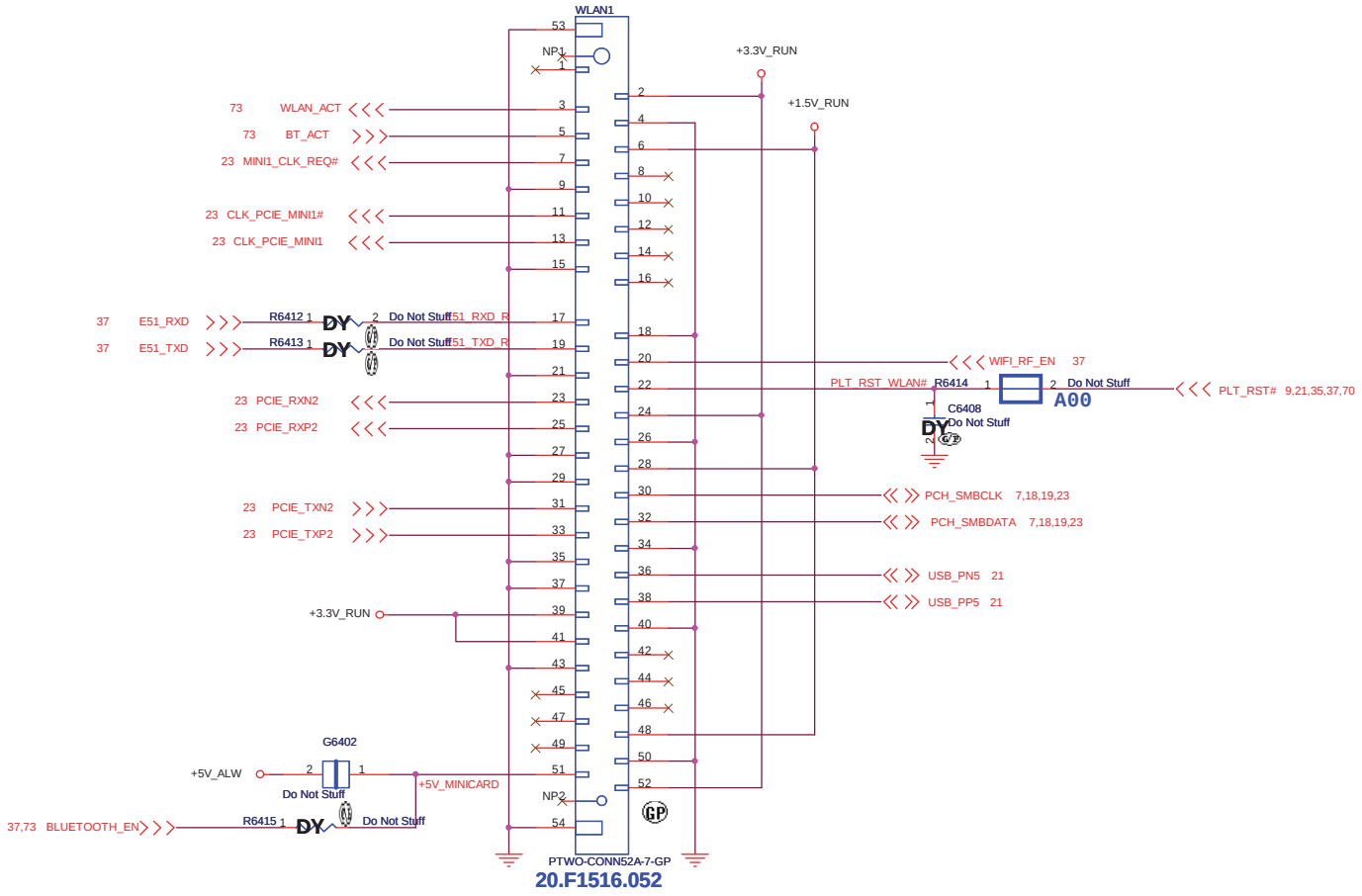
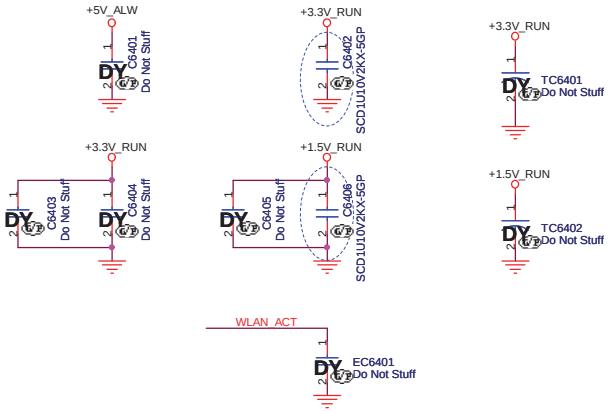
SSID = Wireless

Mini Card Connector(802.11a/b/g)





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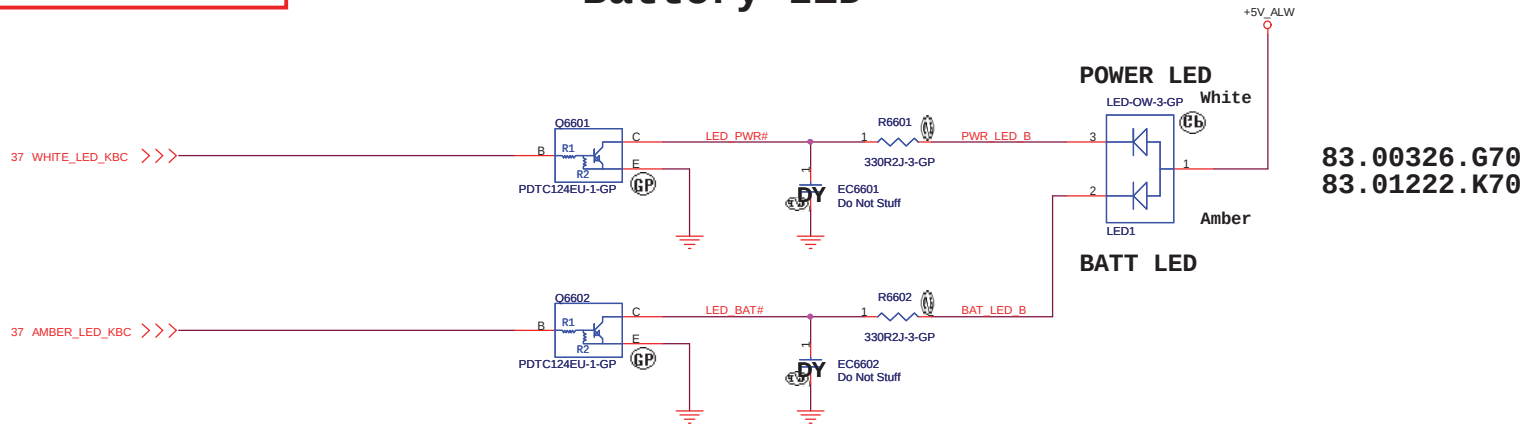
SSID = User.Interface

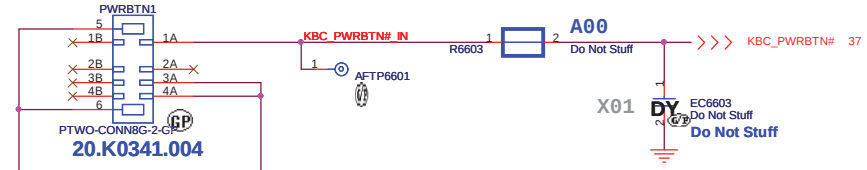
Battery LED



83.00326.G70
83.01222.K70

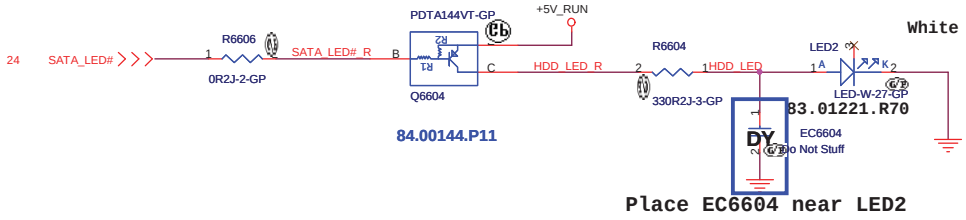
SSID = User.Interface

Power BTN Connector



2ND: 20.K0464.004

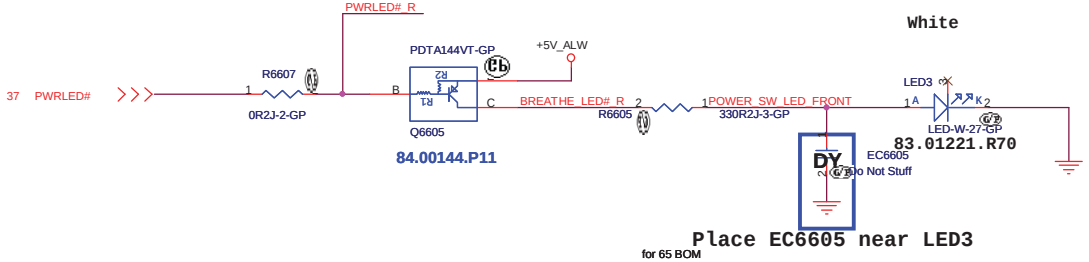
HDD LED



84.00144.P11

83.01221.R70

BREATHE PWR LED (Front)



84.00144.P11

83.01221.R70

for 65 BOM

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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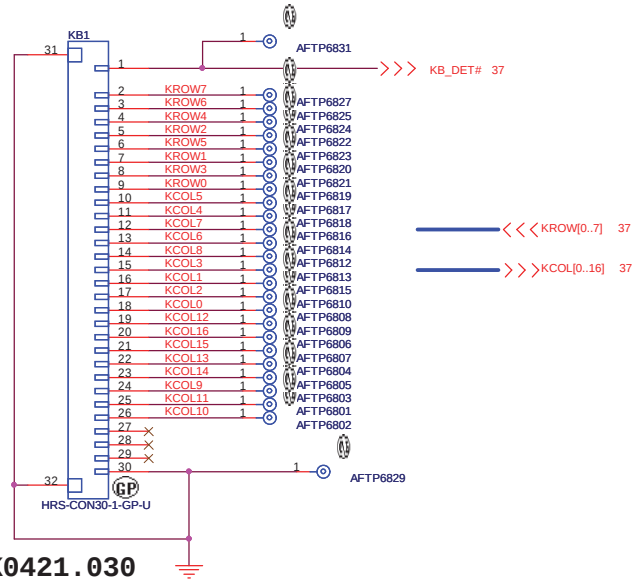
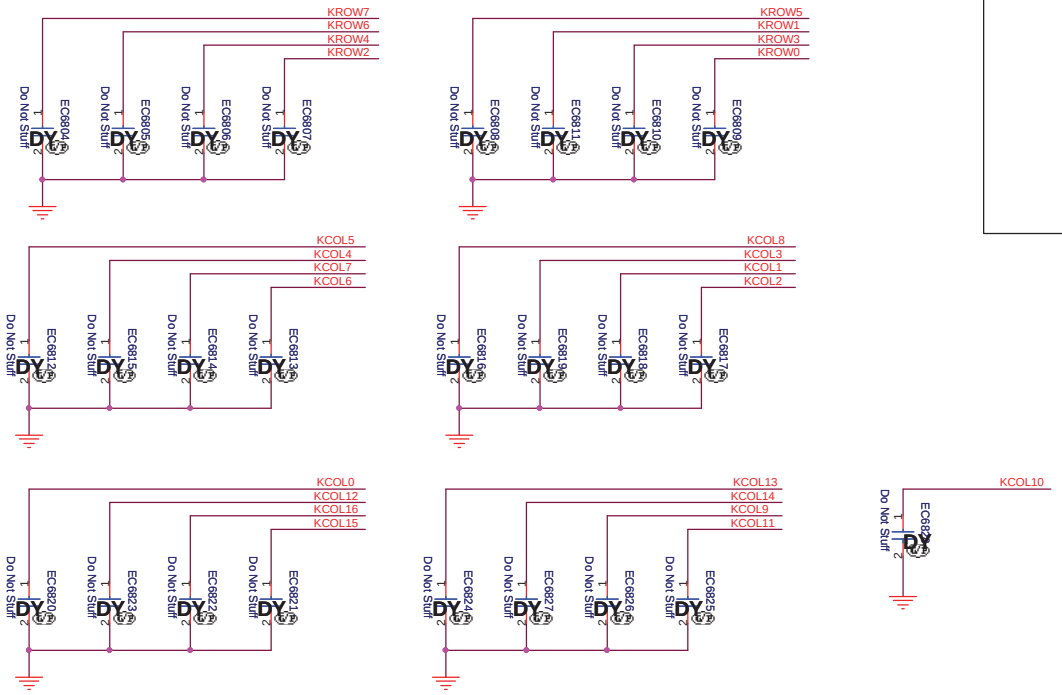
SSID = KBC

Internal KeyBoard Connector

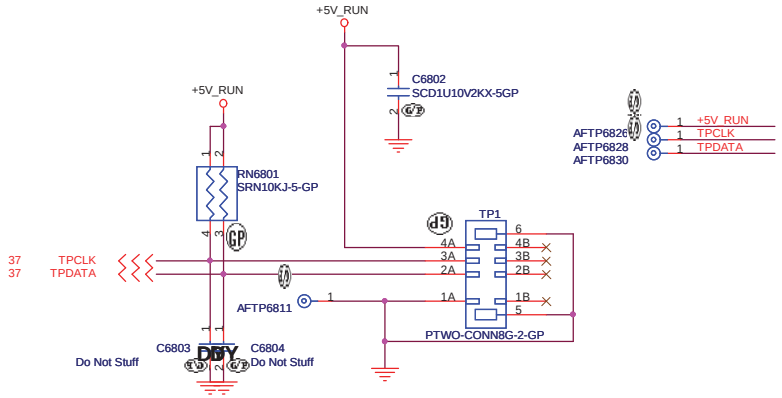


Main 20.K0421.030
20.K0259.030



SSID = Touch.Pad

TouchPad Connector



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Title: Key Board/Touch Pad

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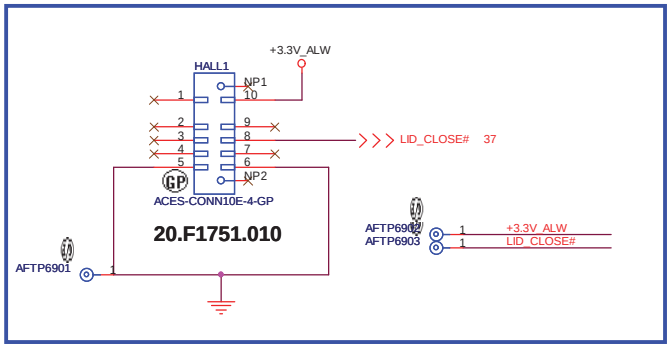
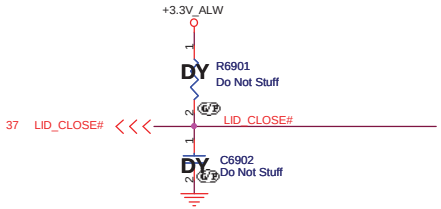


A00



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Title: Hall Sensor

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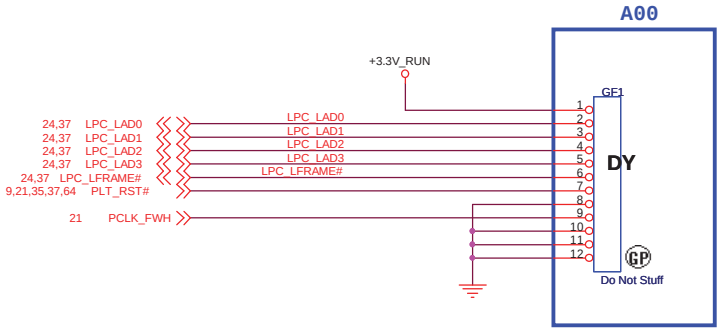

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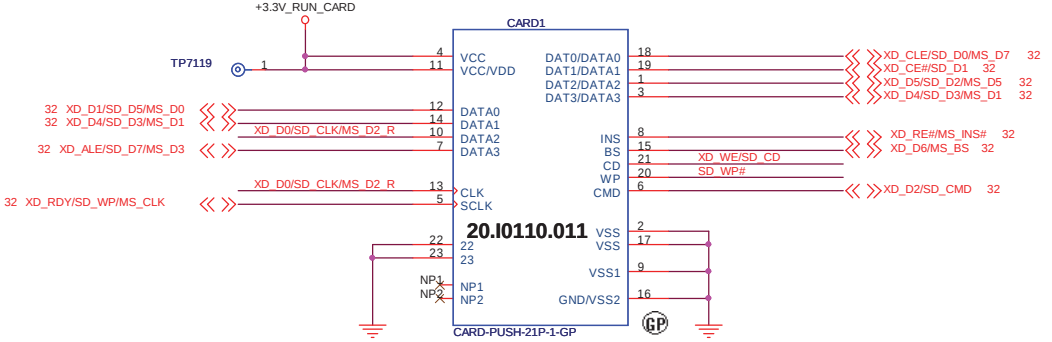
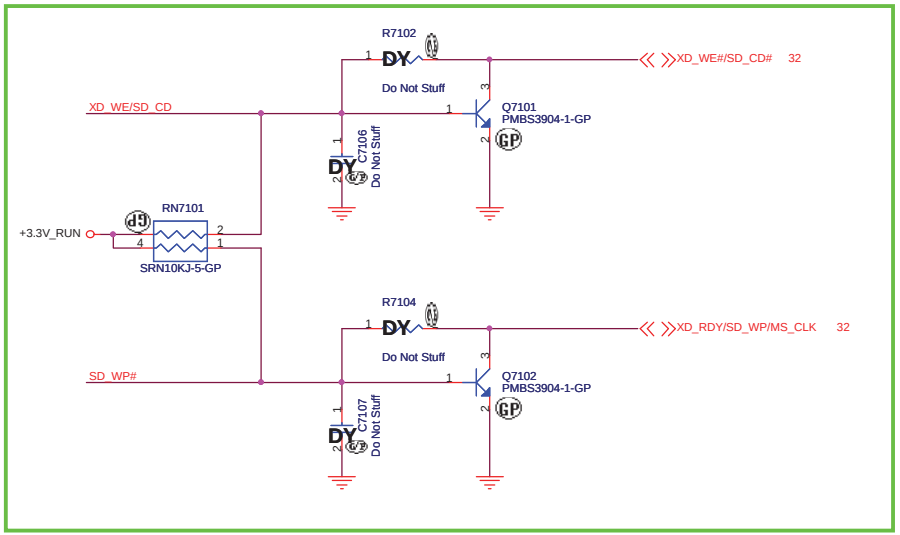
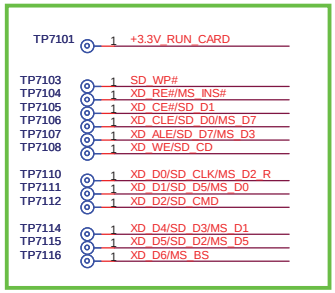
SSID = SDIO

SD/XD/MS Card Reader

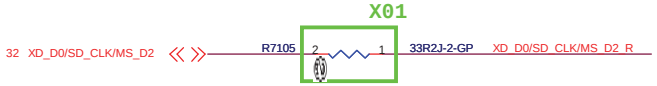




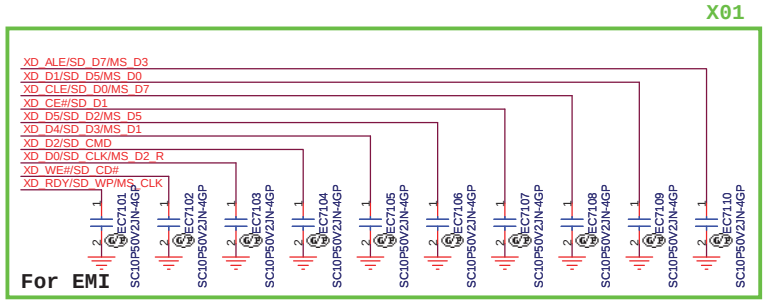
X01

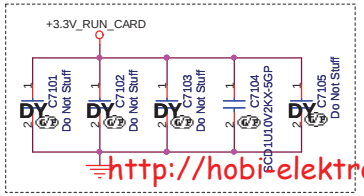


X01



X01





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Title: CARD Reader Connector

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Title: RESERVED

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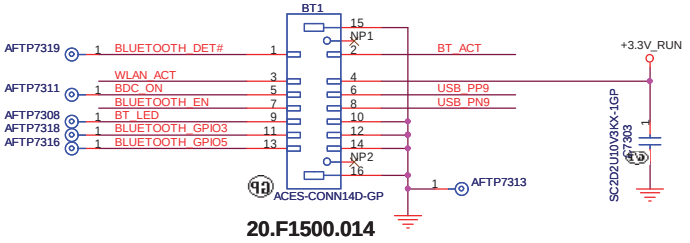
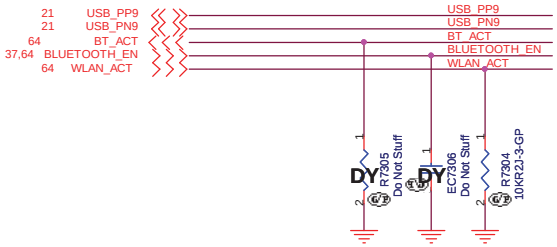
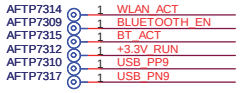
SSID = User.Interface

Bluetooth Module conn.



20.F1500.014





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Title: Bluetooth

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Title: *Reserved*

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Reserved

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Title

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for 65 BOM

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Title: *Reserved*

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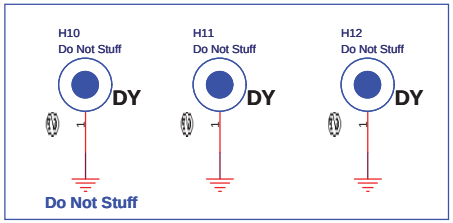
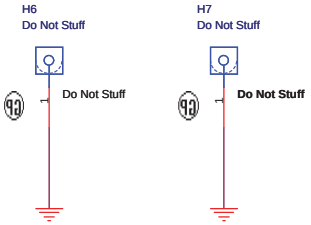
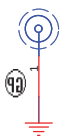
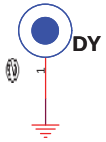
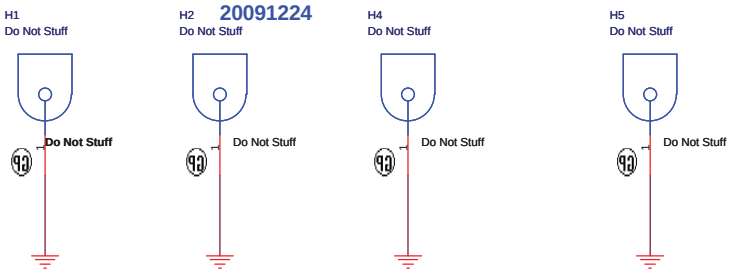
SSID = Mechanical

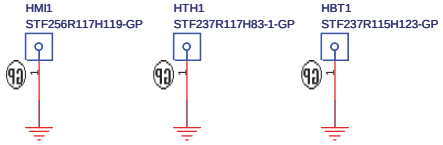


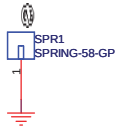


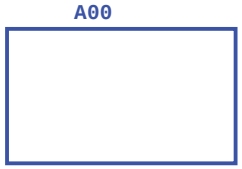


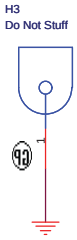


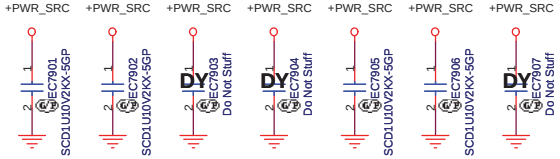


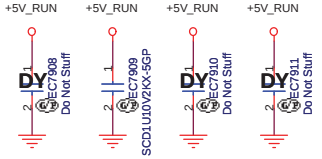


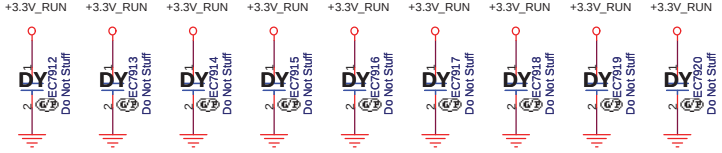


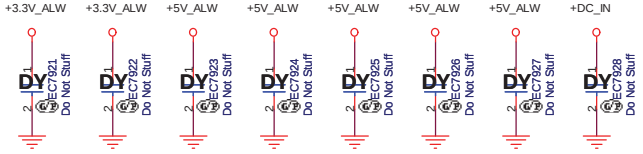












for 65 BOM

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Title: UNUSED PARTS/EMI Capacitors

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SSID = VIDEO

for 65 BOM

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Title: Reserved

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Title: *Reserved*

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Title

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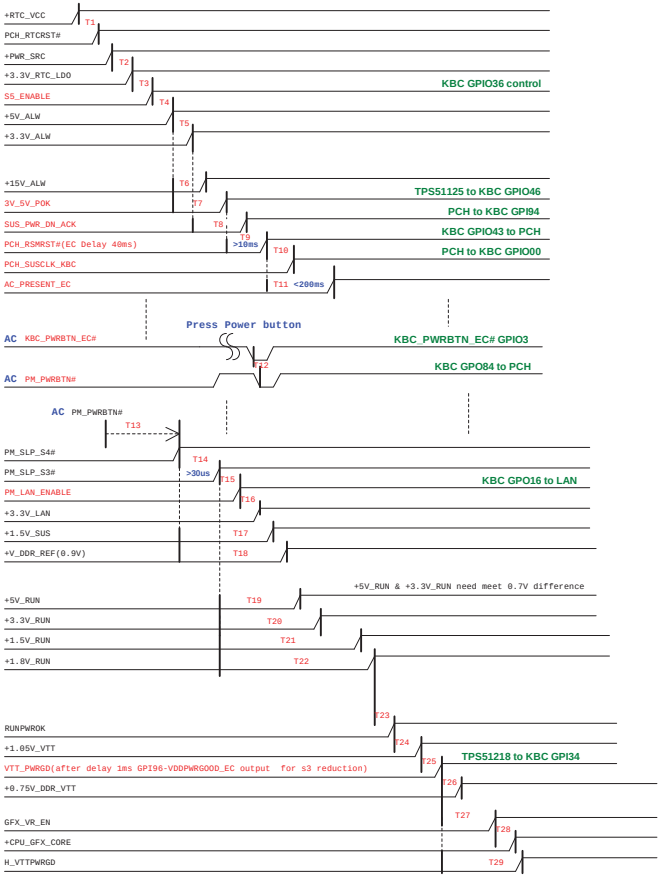
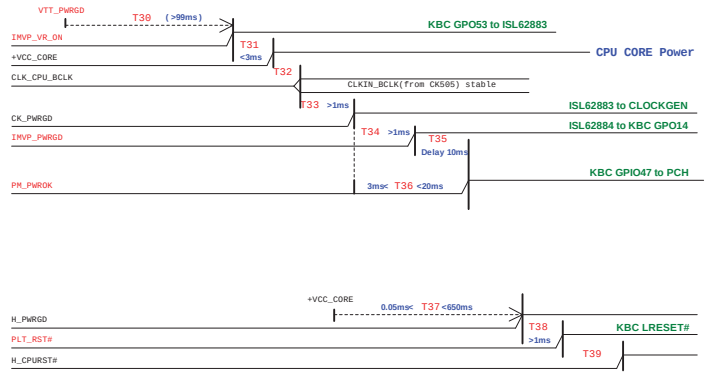
DJ2 Calpella UMA-Power Up Sequence

(AC mode)

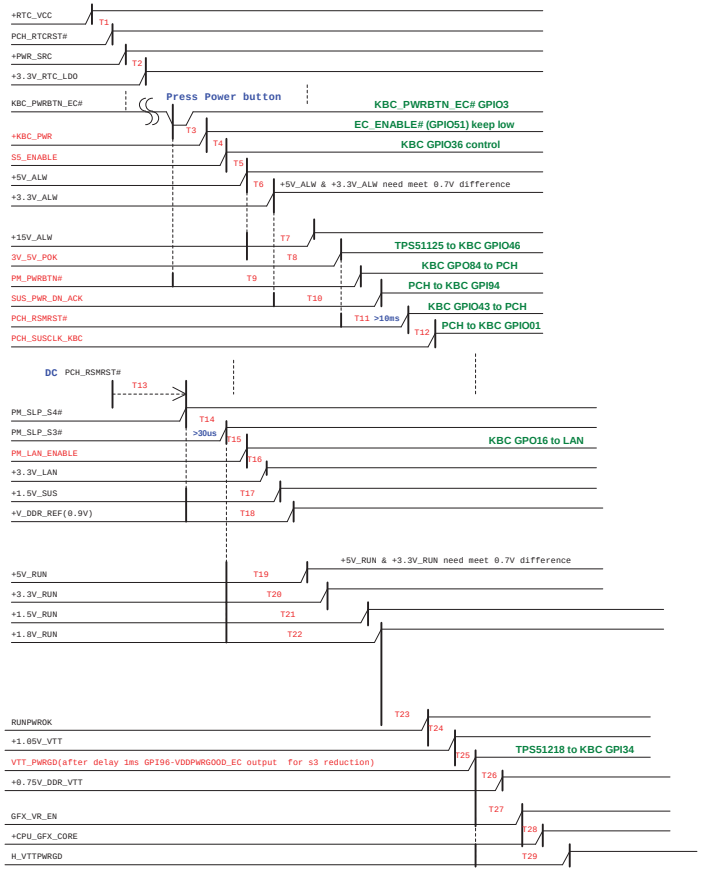
red word: KBC GPIO

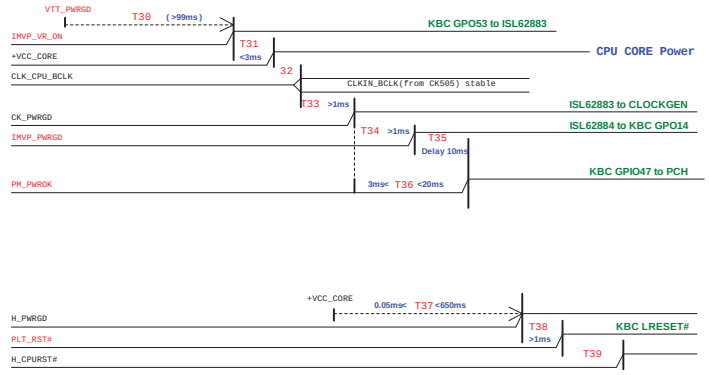




(DC mode)

red word: KBC GPIO





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Title: Power Sequence

Size	Document Number	Rev
A1	DJ2 CP UMA	A.00

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	71	4/8	EE	Card reader no work	Added Q7101, Q7102, R7101 and R7103 for card reader card detect and write protect signals	X01
2	61	4/8	EE	LAN surge circuit for China market	Reserved LAN surge circuit	X01
3	55	4/8	EE	Improve the SI reslut for JVGA_HS and JVGA_VS	Changed the value of RN5504 from 0 Ohm to 33Ohm	X01
4	24	4/9	EE	Crystal report suggest cap value for X2401	Changed C2403 and C2402 from 15pF to 18pF as vendor suggested	X01
5	35	4/9	EE	Crystal report suggest cap value for X3501	Changed C3511 and C3512 from 27pF to 18pF as vendor suggested	X01
6	23	4/9	EE	Crystal report suggest cap value for X2301	Changed C2307 from 12pF to 15pF as vendor suggested.	X01
7	30	4/9	EE	For improve audio codec performance and audio de-pop noise	Pop C3012, C3013, C3024, R3041, R3042, Q3002, R3043, C3035, Q3003, Q3004 and C3005 as codec vendor suggested	X01
8	61	4/12	EE	LAN surge circuit for China market	Added R6101~R6104 for LAN surge circuit and NC the pin11 of U6103 and U6104	X01
9	43	4/12	EMC	For EMC power noise issue in DCIN circuit	Added PL4301	X01
10	30	4/12	EE	For audio codec de-pop circuit	Added D3005 as audio vendor suggest	X01
11	30	4/13	EE	For audio codec de-pop noise circuit	Changed R3043 from 10K Ohm to 1K Ohm and added R3044 and R3045 as vendor suggested	X01
12	54	4/13	EMC	Improve USB port EMI	Pop TR5401 and de-pop R5411 and R5409	X01
13	35	4/13	EE	For SI measurement in PT stage	Added RN3509 for CLK_PCIE_LAN/#	X01
14	37	4/13	EE	For SI measurement in PT stage	Added RN3715 and R3756	X01
15	63	4/14	EMC	For EMC USB port ESD testing	Pop D6303	X01
16	57	4/14	EE	For HDMI SI report	Changed the R5705 from 453Ohm 1% to 442Ohm 1% as vendor request	X01

for 65 BOM

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
17	61	4/13	EE	LAN surge circuit for China market	De-pop R6101~R6104	X01
18	30	4/13	EE	For audio function de-pop noise circuit	Added R3044 and R3045	X01
19	71	4/13	EE	Cost down	Merged R7101 and R7103 to RN7101	X01
20	30	4/14	EE	For audio de-pop noise circuit	Changed R3042 from 220K Ohm to 100K Ohm and changed R3041 from 10K Ohm to 1K Ohm, de-pop R3018, C3027, C3029, C3032 and C3033, pop C3020, C3021, C3002 and C3016	X01 X01
21	46	4/14	Power	For 3V/5V power solution change	Changed PU4603 to TPS51125A and change PR4605, PR4604 to 0 Ohm, pop PR4617, PR4618, de-pop PR4616, PR4619, PR4622.	X01
22	47, 48	4/14	Power	For CPU core power setting fine tune	Changed PR4507 to 2.8K, PR4727 to 1.37K. Change PL4814 and PL4817 to bigger size. Change PQ4833 and PQ4840 to SI7686DP	X01
23	49	4/14	Power	For +1.05V_VTT power setting fine tune	Changed PR4902 to 59K. Changed PL4902 to bigger size and PU4902 to SI7686DP	X01
24	50	4/14	Power	For +1.5V SUS power setting fine tune	Changed PU5003 to SI7686DP and changed PL5001 to bigger size. De-pop PR5011	X01
25	53	4/14	Power	For +GFX_CORE power setting fine tune	Changed PU5302 to SI7686DP and changed PU5303, PU5304 to SIR4600DP. Changed PL5301 to bigger size	X01
26	49, 50	5/4	EE	According to Ibx RTC debug check list	Changed PR5004 from 100K Ohm to 20K Ohm, PC4907 from 1000pF 50V to 0.022uF 16V and added R4905 (1K Ohm)	A00
27	37	5/4	EE	For board id changed to A00	Pop R3723 and de-pop R3726	A00
28	30	5/4	EE	For audio de-pop noise circuit	Connect the AMP_MUTE# and AUD_EAPD to D3004 pin1, pin2, connect the PCH_AZ_CODEC_RST# to D3005 pin1. De-pop D3005 for PCH_AZ_CODEC_RST# don't need to for the de-pop noise circuit.	A00
29	7, 30, 35, 43, 60	5/6	EE	For cost dwon	Change the R708, R709, R3023, R3024, R3025, R3026, R3029, R3027, R3031, R3503, PR4309, R6001, R6002, R6005 and R6006 to short pad	A00
30	32, 54	5/6	EE	For remove co-lay parts	Delete TR3201, R3211, R3210, R5409 and R5411for had confirm with EMI team could be removed.	A00
31	70	5/6	EE	For cost down	DY GF1 (debug connector) for no need after x-build	A00
32						

for 65 BOM

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33	21	5/7	EE	For prevent wrong RTC sequence	Add de-pop R2119 (10K Ohm) and pull up with +3.3_RUN power on PCI_GNT3# net	A00
34	46, 47, 50, 53	5/7	EE	Cost down	Change PR4617, PR4618, PR4620, PR4706,PR4708,PR4713, PR4718,PR4722, PR4732,PR4738,PR4744,PR4755,PR4764, PR4776, PR4784, PR4707,PR4711, PR5002, PR5102, PR5313, PR5314 and PR5317 to short pad	A00
35	37	5/7	EE	For LPC bus EA	Change RN3715 and R3756 from 0 Ohm to 33 Ohm.	A00
36	26, 64, 66, 26	5/10	EE	Cost down	Change the R2603, R2607, L3701, R6414, R6603 and R2611 to short pad.	A00
37	79	5/10	EMI	Cost down	Delete SPR3 and SPR4 for no need.	A00
38	49	5/10	EE	For 65 BOM setting	Change PU4902 from 84.07686.037 to 84.07692.037 and PU4903 from 84.00164.037 to 84.00308.030	A00
39	47, 22, 62	5/11	EE	Cost down	Changed PR4790, R2219, R6204 and R6205 from 0 Ohm resistor to short pad	A00
40	35	5/11	EE	For PCIE_LAN EA	Change RN3509 from 0 Ohm resistor array to 33 Ohm resistor array	A00
41	46	5/13	Power	For 5V OCP setting as power team request	Change the PR4602 to 147K Ohm	A00
42	55	5/13	EE and EMI	For EMI and EA report	Change the L5501~L5503 to 68.00084.D61	A00
43	47	5/14	Power	For IMON setting as power team request	Change PR4717 to 11Kohm(64.11025.6DL)	A00
44	35	5/14	EE	Audio de-pop noise circuit	De-pop D3005 for PCH_AZ_CODEC_RST# no need in de-pop noise circuit	A00
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for 65 BOM

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Taipei Hsien 221, Taiwan, R.O.C.

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Title: *Change History*

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