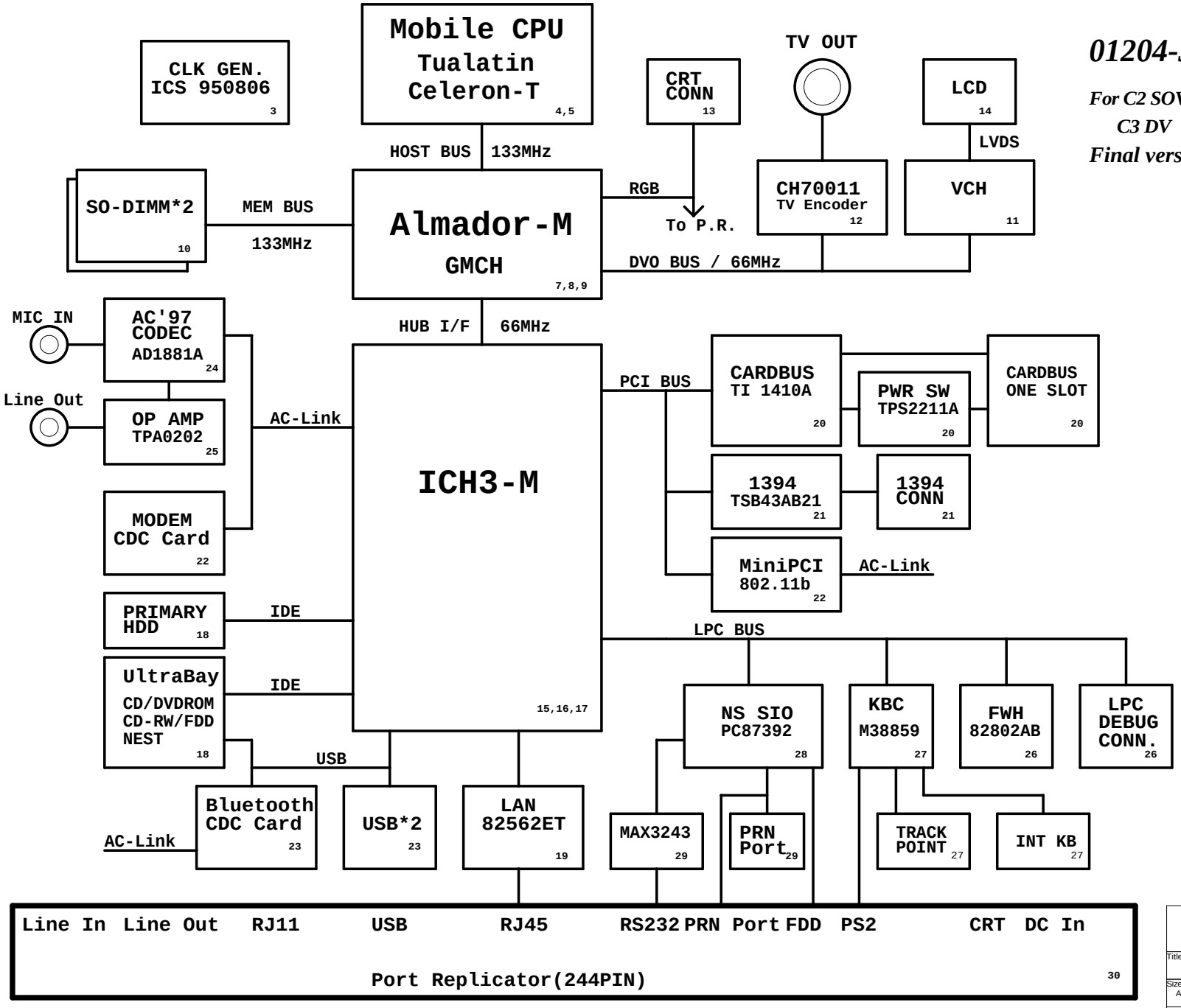
Jan. 11 2002

C-Note 2 Block Diagram

01204-3

For C2 SOVP
C3 DV
Final version



PCB LAYER
L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: GND
L6: POWER
L7: Signal 4(weak)
L8: Signal 5
L9: GND
L10:Signal 6

DC/DC&CHARGER
Switching Power
MAX1631/MAX1772

INPUTS	OUTPUTS
DCBATOUT	LAN+3VAUX UBAY+5V +3VSUS +5VSUS +3VRUN +5VRUN
AD+	BT+
	33,36

CPU DC/DC
Switching Power
MAX1718/MAX1714

INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE +VCCT
	31,32

OTHER DC/DC
MAX1644/MAX1792

INPUTS	OUTPUTS
+3.3VRUN	+1.8VRUN
+3.3VRUN	+1.5VRUN
	32

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Taiwan, R.O.C.

Title: *Block Diagram*

Size: A3 | Document Number: *C-Note 2* | Rev: *-3*

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08.GMCH (2/3)
09.GMCH (3/3)
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12.TV Encoder
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14.LCD/Inverter CONN
15.ICH3-M (1/3)
16.ICH3-M (2/3)
17.ICH3-M (3/3)
18.HDD & ULTRA BAY
19.LAN
20.PCMCIA Controler OZ6912
21.1394 TSB43AA22
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29.Printer Port
30.PORT-REPLICATOR
31.CPU CORE
32.CPUIO/1.5V/1.8V/1.2V
33.3V/5V DC/DC
34.PWR PLANE & RESET LOGIC
35.CHARGER uP-MC68HC908SR
36.CHARGER CONTROLER-MAX1772
37.SPARE Logic/TEST POINT

CG_* : CPU GTL+
CC_* : CPU CMOS
M_*   : MEMORY BUS
G_*   : AGP BUS
P_*   : PCI BUS
HL_* : HUB LINK I/F
LPC_* : LPC I/F
ICH_AC_* : AC'97 LINK I/F
IDE_* : IDE BUS

Cu-T & Tualatin SPEC Summary

July 3 '01

	Early Samples/ES	QS/ Production
Tualatin	VCC = 1.50V (perf mode)/ 1.15V (batt mode) VCCT = 1.3V (min), 1.365V (max) R143 16K5R3F, R142 49K9R3F Tj (min) = 10C	VCC = 1.40V (perf mode)/ 1.15V (batt mode) ICC,MAX = 13.71A VCCDPRSLP=0.85V ICC,DSLP=2.09A VCCT = 1.25V +/- 5% (static) +/- 9%(transient) R143 2D49KR3, R142 10KR3F ICC =2.7A Tj (min) = 0C
Cu-T	VCC = 1.7V (perf Mode)/ 1.35V (Batt Mode) VCCT = 1.2V +/- 5% Functional at : VCCT = 1.3V (min), 1.365 (max)	VCC = 1.7V (perf Mode)/ 1.35V (Batt Mode) VCCT = 1.25V +/- 5% (static) +/- 9%(transient)
GMCH	VCC/VTT = 1.2V +/- 5% Functional at : VCC/VTT= 1.3V (min), 1.365V (max)	VCC/ VTT = 1.25V +/- 5%

MAX1718 Voltage Setting

D4	D3	D2	D1	D0	Vout (V)	
0	0	0	0	0	1.75	
0	0	0	0	1	1.70	Perf for Cu-T
0	0	0	1	0	1.65	
0	0	0	1	1	1.60	
0	0	1	0	0	1.55	
0	0	1	0	1	1.50	
0	0	1	1	0	1.45	Perf for Tualatin
0	0	1	1	1	1.40	Batt for Cu-T
0	1	0	0	0	1.35	
0	1	0	0	1	1.30	
0	1	0	1	0	1.25	
0	1	0	1	1	1.20	
0	1	1	0	0	1.15	Batt for Tualatin
0	1	1	0	1	1.10	
0	1	1	1	0	1.05	
0	1	1	1	1	1.00	

S1	S0	Vout (V)
GND	GND	0.975
GND	REF	0.950
GND	Float	0.925
GND	VCC	0.900
REF	GND	0.875
REF	REF	0.850
REF	Float	0.825
REF	VCC	0.800
Float	GND	0.775
Float	REF	0.750
Float	Float	0.725
Float	VCC	0.700
VCC	GND	0.675
VCC	REF	0.650
VCC	Float	0.625
VCC	VCC	0.600

ZMODE	SUS	Vout Determined by:
GND	GND	Logic Level of D0 - D4
VCC	GND	Impedance of D0 - D4
X	VCC	Logic Level of S0, S1

+VCCT — +VCCT 3,4,5,6,9,32
+VCC_CORE — +VCC_CORE 4,5,31
+1.5VRUN — +1.5VRUN 4,5,6,7,8,9,11,12,17,26,32
+1.8VRUN — +1.8VRUN 4,8,9,11,15,17,32
LAN+3VAUX — LAN+3VAUX 15,17,19,22,30,34
+3VRUN — +3VRUN 3,6,8,9,11,12,13,14,15,16,17,18,20,21,22,23,24,26,27,28,31,32,34,35,37
+3VSUS — +3VSUS 6,9,10,14,18,20,23,27,31,32,34,35,37
+3VALW — +3VALW 14,15,16,17,23,25,32,33,34,36
+3.3VRTC — +3.3VRTC 16
+5VRUN — +5VRUN 6,13,14,15,17,18,22,24,25,26,27,29,30,31,34,35,37
+1.8VALW — +1.8VALW 17,34
+5VSUS — +5VSUS 13,14,20,23,25,27,32,34,37
+5VALW — +5VALW 14,17,18,30,33,34,36
LAN+1.8VAUX — LAN+1.8VAUX 17,34
UBAY+5V — UBAY+5V 18
+5VA — +5VA 24,25
BT+ — BT+ 35,36
+3VAUX — +3VAUX 22,23
USB1_VCC — USB1_VCC 23,30
LCDVDD — LCDVDD 14
AC97_3V — AC97_3V 23
CRT_VCC — CRT_VCC 13,30
AD+ — AD+ 35,36
AD+IN — AD+IN 35,36
DCBATOUT — DCBATOUT 14,31,32,33,34,35,36
DCBATOUT+ — DCBATOUT+ 36
ICH_VBIAS — ICH_VBIAS 16
VCC_RTC — VCC_RTC 6,15,16,17
AD+_IN — AD+_IN 30,36
MAX1631_VL — MAX1631_VL 14,33
BT_VCC — BT_VCC 23
FAN1_VCC — FAN1_VCC 6
TV_DVDD — TV_DVDD 12

TV_AVDD — TV_AVDD 12
TV_VDD — TV_VDD 12
+1.5VRUN_F — +1.5VRUN_F 12
LCD_DCBAT — LCD_DCBAT 14
LIGHT_PWR — LIGHT_PWR 14

SLOTVCC — SLOTVCC 20
SLOTVPP — SLOTVPP 20
1394_AVDD — 1394_AVDD 21
1394_PLLVDD — 1394_PLLVDD 21
MOD_5VAD — MOD_5VAD 22
USB0_VCC — USB0_VCC 23
AUD_VREF — AUD_VREF 25
OP+5V — OP+5V 25
TP_VCC — TP_VCC 27
1718_+5V — 1718_+5V 31
M1772+3V — M1772+3V 36
M1772_LDO — M1772_LDO 36
DC+5V — DC+5V 33
DC+3V — DC+3V 33

PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#
TI 1394	AD19	Auto	REQ2# / GNT2#
MINIPCI SLOT	AD21	C,E	REQ3# / GNT3#
PCMCIA TI1410	AD25	B,D	REQ1# / GNT1#
AGP	AD17(Int.)	A,B	
LAN	AD24(Int.)	E	
USB	AD29	A,D,C	
Hub-to-PCI	AD30		
LPC Bridge/ IDE/AC97/ SMBus	AD15		

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Title: TABLE OF CONTENT
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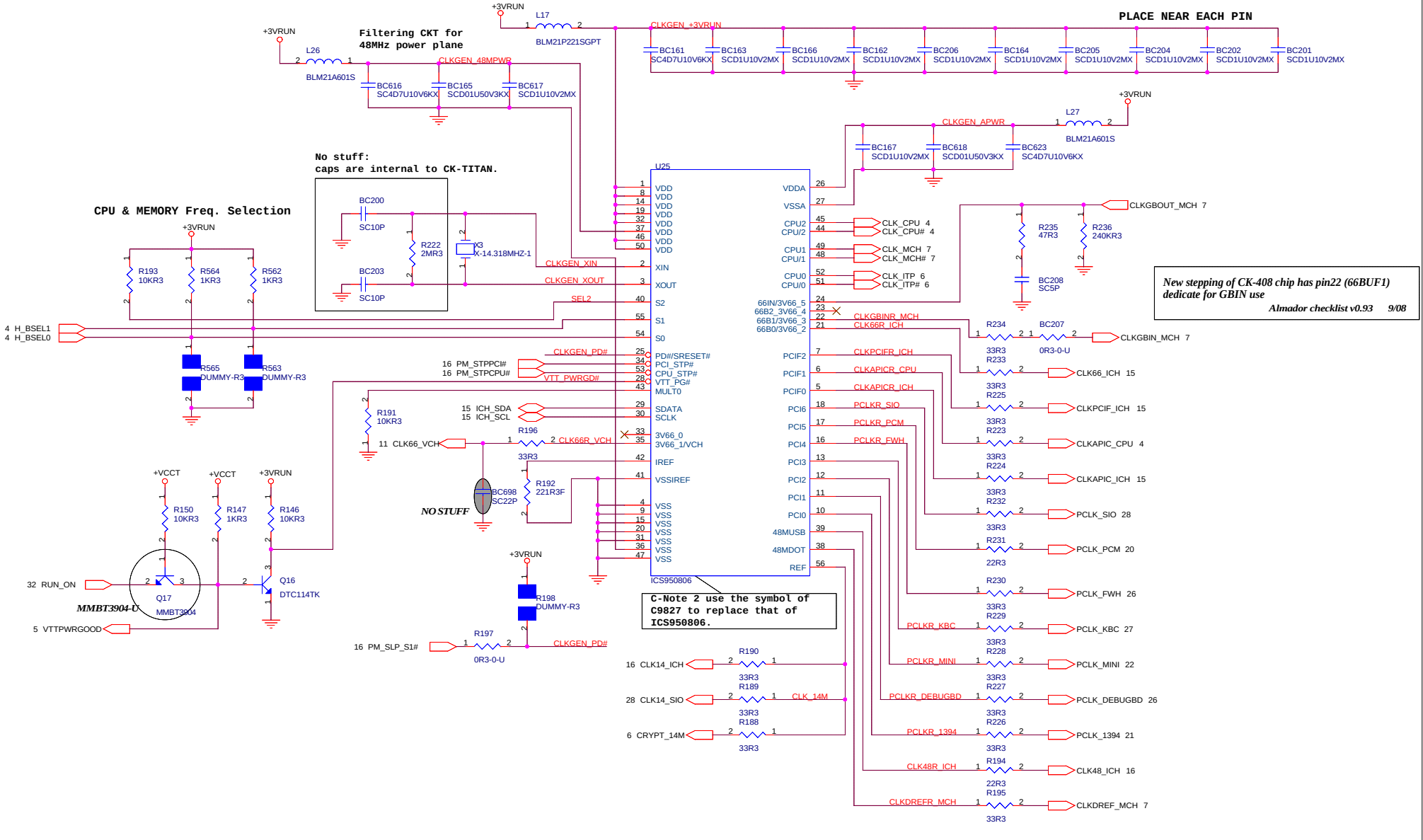
PLACE NEAR EACH PIN
Filtering CKT for 48MHz power plane
No stuff:
caps are internal to CK-TITAN.
CPU & MEMORY Freq. Selection
U25
ICS950806
C-Note 2 use the symbol of C9827 to replace that of ICS950806.
NO STUFF
MMBT3904-U
New stepping of CK-408 chip has pin22 (66BUF1) dedicate for GBIN use
Almador checklist v0.93 9/08
CLK GEN. SECOND SOURCE
ICS : ICS950806 71.95806.00W
CYPRESS : W320-04X 71.00320.00W
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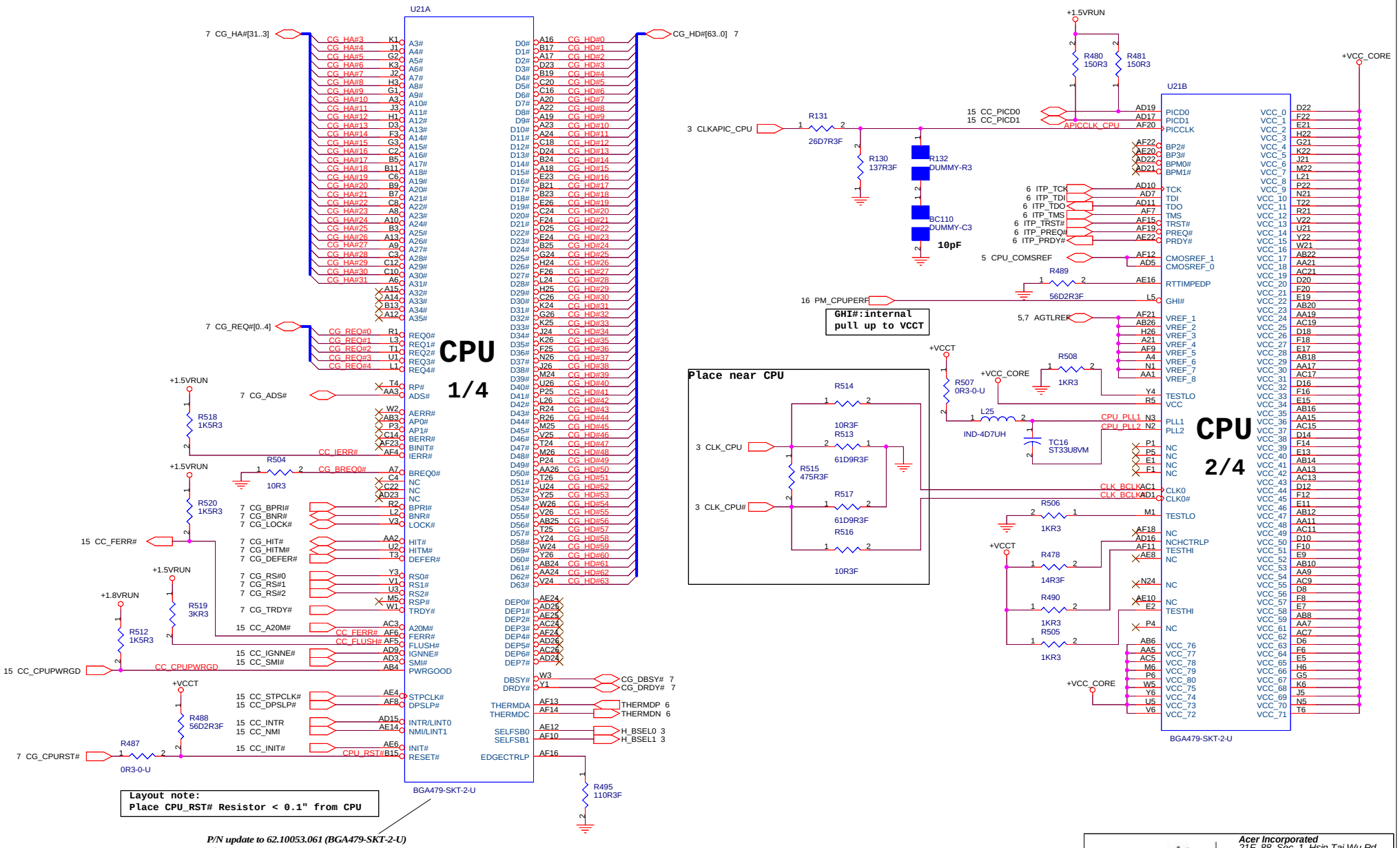
CLOCK GENERATOR
C-Note 2
Friday, January 11, 2002


U21A
CPU 1/4
7 CG_HA#[31..3]
7 CG_REQ#[0..4]
7 CG_ADS#
CG_HD#[63..0] 7
+1.5VRUN
+1.8VRUN
+VCCT
R518 1K5R3
R520 1K5R3
R519 3K3R3
R512 1K5R3
R504 10R3
R488 56D2R3F
R487 0R3-0-U
CC_IERR#
CC_BREQ0#
CC_FERR#
CC_CPUPWRGD
CC_FLUSH#
CC_RST#
15 CC_FERR#
15 CC_CPUPWRGD
7 CG_CPURST#
15 CC_A20M#
15 CC_IGNNE#
15 CC_SMI#
15 CC_STPCLK#
15 CC_DPSLP#
15 CC_INTR
15 CC_NMI
15 CC_INIT#
7 CG_BPRI#
7 CG_BNR#
7 CG_LOCK#
7 CG_HIT#
7 CG_HITM#
7 CG_DEFER#
7 CG_RS#0
7 CG_RS#1
7 CG_RS#2
7 CG_TRDY#
CG_DBSY# 7
CG_DRDY# 7
THERMDP 6
THERMDN 6
H_BSEL0 3
H_BSEL1 3
R495 110R3F
BGA479-SKT-2-U
Layout note:
Place CPU_RST# Resistor < 0.1" from CPU
P/N update to 62.10053.061 (BGA479-SKT-2-U)
7/12
CPU SOCKET SECOND SOURCE
AMP : 62.10053.061
FOXCONN: 62.10055.011
3 CLKAPIC_CPU
R131 26D7R3F
R130 137R3F
R132 DUMMY-R3
BC110 DUMMY-C3
10pF
15 CC_PICD0
15 CC_PICD1
APICCLK_CPU
R480 150R3
R481 150R3
6 ITP_TCK
6 ITP_TDI
6 ITP_TDO
6 ITP_TMS
6 ITP_TRST#
6 ITP_PREQ#
6 ITP_PRDY#
5 CPU_COMSREF
16 PM_CPUPERF
R489 56D2R3F
GHI#:internal pull up to VCCT
5,7 AGTLREF
Place near CPU
3 CLK_CPU
3 CLK_CPU#
R514 10R3F
R513 61D9R3F
R515 475R3F
R517 61D9R3F
R516 10R3F
R507 0R3-0-U
L25 IND-4D7UH
TC16 ST33U8VM
R508 1KR3
R506 1KR3
R478 14R3F
R490 1KR3
R505 1KR3
+VCC_CORE
CPU 2/4
CLK_BCLK
CLK_BCLK#
CPU_PLL1
CPU_PLL2
BGA479-SKT-2-U
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Title
CPU
Size A3
Document Number C-Note 2
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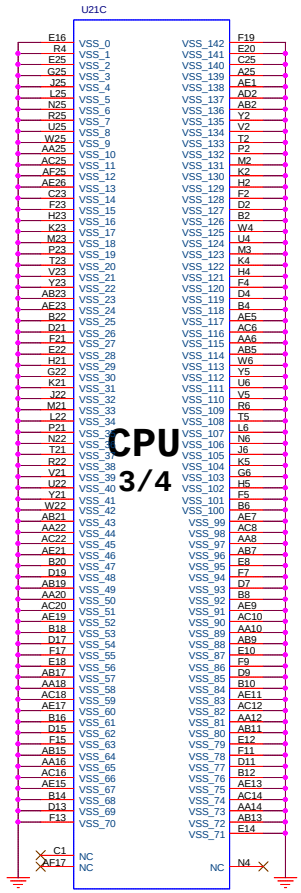

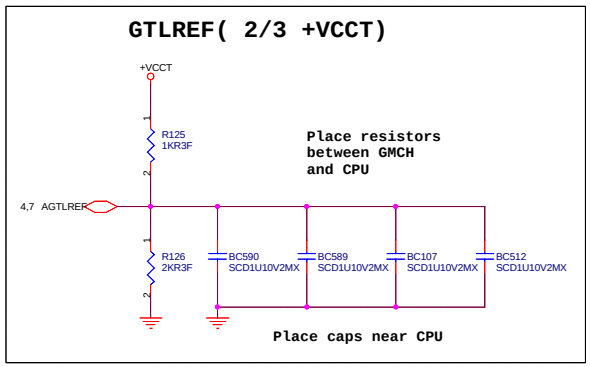

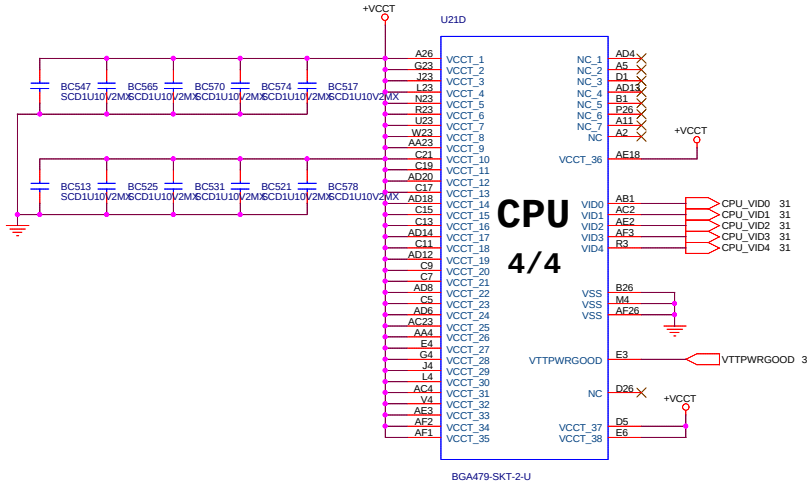

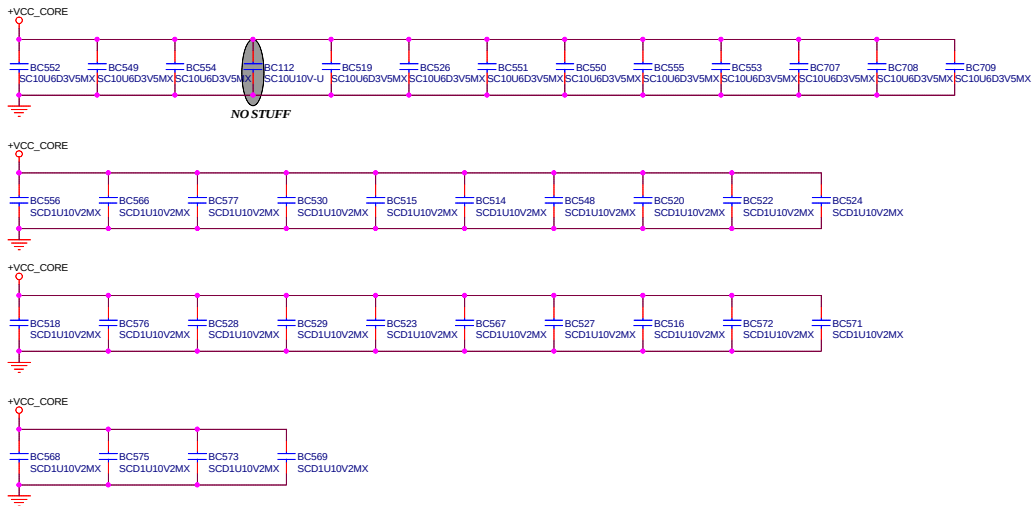

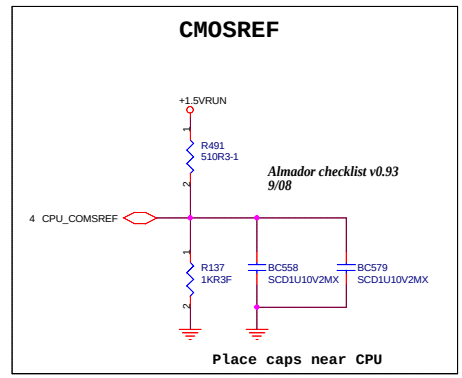

Decouping Recommendation

C-Note 2 Kenora Ver 0.93

VCC_CORE	Underneath balls on solder side	0.22uF * 24	Use 2-3 vias per pad for reduced inductance during layout	0.1uF * 24	0.47uF * 24
	On the peripheral near balls	10uF / 6.3V * 10	Placement should be near processor for all	10uF / 10V * 10	10uF / 6.3V * 10 + 6 * NS
	Bulk Caps			220uF / 2.5V * 7	150uF / 4V * 12 + 2 * NS
VCCT	Place close to processor for all	1uF * 10	Use 2 vias per pad for reduced inductance during layout	0.1uF * 10	1uF * 10 + 2 * NS
	Bulk Caps			220uF / 2.5V * 2	150uF / 4V * 5 + 1 * NS

Almador-M Checklist Ver. 0.93 9/08

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Title: CPU CONFIGURATION

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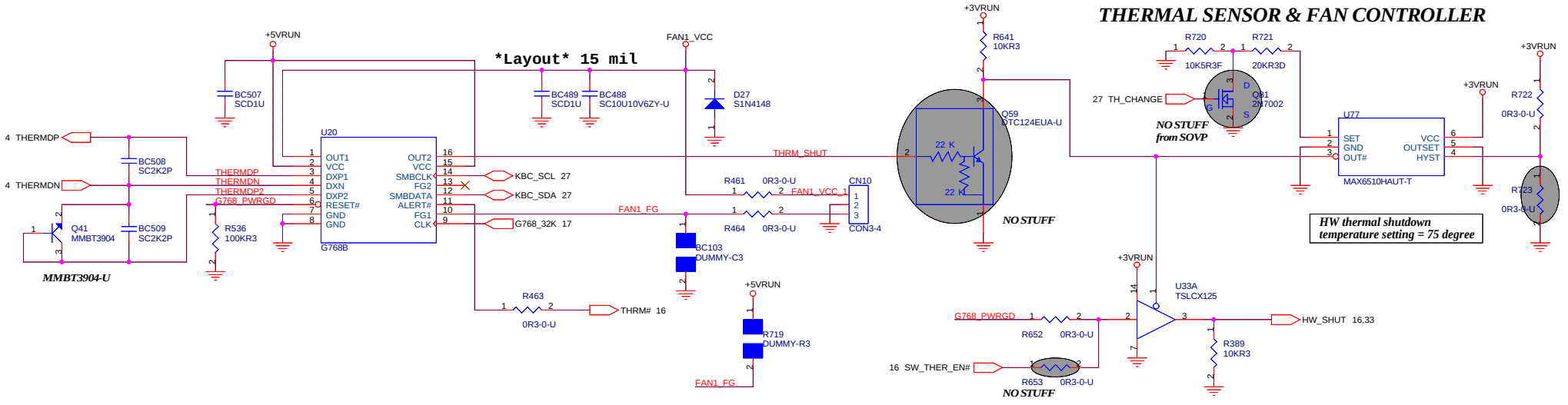
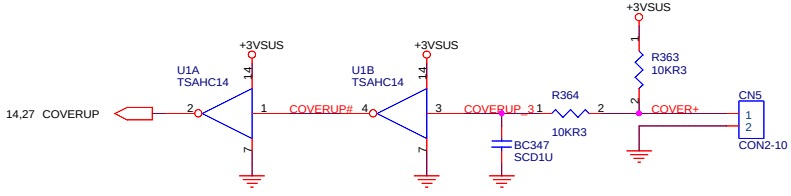
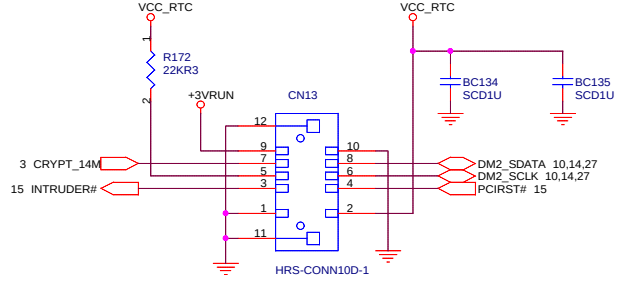
THERMAL SENSOR & FAN CONTROLLER

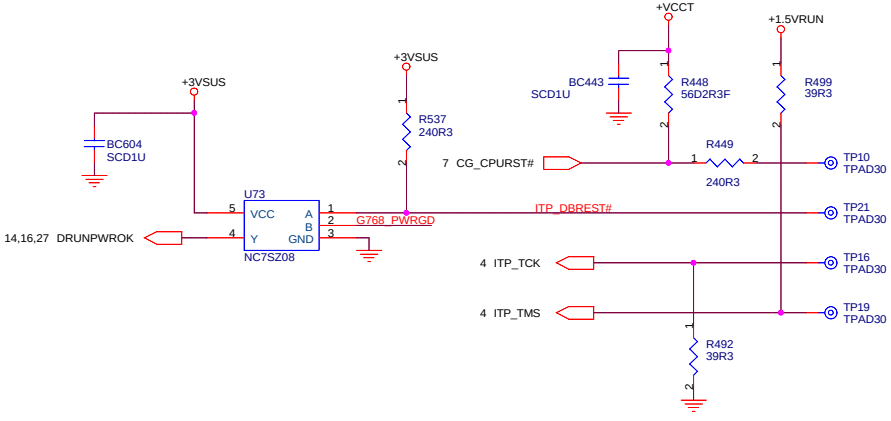


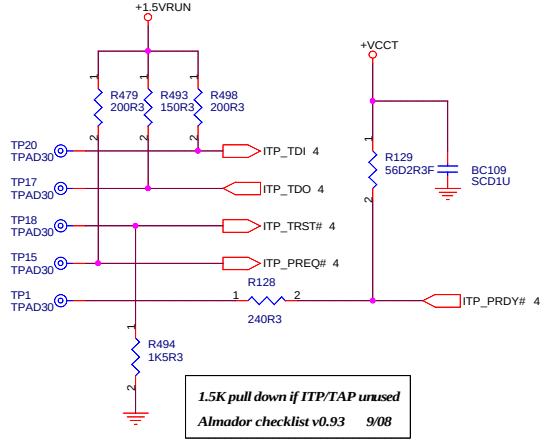
Cover Switch

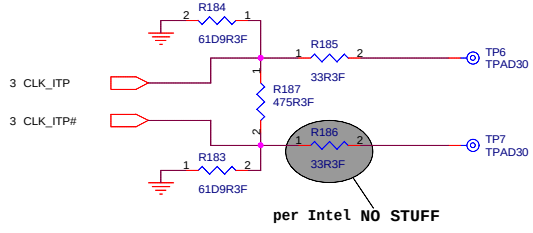


Crypto Card CONN









PULLUP RESISTOR<1"FROM ITP PORT PINS

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Taiwan ,R.O.C.

Title: ITP/Thermal/Fan Control/RFID

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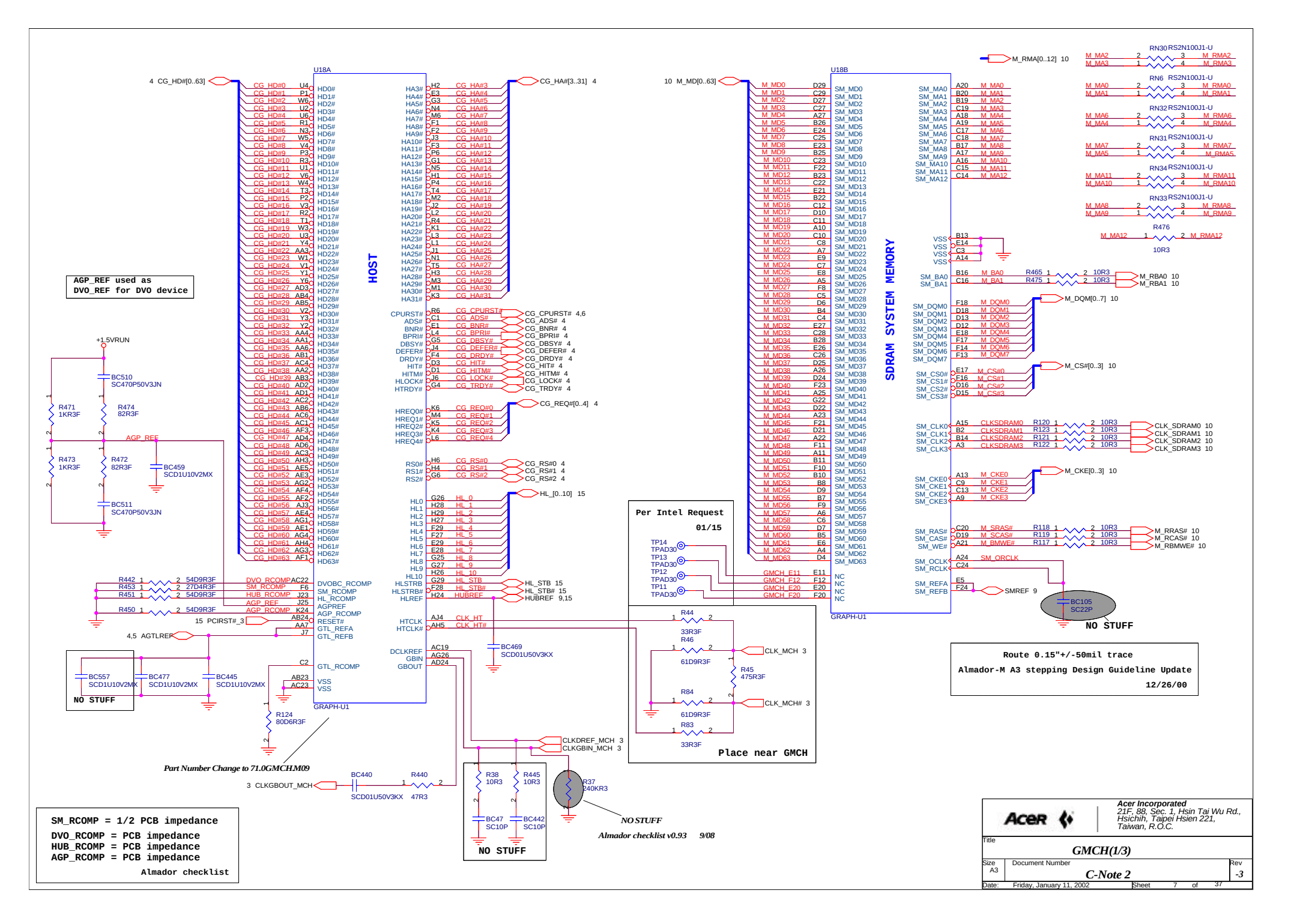
U18A
HOST
GRAPH-U1
U18B
SDRAM SYSTEM MEMORY
GRAPH-U1
AGP_REF used as
DVO_REF for DVO device
Per Intel Request
01/15
Place near GMCH
NO STUFF
NO STUFF
NO STUFF
Route 0.15"+/-50mil trace
Almador-M A3 stepping Design Guideline Update
12/26/00
SM_RCOMP = 1/2 PCB impedance
DVO_RCOMP = PCB impedance
HUB_RCOMP = PCB impedance
AGP_RCOMP = PCB impedance
Almador checklist
Part Number Change to 71.0GMCH.M09
NO STUFF
Almador checklist v0.93 9/08
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GMCH(1/3)
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AGP_PAR	Pull-up 8.2K to 1.5VRUN	AGP device attached
	Pull-down 2.2K to GND	DVO device attached

Strapping Option for SW detection of AGP or DVO device

DVOA_CLK# (AG24) --> DVO_CLKIN1 (N8)
DVOA_CLK (AJ24) --> DVO_CLKIN0 (M8)
Almador EDS Rev 0.9 Apr.7

DVOA_D5 Int. P/D	0 = DESKTOP 1 = MOBILE	Pull-up 2.2K to V1.5S
DVOA_D6 Int. P/D	0 = Dual ended term. 1 = Single ended term.	Pull-up 2.2K to V1.5S
DVOA_D0 Int. P/U	0 = 200MHz 1 = 133MHz	Pull-down 2.2K to GND
DVOA_D1 Int. P/U	0 : IOQD = 1 1 : IOQD = 8	Pull-down 2.2K to GND
DVOA_D7 Int. P/D	0 : Normal mode 1 : Invoking the XOR Chain test mode	
DVOA_D8 Int. P/D	0 : Normal mode 1 : Tri-stating all GMCH outputs when ICH3-M is in XOR Chain mode.	

Per Intel GMCH EDS Rev0.7 12/22/2K

Add pull-ups to +1.5VRUN on G_FRAME#, G_IRDY#, G_TRDY#, G_DEVSEL# in SVT planar

Almador checklist v0.93 9/08

Be close to pin RDDP 1.0

4.7K RDDP1.0 P.72

9/13 per Intel

DVO port of GMCH is +1.5V Power plane

DVO port of VCH is +1.8V Power plane

DVO_INTR#	Pull-up 100K to 1.5VRUN	Pull-up/down required if DVOA not implemented.
DVO_FIELD	Pull-down 100K to GND	
DVO_CLKIN	Pull-up 100K to 1.5VRUN	

DDC1CLK DDC1DAT	Pull-up 2.2K to +5VRUN	Non-5V tolerant, Q-Switch required for 5V support
DDC2CLK DDC2DAT	Pull-up 10K to +5VRUN	
I2CCLK I2CDATA	Pull-up 10K to +3VRUN	

KODIAK 0.7b P.9 33MHz OSC
9/13 change to 32K OSC per Intel

Pull-up required for ext. AGP GFX and int. DVO GFX

Connect pin AE20, G24(VSSA_DPLL[0,1]) to the respective decoupling caps of pin AC20, F25(VCCA_DPLL[0,1])

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Title: GMCH(2/3)

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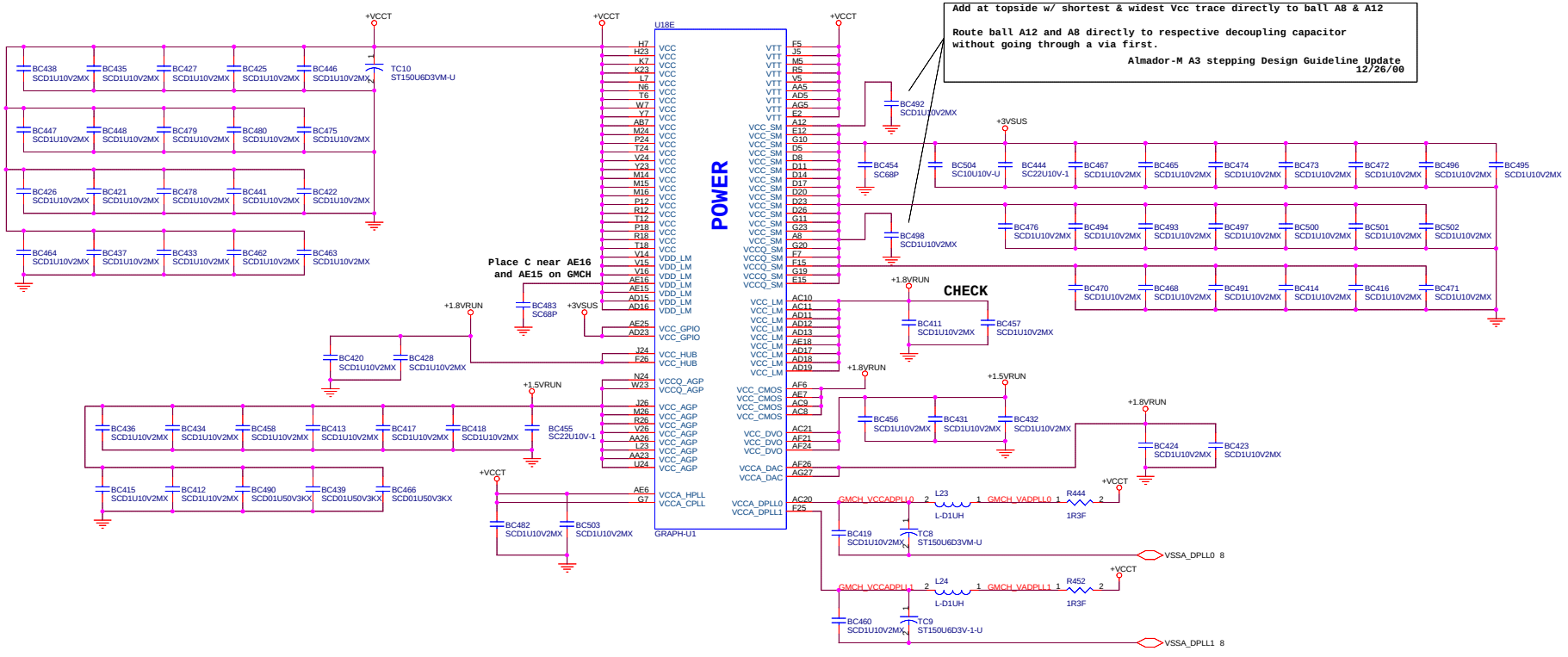
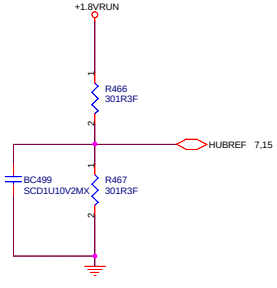


Decouping Recommendation

				C-Note 2	Kenora Ver 0.93
V1.2S_GMCH	Decoupling Caps	0.1uF * 10	Distribute as close as possible to GMCH-M processor Quadrant	0.1uF * 20 150uF / 6.3V * 2 68pF * 1 220uF / 2.5V * 2	0.1uF * 20
	Bulk Caps	10uF * 1			150uF / 4V * 5 + 1 * NS
V1.2S_GMCHCORE	Decoupling Caps	68pF * 1	Close to VDD_LM, near pins AE15 and AE16 on Almador		68pF * 1
		0.1uF * 10			0.1uF * 28
	Bulk Caps	10uF * 1			150uF / 4V * 6
V1.5S_GMCH	Decoupling Caps	0.1uF * 9 82pF * 4	Distribute as close as possible to GMCH-M AGP/DVO Quadrant	0.1uF * 11 0.01uF * 3 10uF /10V * 1	0.1uF * 9 82pF * 4
	Bulk Caps			22uF /10V * 1	22uF / 20V * 1
V1.8S_GMCH	Decoupling Caps	0.1uF * 4 + 2 82pF * 2	Distribute as close as possible to GMCH-M Local Memory Quadrant Additional 4* 0.1uF shall be distributed as close as possible to VCCPCMOS_LM	0.1uF * 6	0.1uF * 4 + 2 0.01uF *2 82pF * 2 22uF / 20V * 2
	Bulk Caps				68uF / 10V * 5
V3_GMCH	Decoupling Caps	0.1uF * 12 + 2 82pF * 4	Distribute as close as possible to GMCH-M System Memory Quadrant Additional 4* 0.1uF shall be distributed as close as possible to IO Quadrant	0.1uF * 20+2 22uF 10V * 1 10uF 10V * 1 82pF * 1	0.1uF * 12 + 2 82pF * 4 22uF / 20V * 2
	Bulk Caps				

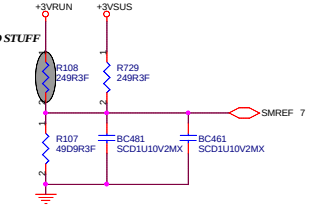
Almador-M Checklist Ver. 0.93 9/08

HUB INTERFACE REF 1/2*1.8V



Layout Note:
Place divider pair in middle of bus.
Place capacitors near GMCH.

SYSTEM MEMORY REF 0.55V



Place capacitor near GMCH ball E5 & F24.

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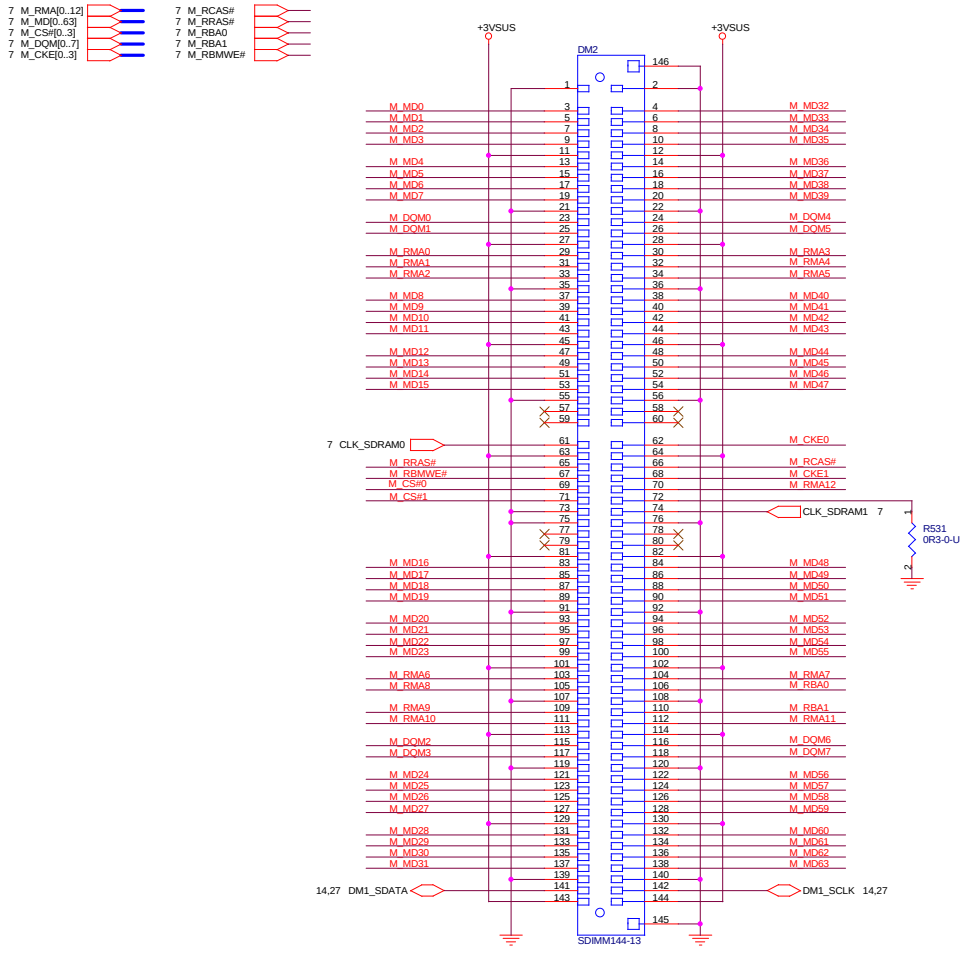
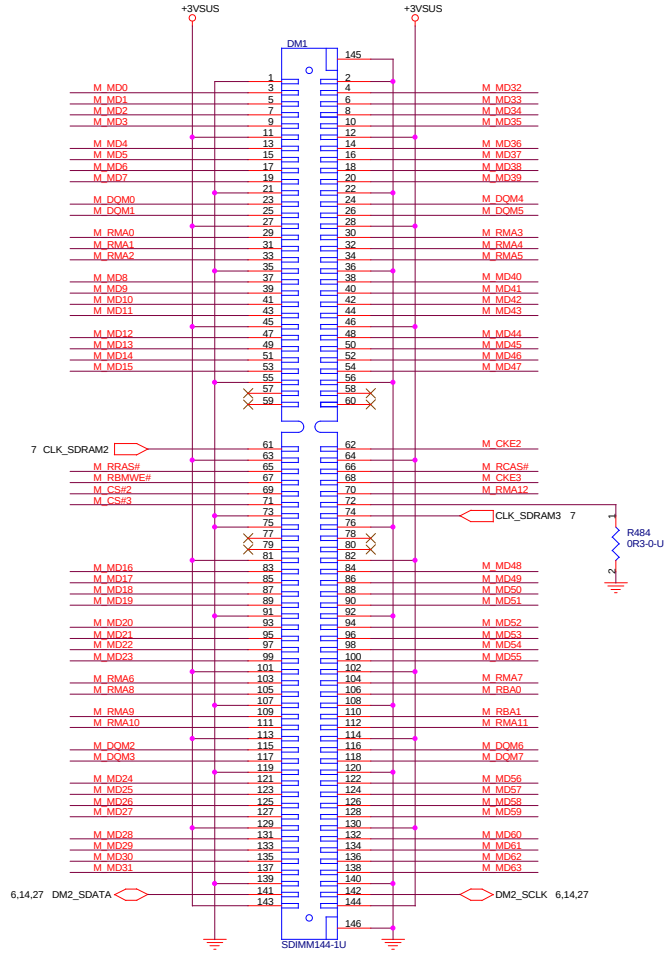
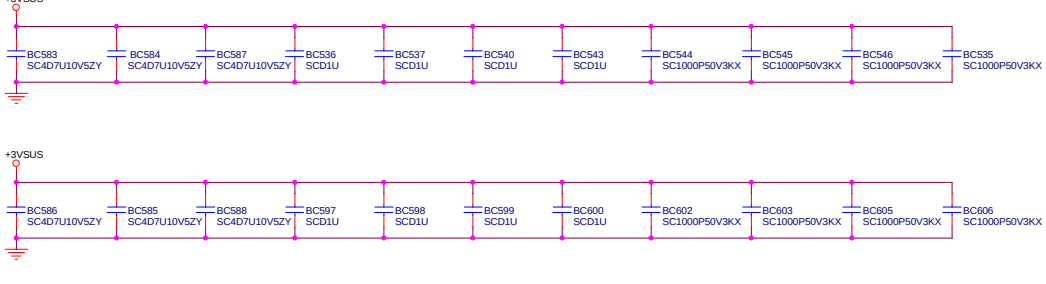
Title: GMCH(3/3)
Size: Custom | Document Number: C-Note 2 | Rev: -3
Date: Friday, January 11, 2002 | Sheet 9 of 37

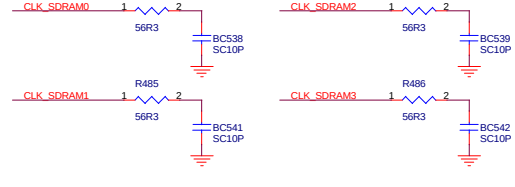
(Normal Type)



(Reverse Type)







SDRAM clock AC terminations change from 33 Ohm 22p to 56 Ohm 10p.

12/14/00

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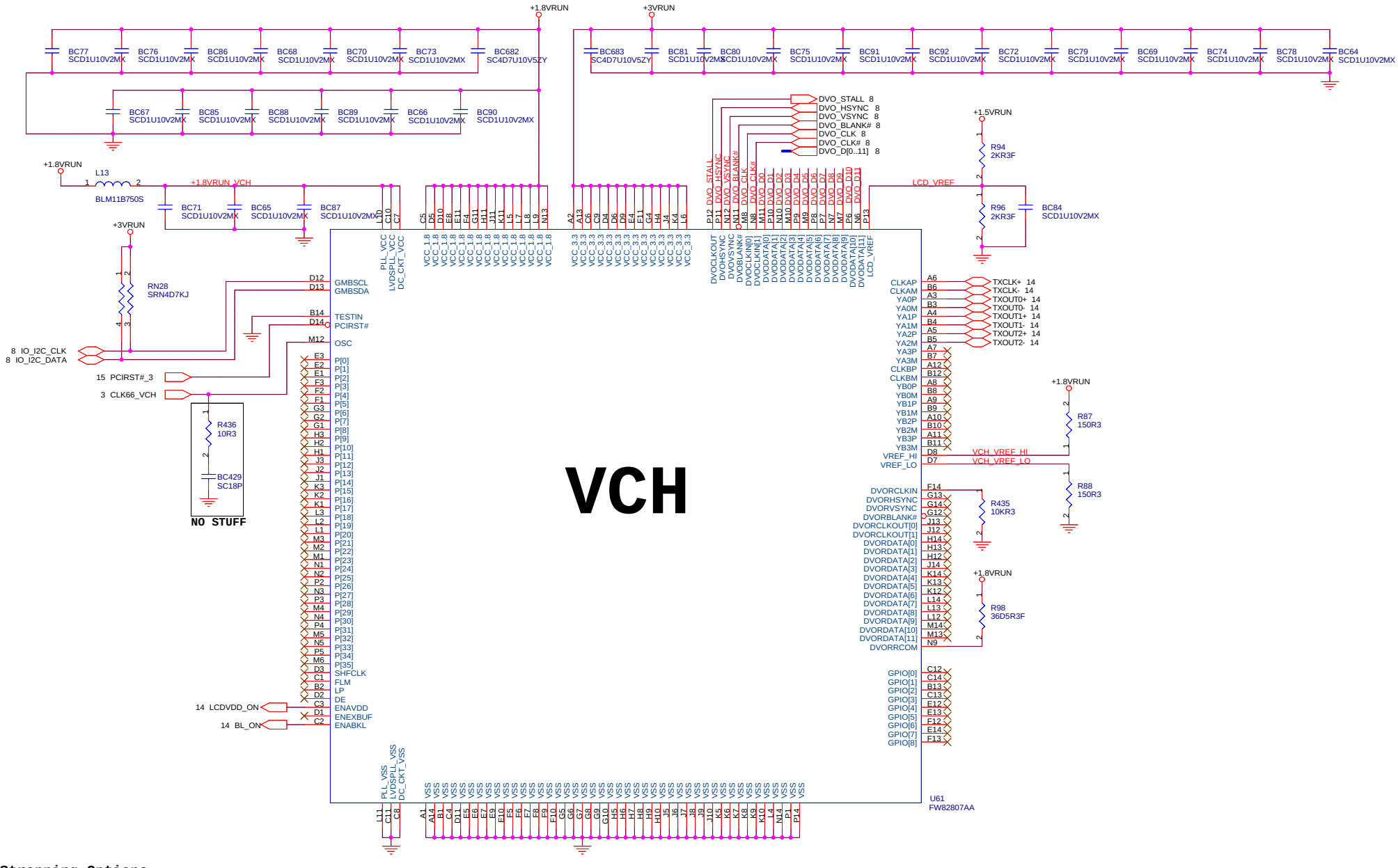
Title: **SO-DIMM**

Size: Custom | Document Number: **C-Note 2** | Rev: -3

Date: Friday, January 11, 2002 | Sheet 10 of 37



Strapping Options

GPIO[5:2]	10 - 4.7K Ohm	Can be used for panel ID select. Default state is GPI w/ int. weak pull down.
GPIO6	10 - 4.7K Ohm	For normal VCH operation pin has to be read as low. Default state is GPI w/ int. weak pull down.
GPIO[8:7]	10 - 4.7K Ohm	Used for GMBus base address select. Default state is GPI w/ int. weak pull down.

Almador checklist ver.0.93

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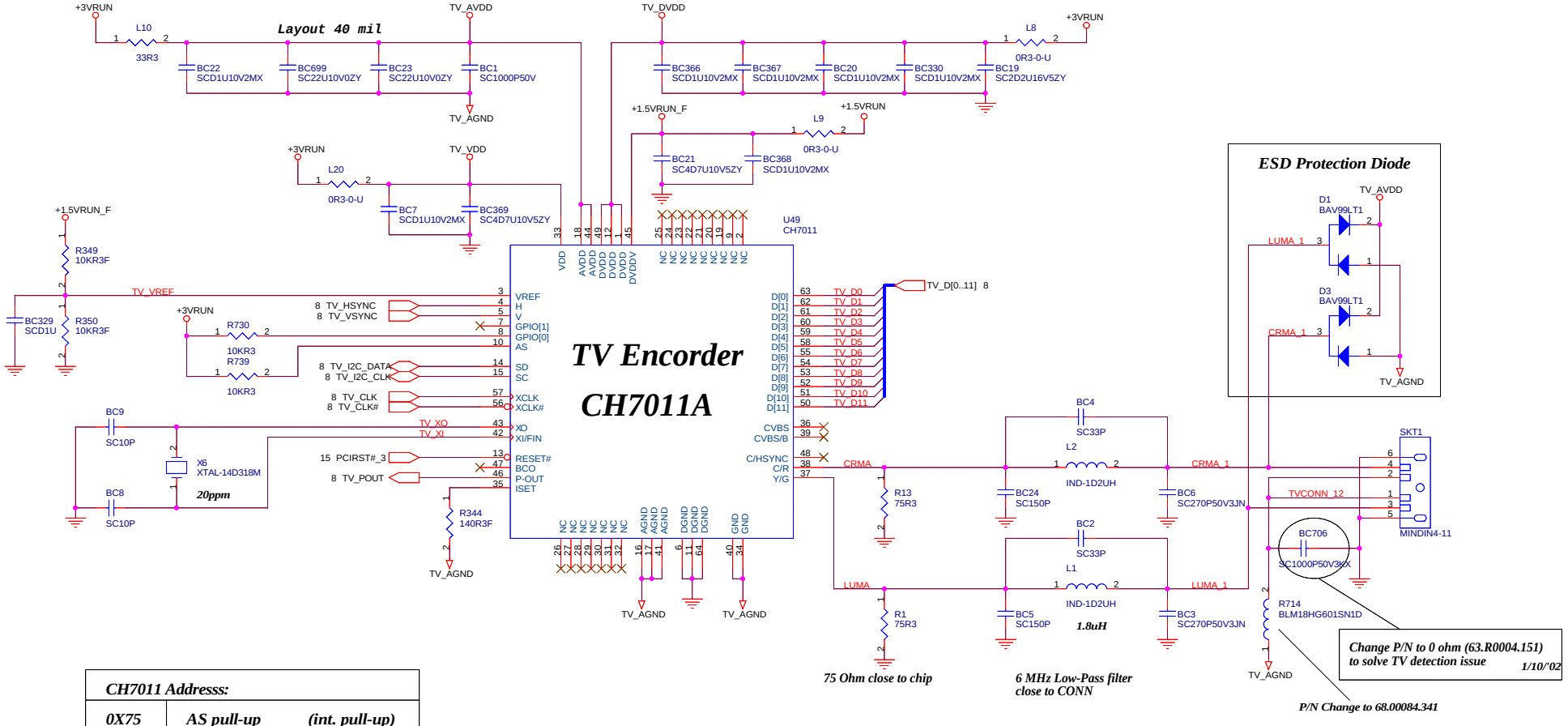
Title: *VCH*

Size: A3 | Document Number: *C-Note 2* | Rev: -3

Date: Friday, January 11, 2002 | Sheet 11 of 37



CH7011 Addresss:		
0X75	AS pull-up	(int. pull-up)
0X76	AS pull-down	

Power up default:		
NTSC	GPIO0 pull-up	(int. pull-up)
PAL	GPIO0 pull-down	

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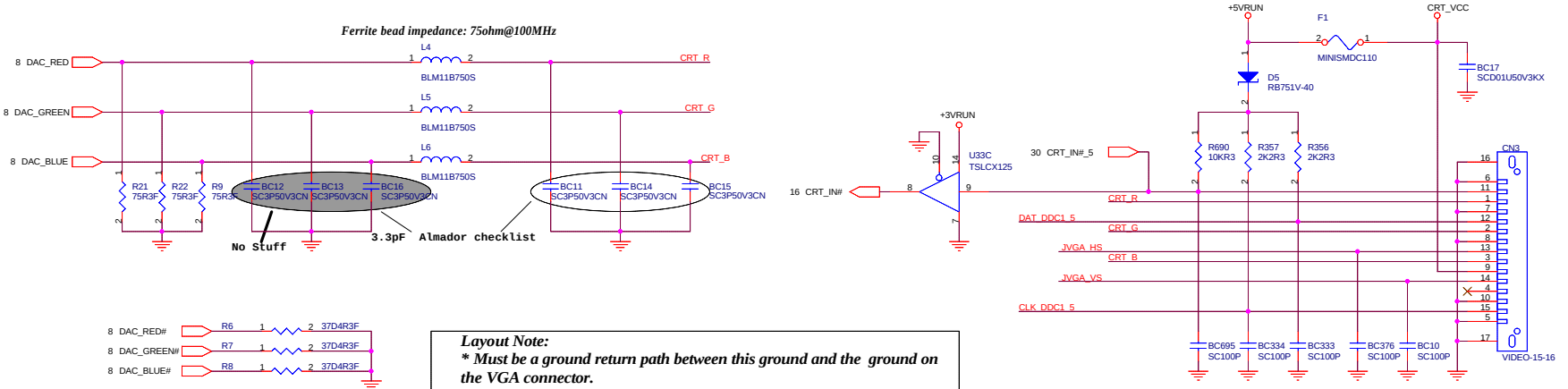
Title	TV Encorder	
Size A3	Document Number C-Note 2	Rev -3
Date: Friday, January 11, 2002	Sheet 12 of 37	

CRT I/F & CONN

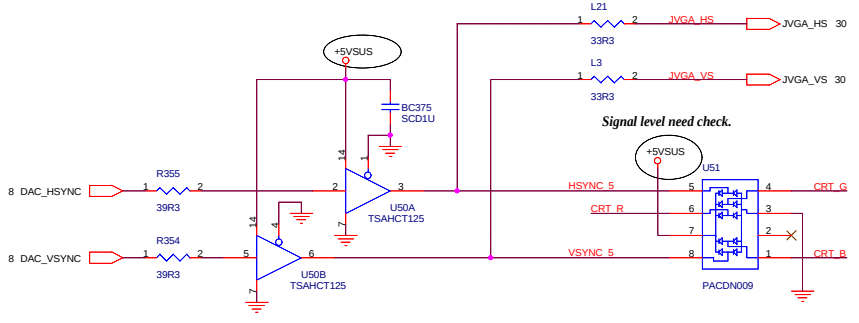


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
**** 37.4_1% resistors must be placed at the same place as the RGB 75 Ohm pull-down resistors.***

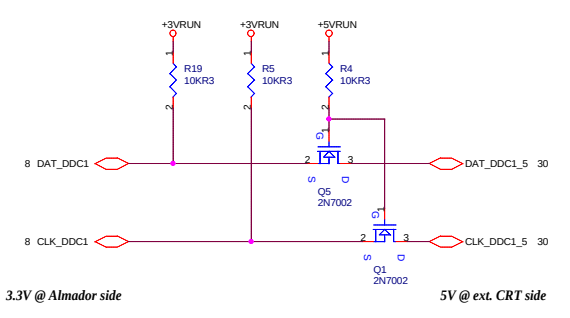
Pi-filter & 75 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

RDDP 1.0

Hsync & Vsync level shift



DDC_CLK & DATA level shift



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Title: **CRT Connector**

Size: Custom | Document Number: **C-Note 2** | Rev: -3

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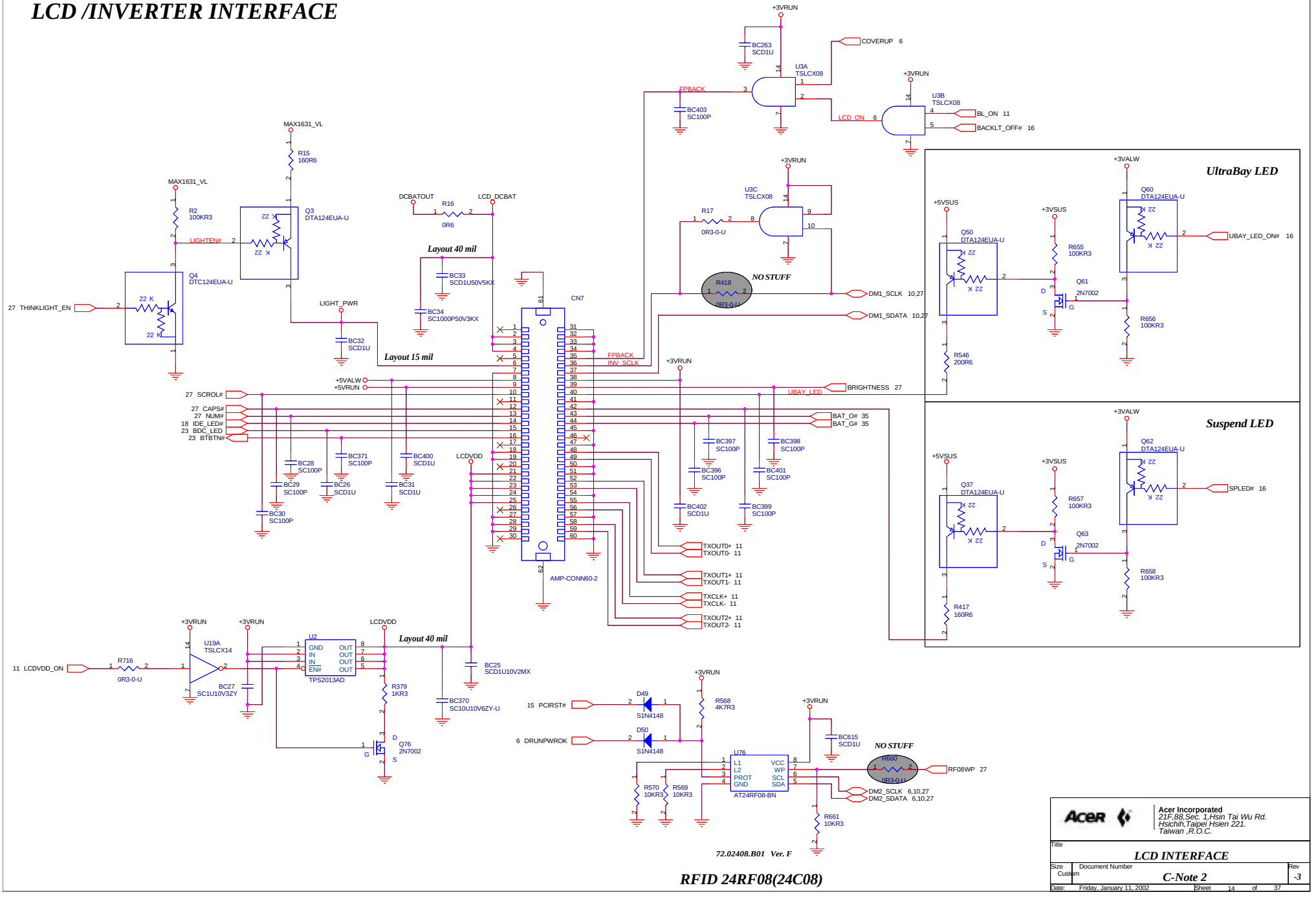
LCD /INVERTER INTERFACE



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Title	LCD INTERFACE	
Size: Custom	Document Number: C-Note 2	Rev: -3
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PCI I/F Pullups

+3VRUN

RN44 RS2N822J1-U: 2-3 DOCK_ATTACH#, 1-4 PIRQE#
RN46 RS2N822J1-U: 2-3 P_STOP#, 1-4 P_SERR#
RN48 RS2N822J1-U: 2-3 P_REQ#3, 1-4 PIRQB#
RN50 RS2N822J1-U: 2-3 PIRQF#, 1-4 PIRQD#
RN51 RS2N822J1-U: 2-3 PIRQC#, 1-4 P_REQ#2
RN52 RS2N822J1-U: 2-3 PIRQA#, 1-4 P_PERR#
RN53 RS2N822J1-U: 2-3 P_FRAME#, 1-4 P_REQ#0

+3VALW
R157 10KR3 1-2 ICH_PME#
NO STUFF

ICH_PME# has weak internal pullup.

+3VRUN
U32C TSLCX08
PCIRST#_3 10 → 9, 14; 8 → PCIRST# 6,14,21,22,26,27,28
7

PCIRST# Buffer to enhance the driving strength

+5VRUN
U43A TSAHCT125
PCIRST#_3 2 → 1, 14; 3 → RSTDRV#_5 18
7

PCIRST# 3V to 5V level shift for HDD & CDROM

Interrupt I/F Pullups

+3VRUN
RN45 RS2N822J1-U: 3-2 P_REQ#1, 4-1 P_DEVSEL#
RN47 RS2N822J1-U: 3-2 P_IRDY#, 4-1 P_PLOCK#
R583 1-2 P_SERIRQ
8K2R3

ICH3-M

PART A

System Management I/F

U75A ICH3-M-U

20,21,22 P_AD[0..31]
20,21,22 P_C/BE#[0..3]

PCI BUS:
P_AD0 J2 PCI_AD0
P_AD1 K1 PCI_AD1
P_AD2 J4 PCI_AD2
P_AD3 K3 PCI_AD3
P_AD4 H5 PCI_AD4
P_AD5 K4 PCI_AD5
P_AD6 H3 PCI_AD6
P_AD7 L1 PCI_AD7
P_AD8 L2 PCI_AD8
P_AD9 G2 PCI_AD9
P_AD10 L4 PCI_AD10
P_AD11 H4 PCI_AD11
P_AD12 M4 PCI_AD12
P_AD13 J3 PCI_AD13
P_AD14 M5 PCI_AD14
P_AD15 J1 PCI_AD15
P_AD16 F5 PCI_AD16
P_AD17 N2 PCI_AD17
P_AD18 G4 PCI_AD18
P_AD19 P2 PCI_AD19
P_AD20 G1 PCI_AD20
P_AD21 P1 PCI_AD21
P_AD22 F2 PCI_AD22
P_AD23 P3 PCI_AD23
P_AD24 F3 PCI_AD24
P_AD25 R1 PCI_AD25
P_AD26 E2 PCI_AD26
P_AD27 N4 PCI_AD27
P_AD28 D1 PCI_AD28
P_AD29 P4 PCI_AD29
P_AD30 E1 PCI_AD30
P_AD31 P5 PCI_AD31

P_C/BE#0 K2 PCI_C/BE#0
P_C/BE#1 K5 PCI_C/BE#1
P_C/BE#2 N1 PCI_C/BE#2
P_C/BE#3 R2 PCI_C/BE#3

P_GNT#0 A4 PCI_GNT#0
E3 PCI_GNT#1
D2 PCI_GNT#2
D5 PCI_GNT#3
P_GNT#4 B4 PCI_GNT#4

20 P_GNT#1
21 P_GNT#2
22 P_GNT#3

P_REQ#0 D3 PCI_REQ#0
P_REQ#1 F4 PCI_REQ#1
A3 PCI_REQ#2
R4 PCI_REQ#3
P_REQ#4 E4 PCI_REQ#4

20 P_REQ#1
21 P_REQ#2
22 P_REQ#3

CLKPCIF_ICH T5 PCI_CLK
20,21,22 P_DEVSEL# M3 PCI_DEVSEL#
20,21,22 P_FRAME# F1 PCI_FRAME#
23 BT_SMI C4 PCI_GPIO0/REQA#
P_REQB# D4 PCI_GPIO1/REQB#/REQ5#
P_GNTA# B6 PCI_GPIO16/GNTA#
P_GNTB# B3 PCI_GPIO17/GNTB#/GNTS#
N3 PCI_IRDY#
20,21,22 P_IRDY# G5 PCI_PAR
20,21,22 P_PAR M2 PCI_PERR#
20,21,22 P_PERR# M1 PCI_LOCK#
P_PLOCK# W1 PCI_PME#
20,22 ICH_PME# Y1 PCI_RST#
7,11,12,17 PCIRST#_3 L5 PCI_SERR#
20,21,22 P_SERR# H2 PCI_STOP#
20,21,22 P_STOP# H1 PCI_TRDY#
20,21,22 P_TRDY#

TPAD30 TP29

CPU Interface:
SM_INTRUDER# Y6
SMLINK0 AC3 SMLINK0
SMLINK1 AB2 SMLINK1
SMB_CLK AC4 ICH_SCL_3
SMB_DATA AB5 ICH_SDA_3
SMB_ALERT#/GPIO11 AC5

CPU_A20GATE Y22 ICH_A20GATE 27
CPU_A20M# Y23 CC_A20M# 4
CPU_DPLSP# AB22 CPU_DPLSP# → R542 1-2 0R3-0-U → CC_DPSLP# 4,31
CPU_FERR# J22 CC_FERR# 4
CPU_IGNNE# AA21 CC_IGNNE# 4
CPU_INIT# AB23 CC_INIT# 4,26
CPU_INTR AA23 CC_INTR 4
CPU_NMI Y21 CC_NMI 4
CPU_PWRGOOD W23 CC_CPUPWRGD 4
CPU_RCIN# U22 RCIN# 27
CPU_SLP# W21 CPU_SLP# → TP22 TPAD30
CPU_SMI# Y23 CC_SMI# 4
CPU_STPCLK# U23 CC_STPCLK# 4

HUB Interface:
HUB_PD0 L22 HL_0
HUB_PD1 M21 HL_1
HUB_PD2 M23 HL_2
HUB_PD3 N20 HL_3
HUB_PD4 P21 HL_4
HUB_PD5 R22 HL_5
HUB_PD6 R20 HL_6
HUB_PD7 T23 HL_7
HUB_PD8 M19 HL_8
HUB_PD9 P19 HL_9
HUB_PD10 N19 HL_10
HL_[0..10] 7
TP5 TPAD30

CLK66 T19 CLK66_ICH
HUB_PAR R19
HI_STB N22 HL_STB 7
HI_STB# P23 HL_STB# 7
HUB_RCOMP K19 HUB_RCOMP_ICH3
HUB_VREF L20
HUB_VSWING L19 HUB_VSWING → HUBREF 7,9

INTERRUPT Interface:
INT_APICCLK J19 APICCLK_ICH
INT_APICD0 J20 CC_PICD0 4
INT_APICD1 J21 CC_PICD1 4
INT_PIRQA# B1 PIRQA#
INT_PIRQB# C1 PIRQB# 20
INT_PIRQC# B2 PIRQC# 22
INT_PIRQD# A2 PIRQD#
INT_PIRQE#/GPIO2 A6 PIRQE# 22
INT_PIRQF#/GPIO3 B5 PIRQF# 21
INT_PIRQG#/GPIO4 C5 HOTKEY 27
INT_PIRQH#/GPIO5 A5 DOCK_ATTACH# 30
INT_IRQ14 AB14 IRQ14 18
INT_IRQ15 W19 IRQ15 18
INT_SERIRQ H22 P_SERIRQ 20,22,27,28

EEPROM I/F:
EEP_CS E9 EEP_CS
EEP_DIN D8 EEP_DIN
EEP_DOUT E8 EEP_DOUT
EEP_SHCLK D10 EEP_SHCLK

LAN I/F:
LAN_RXD0 C8 LAN_RXD0 LAN_RXD0 19
LAN_RXD1 A8 LAN_RXD1 LAN_RXD1 19
LAN_RXD2 A9 LAN_RXD2 LAN_RXD2 19
LAN_TXD0 B9 LAN_TXD0 LAN_TXD0 19
LAN_TXD1 C10 LAN_TXD1 LAN_TXD1 19
LAN_TXD2 A10 LAN_TXD2 LAN_TXD2 19
LAN_JCLK C9 → R577 10R3 → BC631 SC10P → LAN_JCLK 19
LAN_RSTSYNC D7 LAN_RSTSYNC 19

VCC_RTC
R159 22KR3 NO STUFF
INTRUDER# 6
R691 1MR3

+5VRUN
R662 10KR3
Q64 2N7002
RN43 RS2N103J1-U
Q65 2N7002
ICH_SCL 3,27
ICH_SDA 3,27

+3VALW
RN12 RS2N472J1-U
RN26 RS2N472J1-U
R541 10KR3

HUB INTERFACE LAYOUT
Route signals with 5/20 trace/space routing.
Signals must match +/- 0.1" of HUB_STB/STB# signals.

Kodiak Ver. 0.7

R199 1-2 36D5R3F

PLACE RCOMP resistor within 0.5" of ICH pad using a thick trace
RCOMP should be 2/3 board impedance

SC-3062

HUB I/F VSWING VOLTAGE

+1.8VRUN
R247 301R3F
R248 301R3F
BC222 SCD01U50V3KX
BC221 SCD1U

LAYOUT NOTE: Place divider pair in middle of bus.

BC153 SCD01U50V3KX
CLOSE TO PIN

CLK66_ICH 3
R202 1-2 51D1R3F → CLKAPIC_ICH 3
R176 10R3
R200 DUMMY-R3
R201 348R3F
BC150 SC10P
BC180 DUMMY-C3
10pF
No Stuff
12/14/00

CLK termination close to ICH

+3VRUN
R99 2-1 P_REQB# 10KR3
TP9 TPAD30 P_GNT#0
TP8 TPAD30 P_GNT#4
TP23 TPAD30 P_GNTA#

3 CLKPCIF_ICH
R173 10R3
BC141 SC10P

CLK termination close to ICH

Part Number Change to 71.0ICH3.M03

LAN+3VAUX
U31 M93C46-W-2
GND ORG DC VCC DO DI SK CS
5 6 7 8 4 3 2 1
EEP_DIN EEP_DOUT EEP_SHCLK EEP_CS
BC223 SCD1U

EEPROM for LAN

+3VRUN
RN54 RS2N822J1-U 2-3 P_REQ#4, 1-4 P_TRDY#
R543 1-2 HOTKEY 100KR3

No Stuff

H/W Strapping

No Stuff
EEP_DOUT → R250 1KR3 → 1
P_GNTA# → R574 1KR3 → 1

Kodiak V. 0.7b P.19

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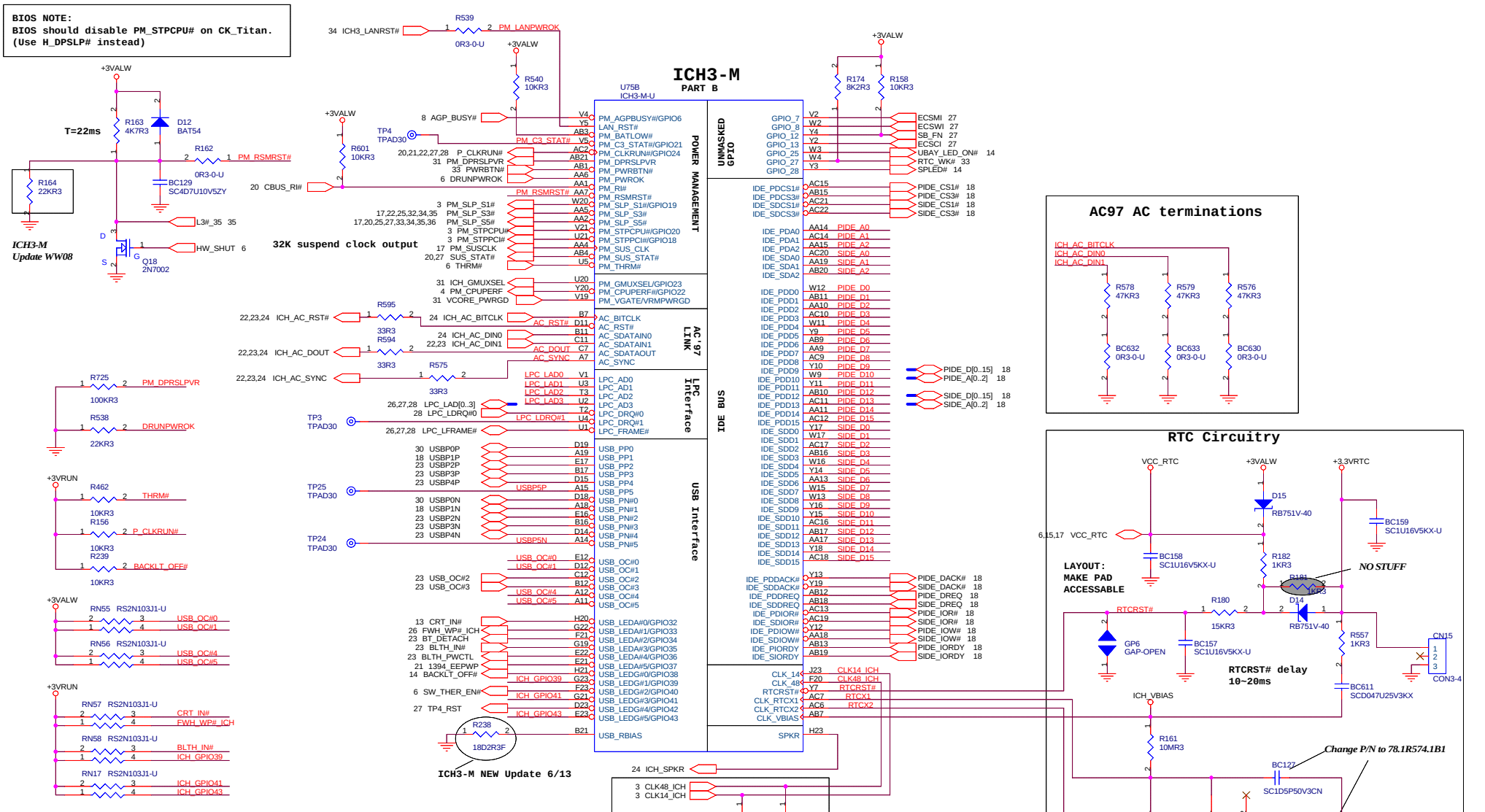
Title: ICH3-M(1/3) PCI,HUBLINK,SM,CPU,INT
Size: A3 | Document Number: C-Note 2 | Rev: -3
Date: Friday, January 11, 2002 | Sheet 15 of 37

BIOS NOTE:
BIOS should disable PM_STPCPU# on CK_Titan.
(Use H_DPSLP# instead)



ICH3 Integrated Pull-up and Pull-down Resistors

EE_DIN , EE_DOUT, LDRQ[1:0] , PME# GNT[B:A]#/GNT[5]#/GPIO[17:16] , LAD[3:0]#/FWH[3:0]# , PWRBTN#	ICH3 internal 24K pull-ups
LAN_RXD[2:0]	ICH3 internal 9K pull-ups
AC_BITCLK, AC_SDIN[0], AC_SDOUT, AC_SDIN[1]/GPIO[9], AC_SYNC,	ICH3 internal 20K pull-downs
SPKR	ICH3 internal 24K pull-downs
PDD[7]/SDD[7], PDDREQ / SDDREQ	ICH3 internal 5.9K pull-downs
DPRSLPVR	ICH3 internal TBD K pull-downs

FM-1882 P4-1,2

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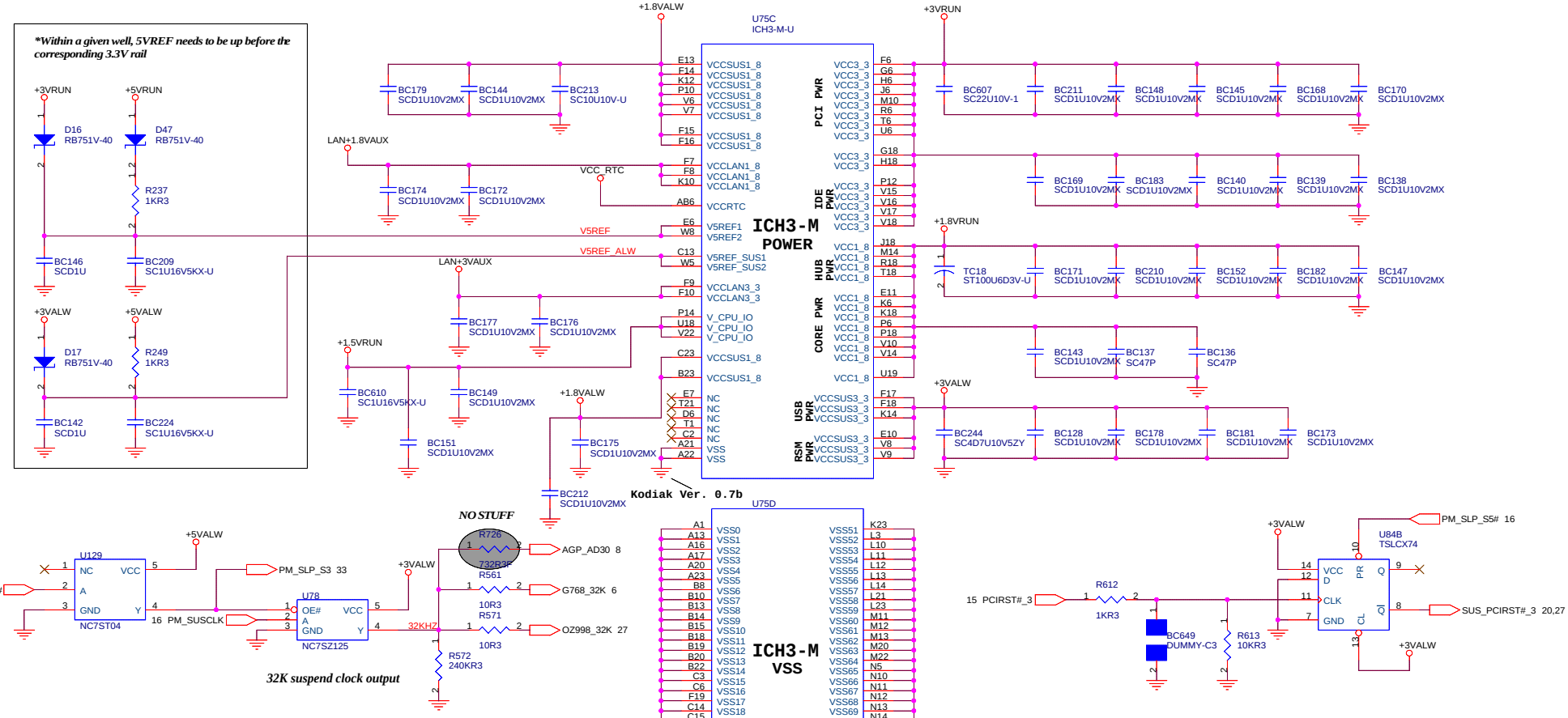
Taiwan, R.O.C.

Title: ICH3-M(2/3) PM,USB,AC'97,LPC,IDE,RTC

Size: Custom | Document Number: C-Note 2 | Rev: -3

Date: Friday, January 11, 2002 | Sheet 16 of 37



ICH3 H/W Pin Straps — FM-1882

AC_SDOUT	SAFE MODE	Rising Edge of PWROK	This signal has a weak int. pull-down. If the signal is sampled high, the ICH3 will set the CPU speed strap pins for safe mode.
EE_DOUT	Reserved		System designers should include a placeholder for a pull-down resistor on EE_DOUT but do not populate the resistor.
GNT[A]#	TOP-SWAP OVERRIDE	Rising Edge of PWROK	This signal has a weak int. pull-up. If the signal is sampled low, this indicates that the system is strapped to the "TOP-SWAP" mode(ICH3 will invert A16 for all cycles targeting FWH BIOS spacing). Note that SW will not be able to clear the Top-Swap bit until the system is rebooted w/o GNT[A]# being pulled down.
DPRSLPVR	HUB INTERFACE TERMINATION SCHEME (PARALLEL vs. SOURCE)	Rising Edge of PWROK	If this signal is sampled low (default due to weak int. pull-down), the termination scheme will be set to source. If this signal is sampled high (via an ext. pull-up to Vcc1_8), the termination scheme will be set to parallel.
SPKR	NO REBOOT	Rising Edge of PWROK	This signal has a weak int. pull-down. If the signal is sampled high, this indicates that the system is strapped to the " No Reboot " mode (ICH3 will disable the TXO Timer system reboot feature).

Decouping Recommendation — Kenora Bulk

+1.5VRUN	0.1uF * 2 1uF / 16V * 1	X
1.8VRUN	0.1uF * 5 47pF * 2	100uF*1+22uF*1
1.8VSUS	0.1uF * 3	10uF * 1
1.8V_ICHLAN	0.1uF * 2	22uF *1
3.3VRUN	0.1uF * 13 47pF * 5	22uF *2
3.3VSUS	0.1uF * 8	22uF *1
3.3V_ICHLAN	0.1uF * 2 47pF * 1	22uF *1

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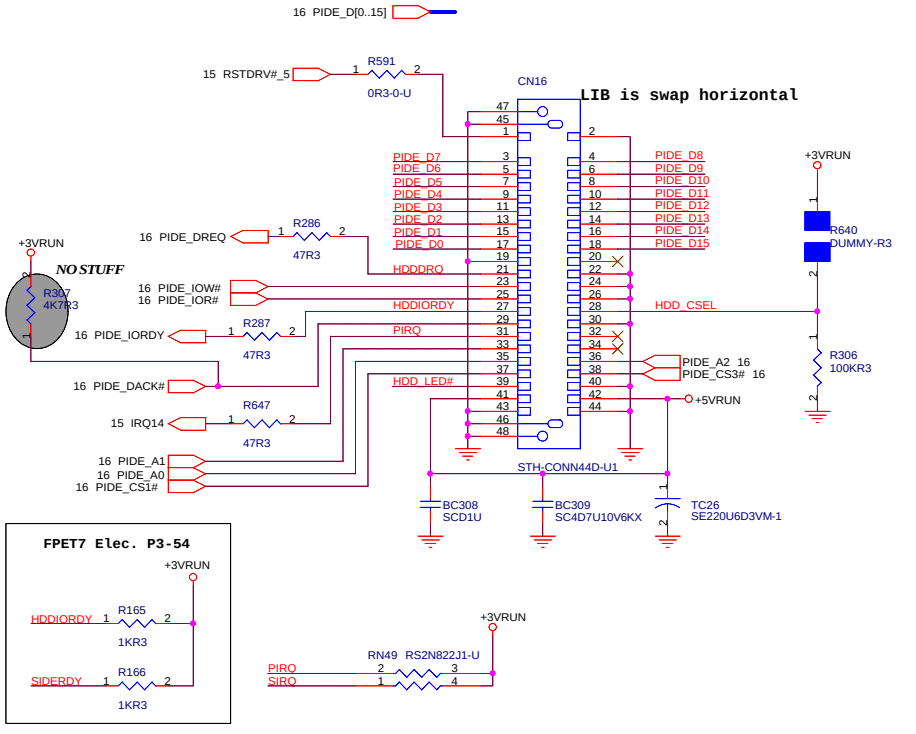
Title: ICH3-M(3/3) POWER,VSS,BYPASS CAPS

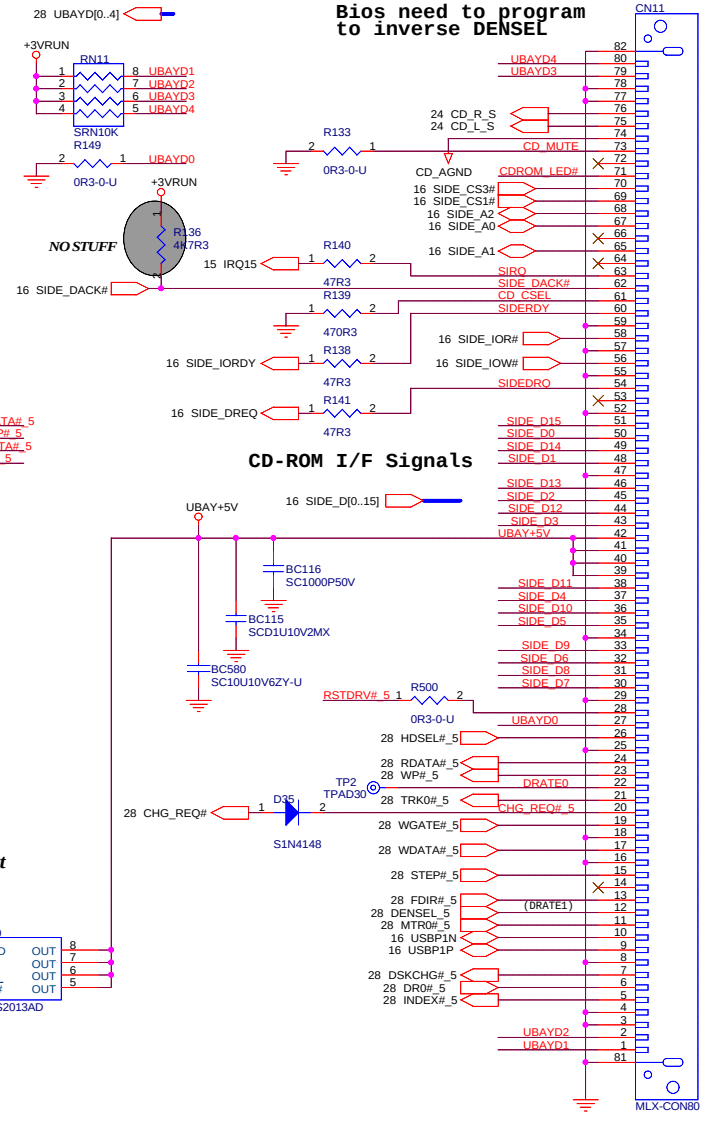
Size: A3 | Document Number: C-Note 2 | Rev: -3

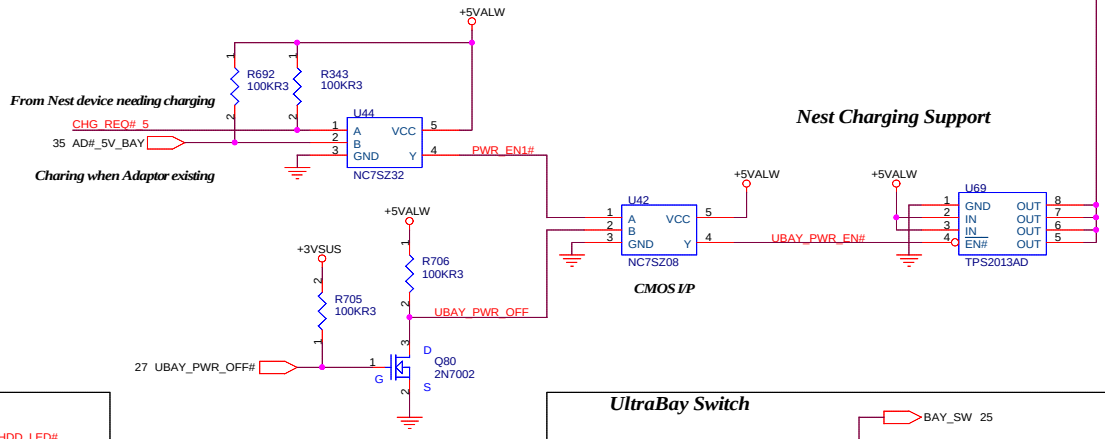
Date: Friday, January 11, 2002 | Sheet 17 of 37

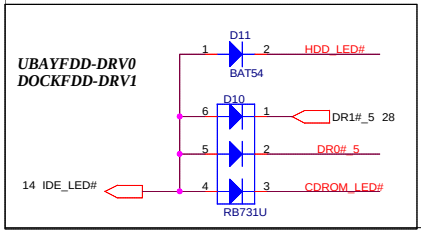
HDD CONN

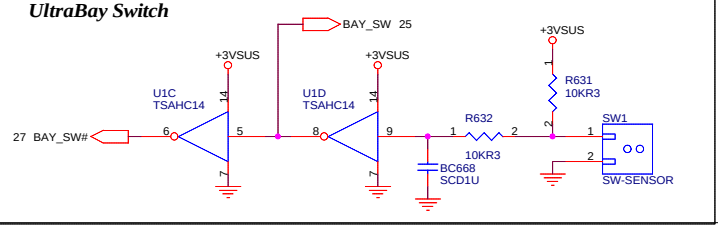


UltraBay CONN









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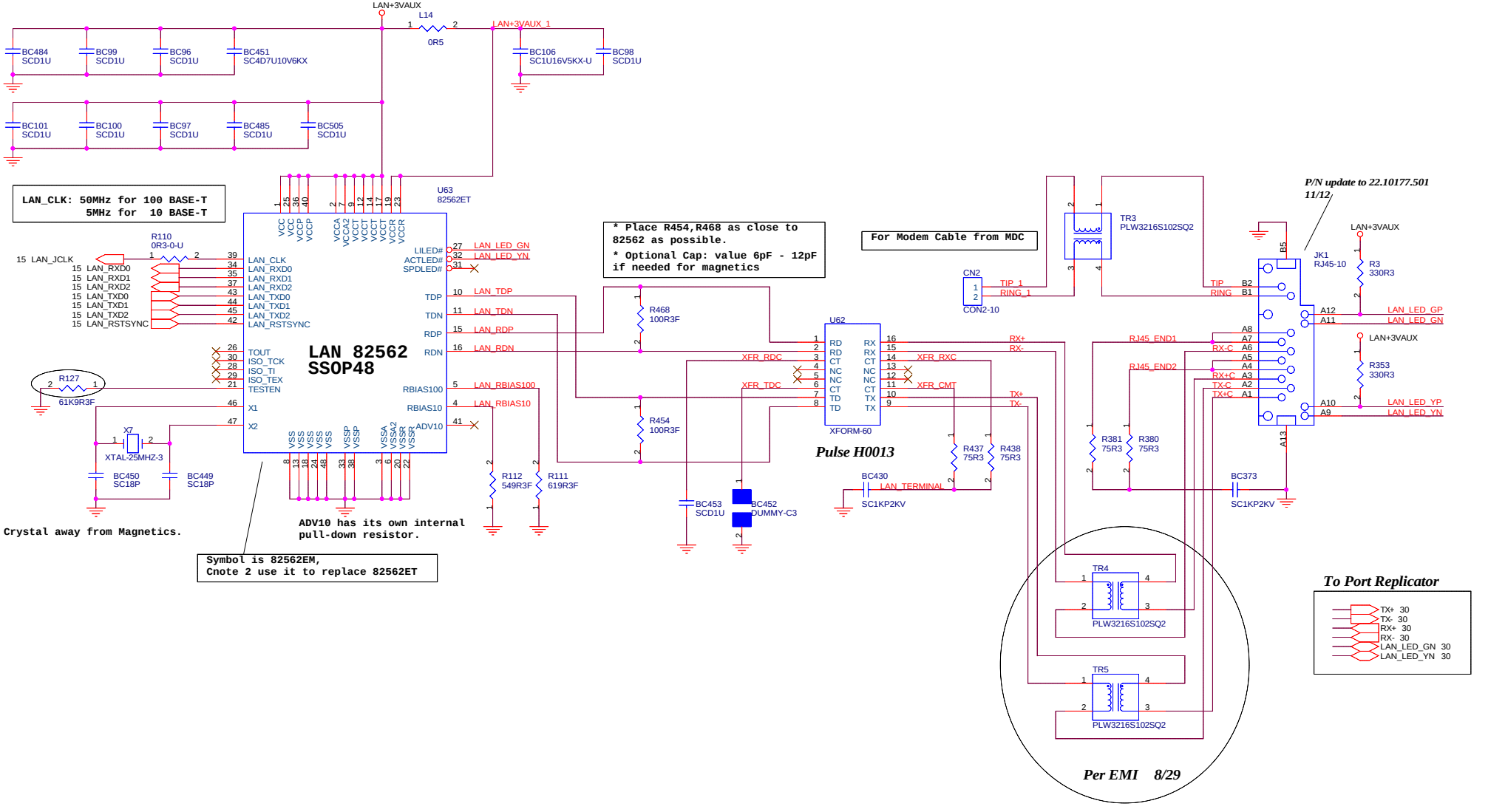
Taiwan ,R.O.C.

Title: IDE & USB INTERFACE

Size	Document Number	Rev
A3	C-Note 2	-3

Date: Friday, January 11, 2002 Sheet 18 of 37


LAN+3VAUX
L14
0R5
LAN+3VAUX_1
BC484 SCD1U
BC99 SCD1U
BC96 SCD1U
BC451 SC4D7U10V6KX
BC106 SC1U16V5KX-U
BC98 SCD1U
BC101 SCD1U
BC100 SCD1U
BC97 SCD1U
BC485 SCD1U
BC505 SCD1U
LAN_CLK: 50MHz for 100 BASE-T
5MHz for 10 BASE-T
U63
82562ET
R110
0R3-0-U
LAN 82562
SS0P48
R127
61K9R3F
X7
XTAL-25MHZ-3
BC450 SC18P
BC449 SC18P
Crystal away from Magnetics.
ADV10 has its own internal pull-down resistor.
Symbol is 82562EM,
Cnote 2 use it to replace 82562ET
R112 549R3F
R111 619R3F
* Place R454,R468 as close to 82562 as possible.
* Optional Cap: value 6pF - 12pF if needed for magnetics
R468 100R3F
R454 100R3F
BC453 SCD1U
BC452 DUMMY-C3
U62
XFORM-60
Pulse H0013
BC430 LAN_TERMINAL SC1KP2KV
R437 75R3
R438 75R3
For Modem Cable from MDC
CN2
CON2-10
TR3
PLW3216S102SQ2
P/N update to 22.10177.501
11/12
JK1
RJ45-10
R3 330R3
R353 330R3
R381 75R3
R380 75R3
BC373 SC1KP2KV
TR4
PLW3216S102SQ2
TR5
PLW3216S102SQ2
Per EMI 8/29
To Port Replicator
TX+ 30
TX- 30
RX+ 30
RX- 30
LAN_LED_GN 30
LAN_LED_YN 30
Acer Incorporated
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Taiwan, R.O.C.
Title
LAN 82562ET
Size A3
Document Number
C-Note 2
Rev -3
Date: Friday, January 11, 2002
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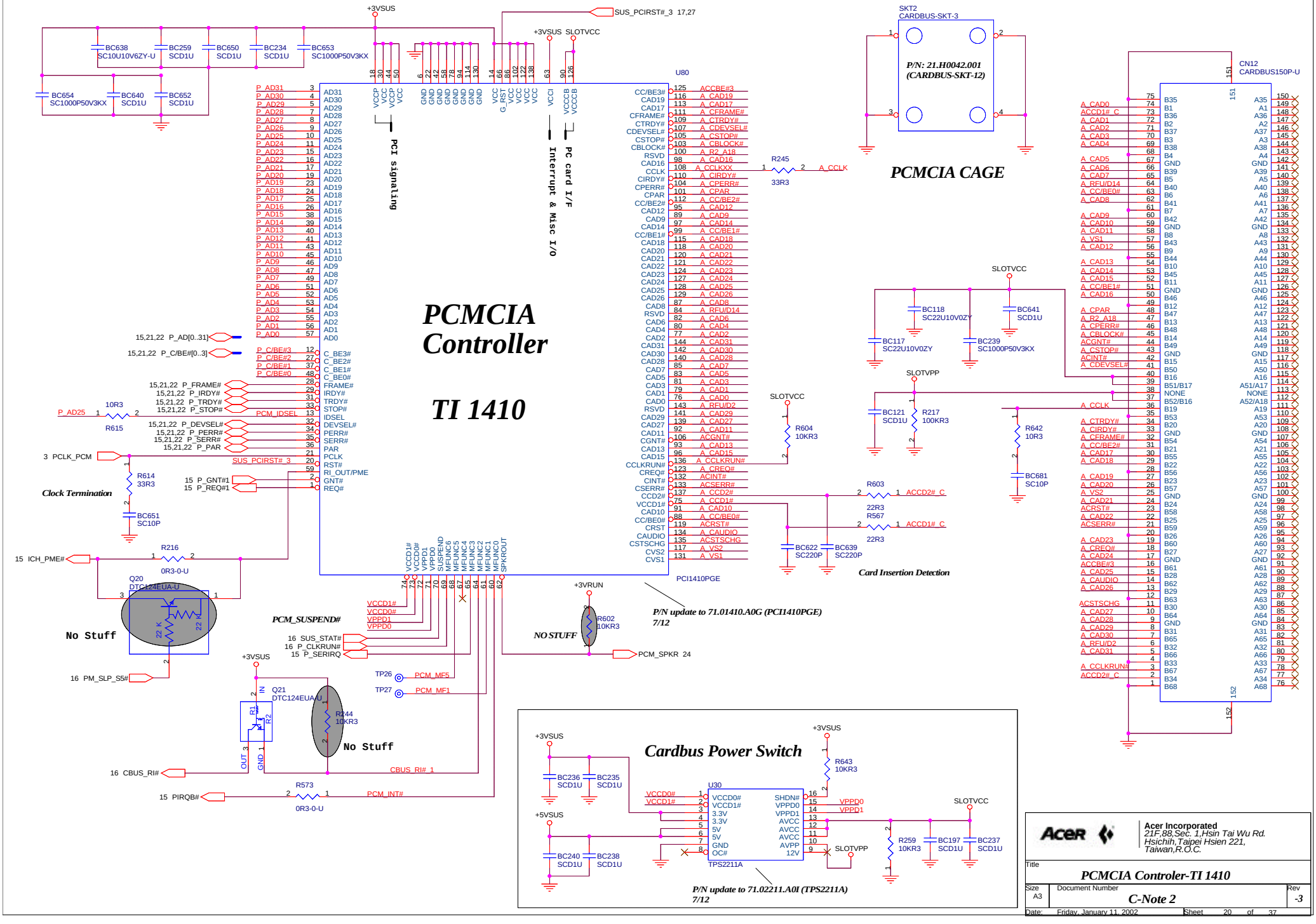
PCMCIA Controller
TI 1410
PCMCIA CAGE
Cardbus Power Switch
Clock Termination
Card Insertion Detection
PCI signaling
Interrupt & Misc I/O
PC card I/F
No Stuff
PCM_SUSPEND#
NO STUFF
P/N update to 71.01410.A0G (PCI1410PGE) 7/12
P/N update to 71.02211.A0I (TPS2211A) 7/12
P/N: 21.H0042.001 (CARDBUS-SKT-12)
U80
PCI1410PGE
U30
TPS2211A
SKT2 CARDBUS-SKT-3
CN12 CARDBUS150P-U
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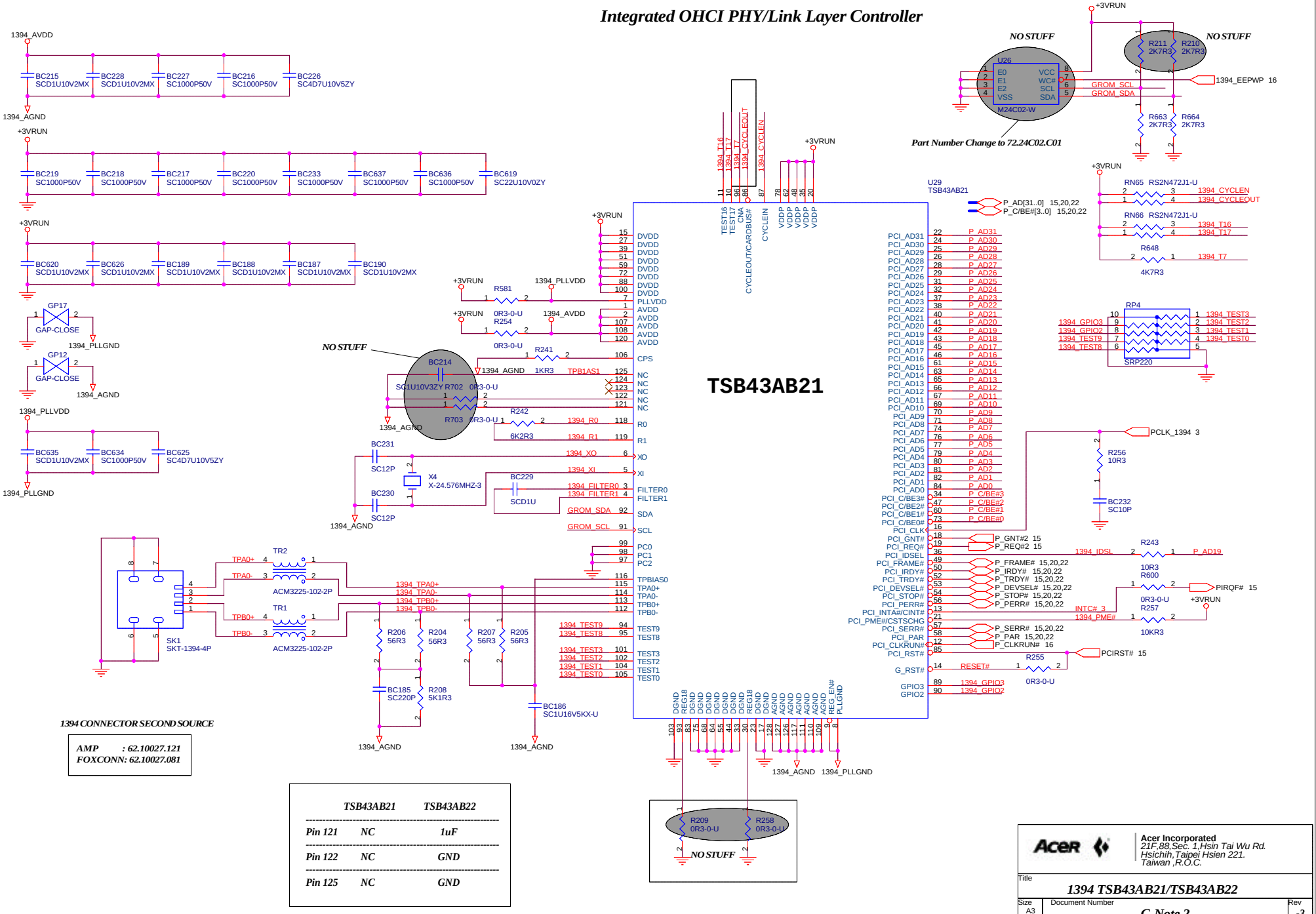
PCMCIA Controler-TI 1410
C-Note 2
Friday, January 11, 2002

Integrated OHCI PHY/Link Layer Controller



1394 CONNECTOR SECOND SOURCE

AMP	***: 62.10027.121***
FOXCONN:	***62.10027.081***

TSB43AB21	*TSB43AB22*	
Pin 121	*NC*	*1uF*
Pin 122	*NC*	*GND*
Pin 125	*NC*	*GND*

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Taiwan ,R.O.C.

Title: ***1394 TSB43AB21/TSB43AB22***

Size: A3 | Document Number: ***C-Note 2*** | Rev: *-3*

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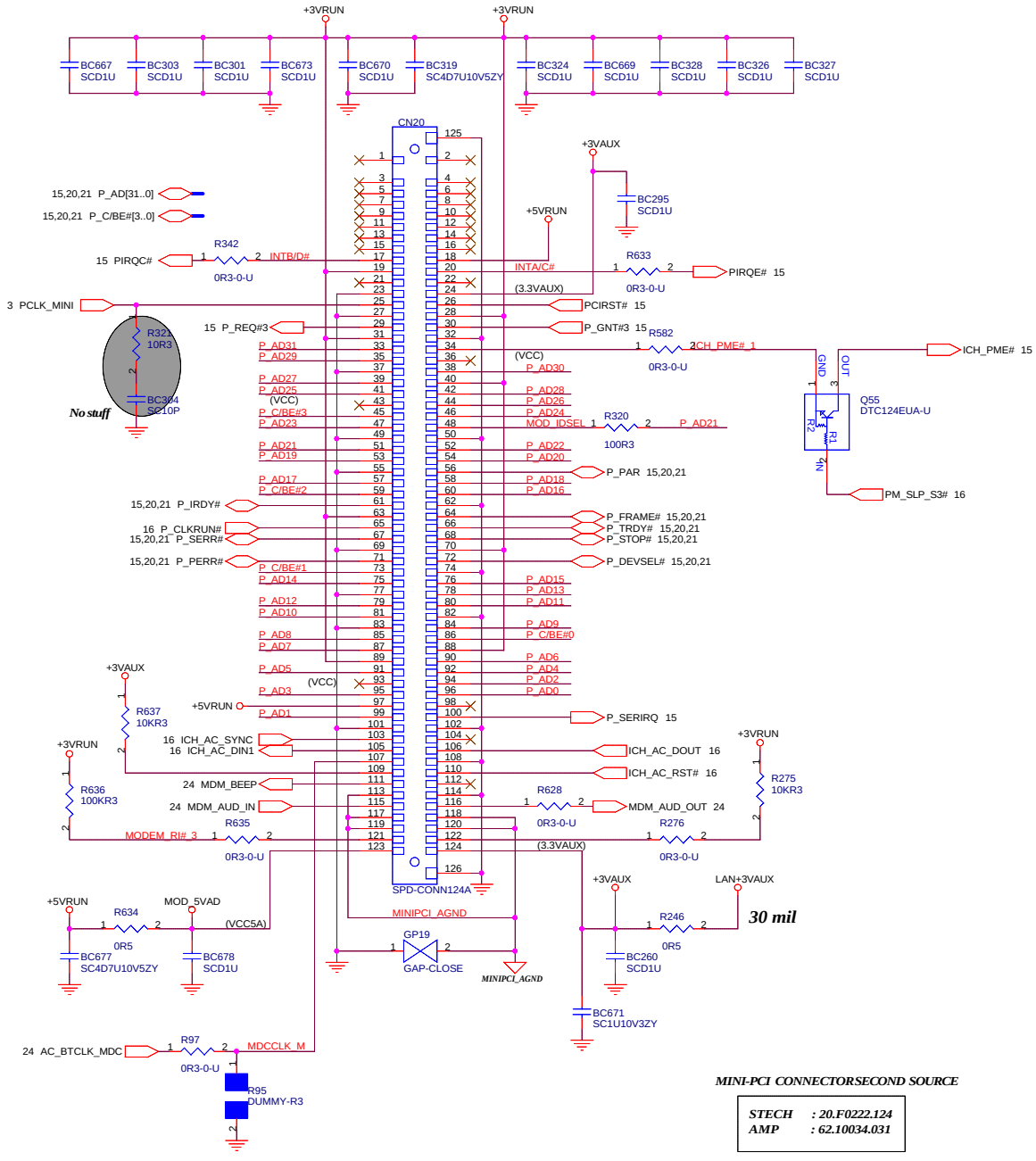
MiniPCI Socket

20.F0222.124 4/18



MINI-PCI CONNECTORSECOND SOURCE

STECH	***: 20.F0222.124***
AMP	***: 62.10034.031***

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Taiwan ,R.O.C.

Title: ***Mini PCI SOCKET & MDC MODEM***

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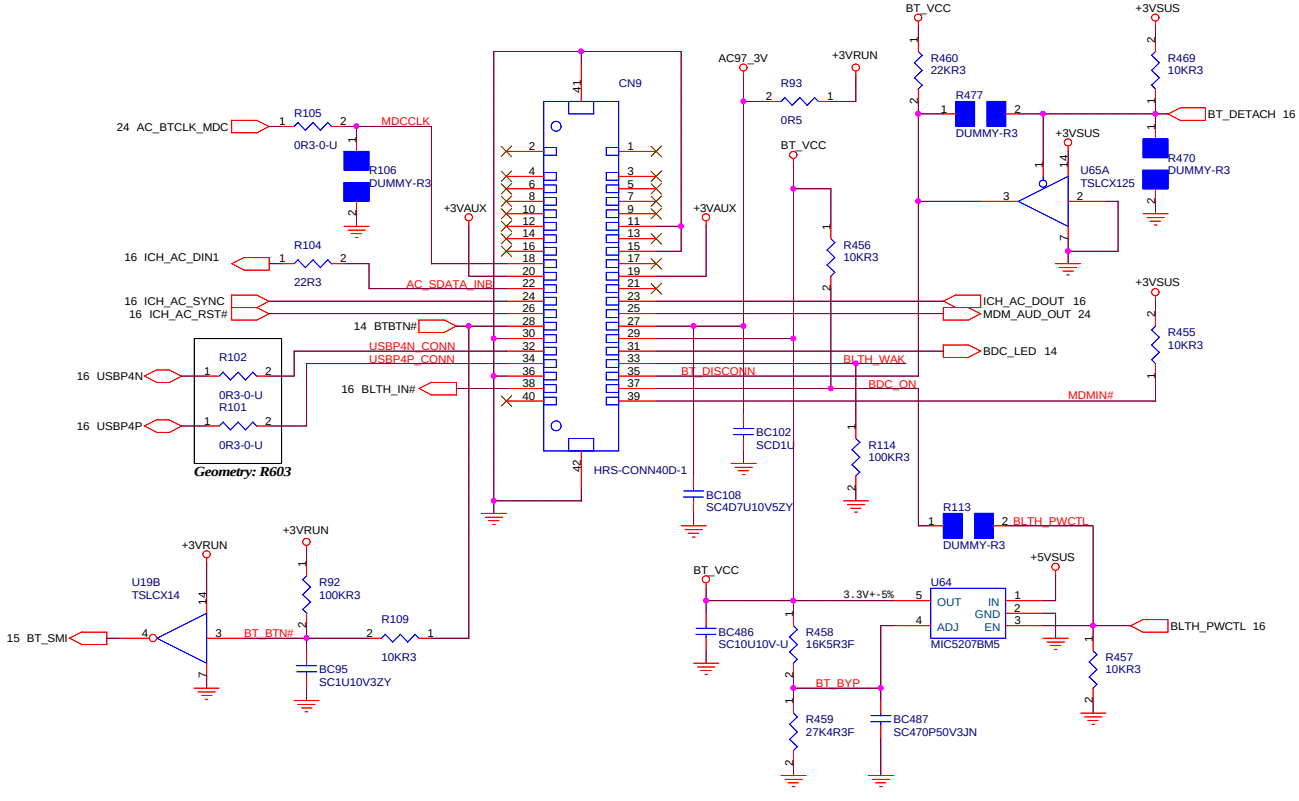
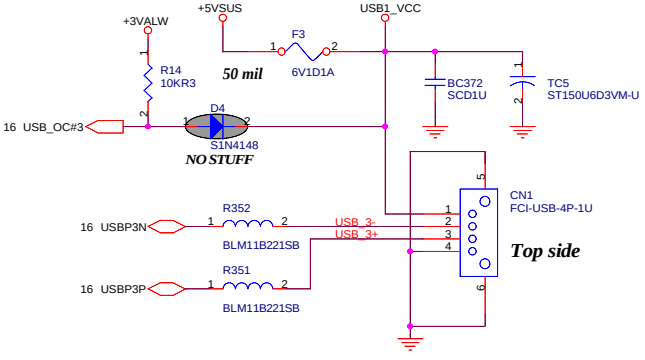
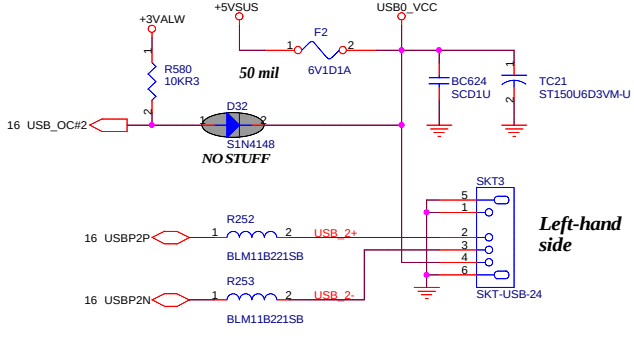
CDC Connector





USB PORT



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Taiwan, R.O.C.

Title: BLUETOOTH MODULE

Size: A3 | Document Number: C-Note 2 | Rev: -3

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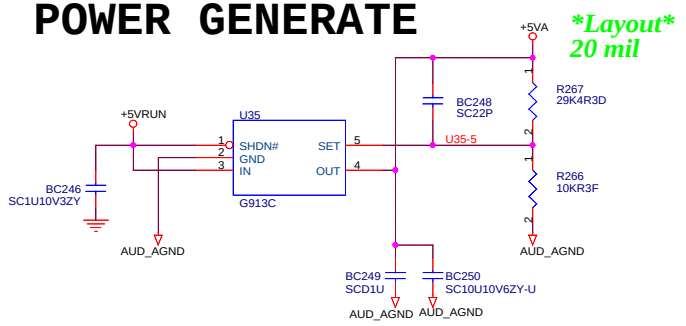
AD1881A AC97 AUDIO CODEC

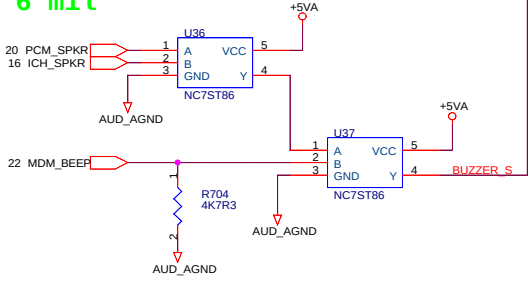
POWER GENERATE

Layout
20 mil



BEEP SOUND LOGIC

Layout
locate near audio moat opening
6 mil



Layout
AUDIO(analog)
(20,10) mil

Layout
AC-LINK(digital)
6 mil

Layout
20 mil

Change P/N to 78.90034.1B1
11/09

Per EMI request
Jan 3 '02

U39
AD1881A

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Title	AC'97 CODEC - AD1881A
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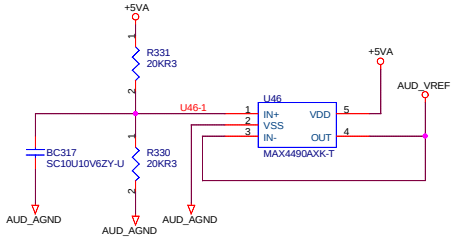
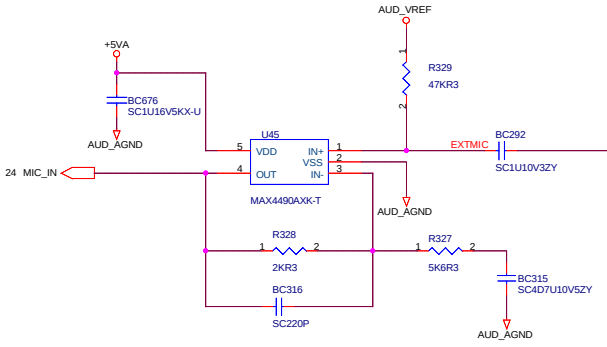
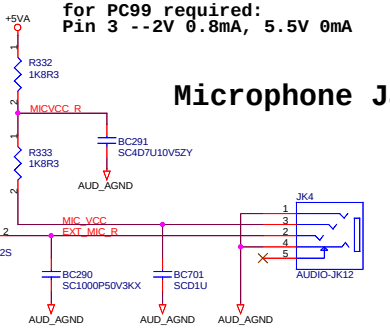
AUDIO VREF GENERATE



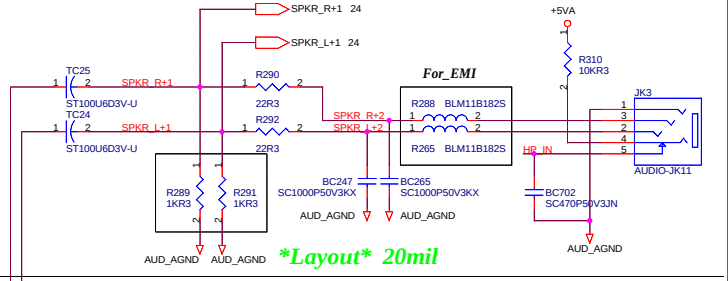
EXT. MICROPHONE IN



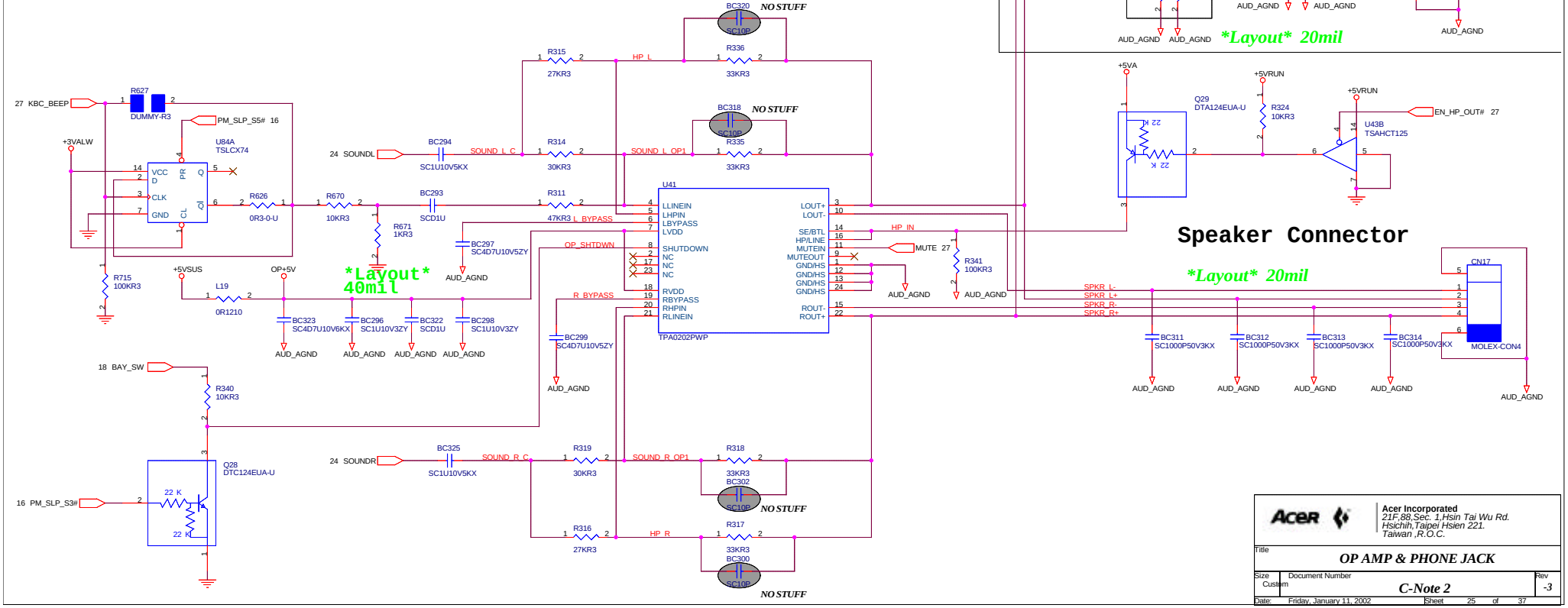
Microphone Jack



Headphone Jack



AUDIO OP AMPLIFIER



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Title: OP AMP & PHONE JACK

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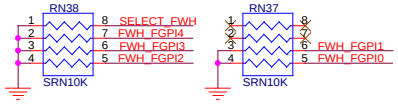
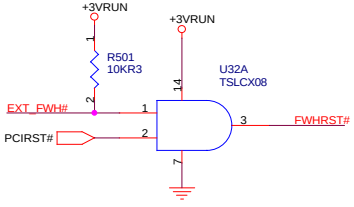
Unused FGPI pins must not be float



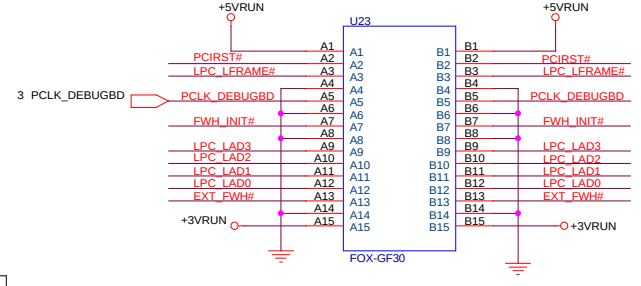


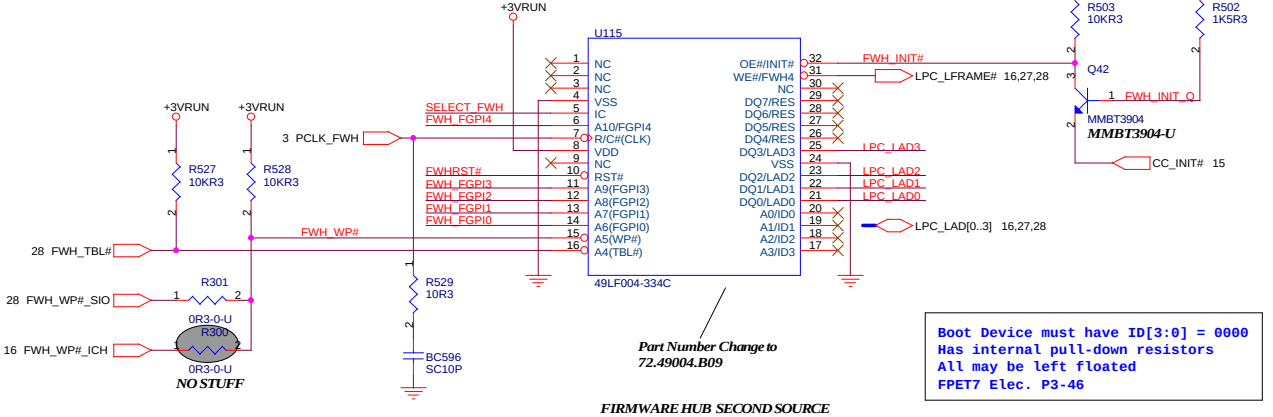
TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD



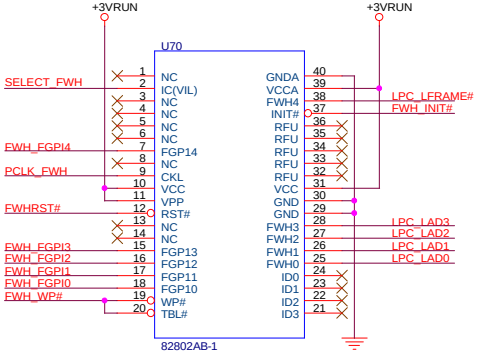


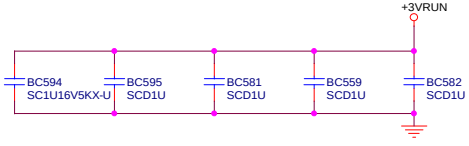
Part Number Change to 72.49004.B09

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

FIRMWARE HUB SECOND SOURCE

SST : 72.49004.B09
STM : 72.50040.009





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Title: *FIRMWARE HUB & DEBUG PORT*

Size	Document Number	Rev
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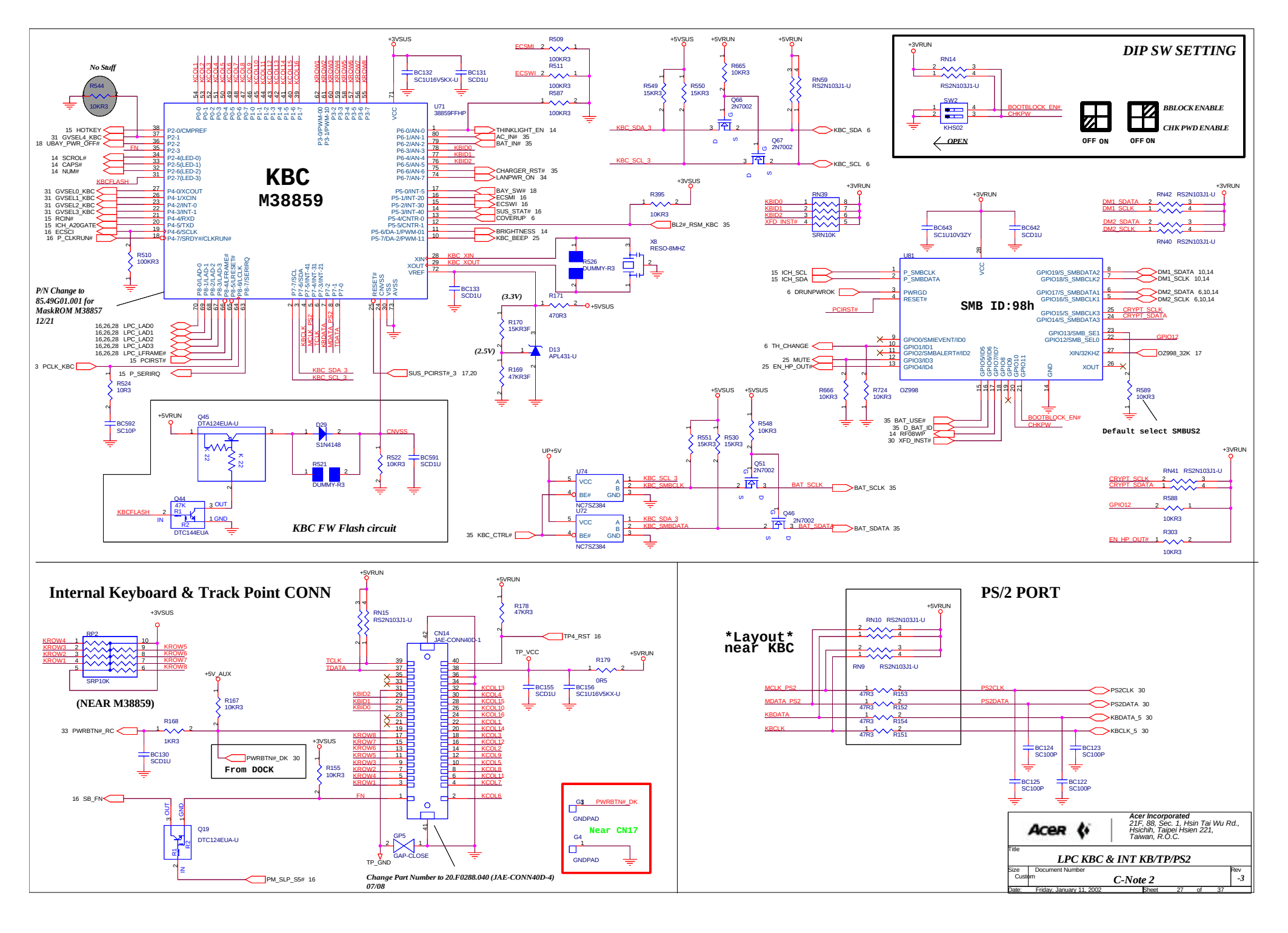
KBC
M38859
No Stuff
P/N Change to
85.49G01.001 for
MaskROM M38857
12/21
KBC FW Flash circuit
DIP SW SETTING
BBLOCK ENABLE
CHK PWD ENABLE
OFF ON
OFF ON
OPEN
SMB ID:98h
Default select SMBUS2
Internal Keyboard & Track Point CONN
(NEAR M38859)
From DOCK
Change Part Number to 20.F0288.040 (JAE-CONN40D-4)
07/08
Near CN17
PS/2 PORT
Layout
near KBC
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.
LPC KBC & INT KB/TP/PS2
C-Note 2
-3
Friday, January 11, 2002
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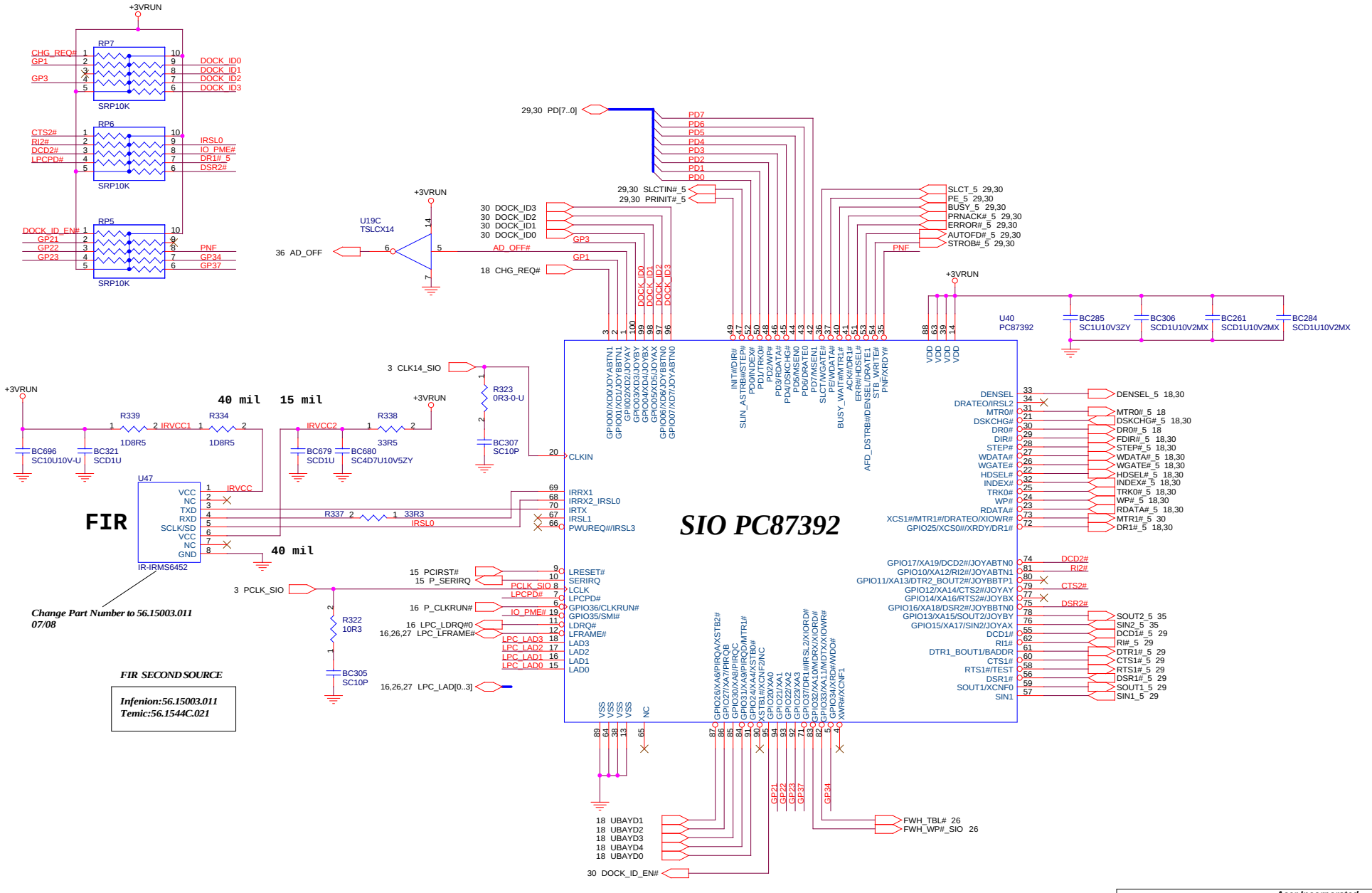
37



Acer Incorporated 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LPC SIO		
Size: A3	Document Number: C-Note 2	Rev: -3
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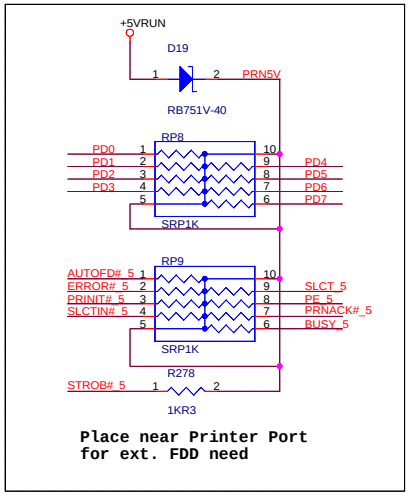
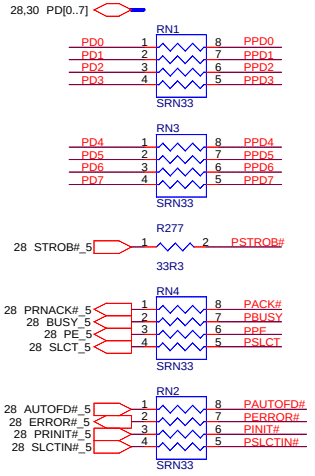
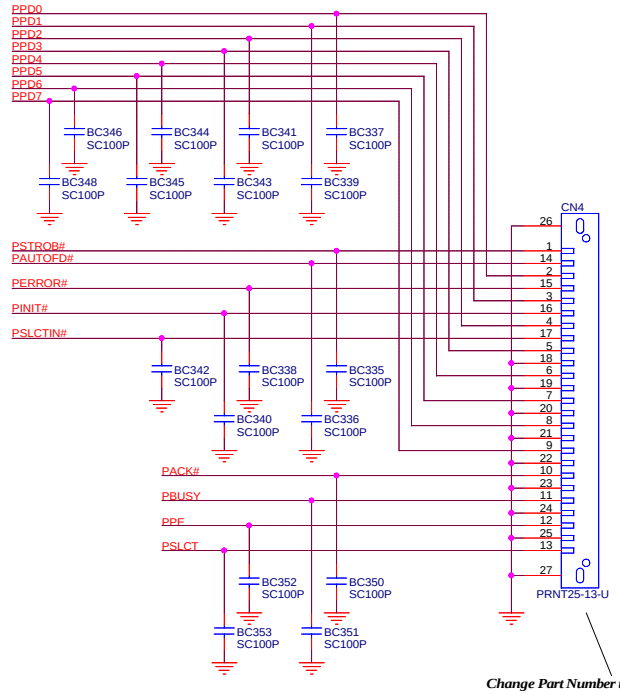


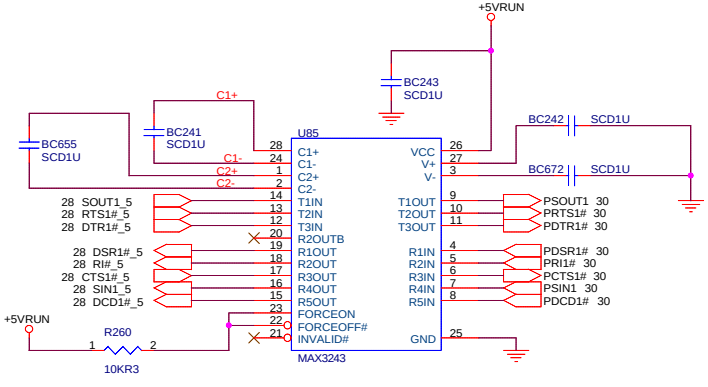


Place CAPs close to CONN

Printer Port



Change Part Number to 20.B0028.025 (AMP-CON25)
07/08



RS232 Transceiver

RS232 SECOND SOURCE

MAXIM:74.03243.0F9
TI :74.03243.FF9

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Title: ***LPC SIO***

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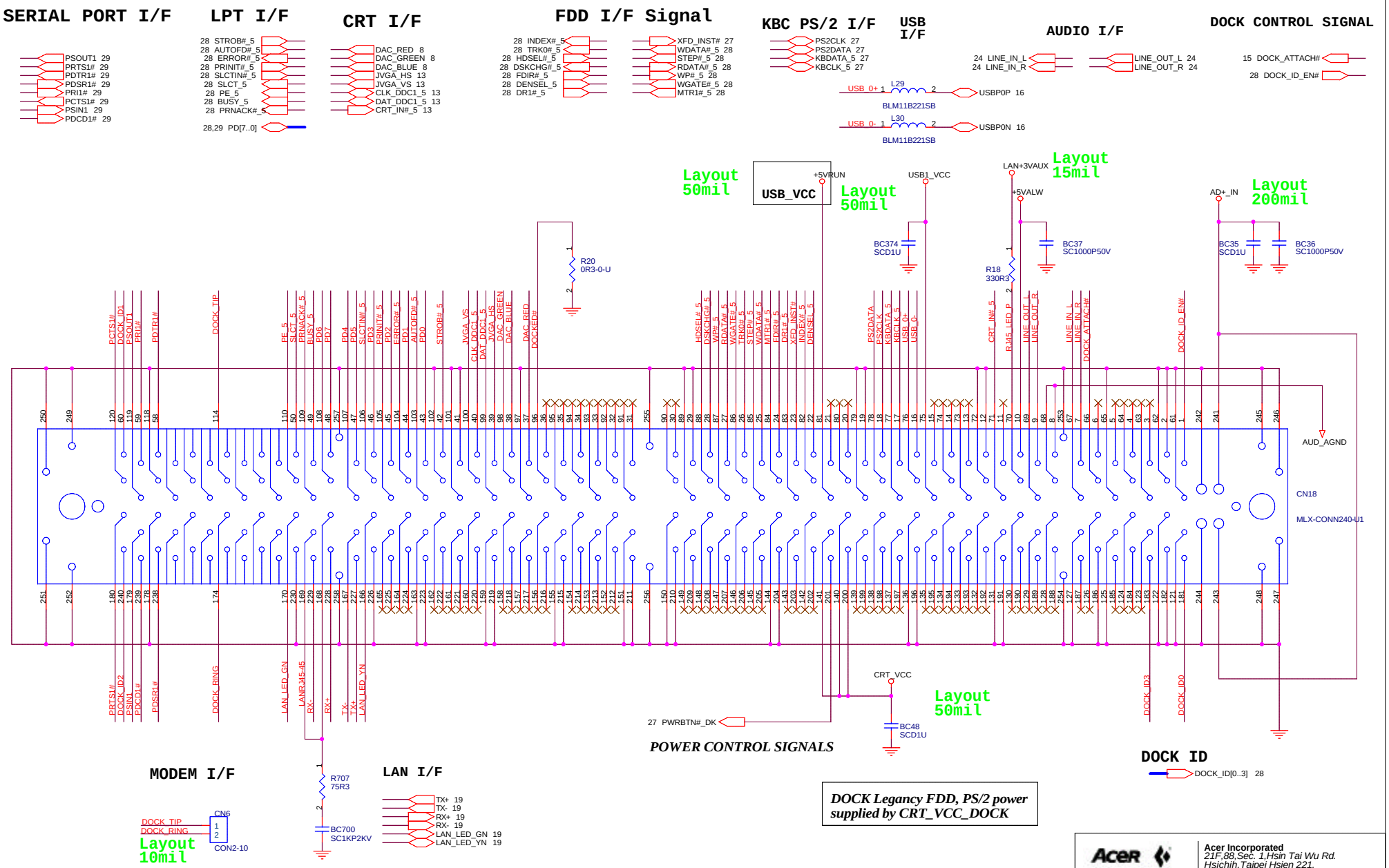
SERIAL PORT I/F
PSOUT1 29
PRTS1# 29
PDTR1# 29
PDSR1# 29
PRI1# 29
PCTS1# 29
PSIN1 29
PDCD1# 29
LPT I/F
28 STROB#_5
28 AUTOFD#_5
28 ERROR#_5
28 PRINIT#_5
28 SLCTIN#_5
28 SLCT_5
28 PE_5
28 BUSY_5
28 PRNACK#_5
28,29 PD[7..0]
CRT I/F
DAC_RED 8
DAC_GREEN 8
DAC_BLUE 8
JVGA_HS 13
JVGA_VS 13
CLK_DDC1_5 13
DAT_DDC1_5 13
CRT_IN#_5 13
FDD I/F Signal
28 INDEX#_5
28 TRK0#_5
28 HDSEL#_5
28 DSKCHG#_5
28 FDIR#_5
28 DENSEL_5
28 DR1#_5
XFD_INST# 27
WDATA#_5 28
STEP#_5 28
RDATA#_5 28
WP#_5 28
WGATE#_5 28
MTR1#_5 28
KBC PS/2 I/F
PS2CLK 27
PS2DATA 27
KBDATA_5 27
KBCLK_5 27
USB I/F
USB_0+ 1
L29
2
USBP0P 16
BLM11B221SB
USB_0- 1
L30
2
USBP0N 16
BLM11B221SB
AUDIO I/F
24 LINE_IN_L
24 LINE_IN_R
LINE_OUT_L 24
LINE_OUT_R 24
DOCK CONTROL SIGNAL
15 DOCK_ATTACH#
28 DOCK_ID_EN#
Layout 50mil
USB_VCC
+5VRUN
USB1_VCC
Layout 50mil
LAN+3VAUX
+5VALW
Layout 15mil
AD+_IN
Layout 200mil
BC374 SCD1U
BC37 SC1000P50V
BC35 SCD1U
BC36 SC1000P50V
R18 330R3
R20 0R3-0-U
PCTS1#
DOCK_ID1
PSOUT1
PRI1#
PDTR1#
DOCK_TIP
PE_5
SLCT_5
BUSY_5
PD6
PD7
PD4
PD5
SLCTIN#_5
PD3
PRINIT#_5
PD2
ERROR#_5
PD1
AUTOFD#_5
PD0
STROB#_5
JVGA_VS
CLK_DDC1_5
DAT_DDC1_5
JVGA_HS
DAC_GREEN
DAC_BLUE
DAC_RED
DOCKED#
HDSEL#_5
DSKCHG#_5
WP#_5
RDATA#_5
WGATE#_5
TRK0#_5
STEP#_5
WDATA#_5
MTR1#_5
PDIR#_5
XFD_INST#
INDEX#_5
DENSEL_5
PS2DATA
PS2CLK
KBDATA_5
KBCLK_5
USB_0+
USB_0-
CRT_IN#_5
RJ45_LED_P
LINE_OUT_L
LINE_OUT_R
LINE_IN_L
LINE_IN_R
DOCK_ATTACH#
DOCK_ID_EN#
AUD_AGND
CN18
MLX-CONN240-U1
CRT_VCC
27 PWRBTN#_DK
BC48 SCD1U
Layout 50mil
POWER CONTROL SIGNALS
DOCK ID
DOCK_ID[0..3] 28
DOCK_ID3
DOCK_ID0
MODEM I/F
DOCK_TIP
DOCK_RING
CN6
1
2
CON2-10
Layout 10mil
PRTS1#
DOCK_ID2
PSIN1
PDCD1#
PDSR1#
DOCK_RING
LAN_LED_GN
LANR J45-45
RX-
RX+
TX-
TX+
LAN_LED_YN
R707 75R3
BC700 SC1KP2KV
LAN I/F
TX+ 19
TX- 19
RX+ 19
RX- 19
LAN_LED_GN 19
LAN_LED_YN 19
DOCK Legacy FDD, PS/2 power supplied by CRT_VCC_DOCK
Acer
Acer Incorporated
21F,88,Sec. 1,Hsin Tai Wu Rd.
Hsichih,Taipei Hsien 221.
Taiwan ,R.O.C.
Title
PORT REPLICATOR
Size A3
Document Number
C-Note 2
Rev -3
Date: Friday, January 11, 2002
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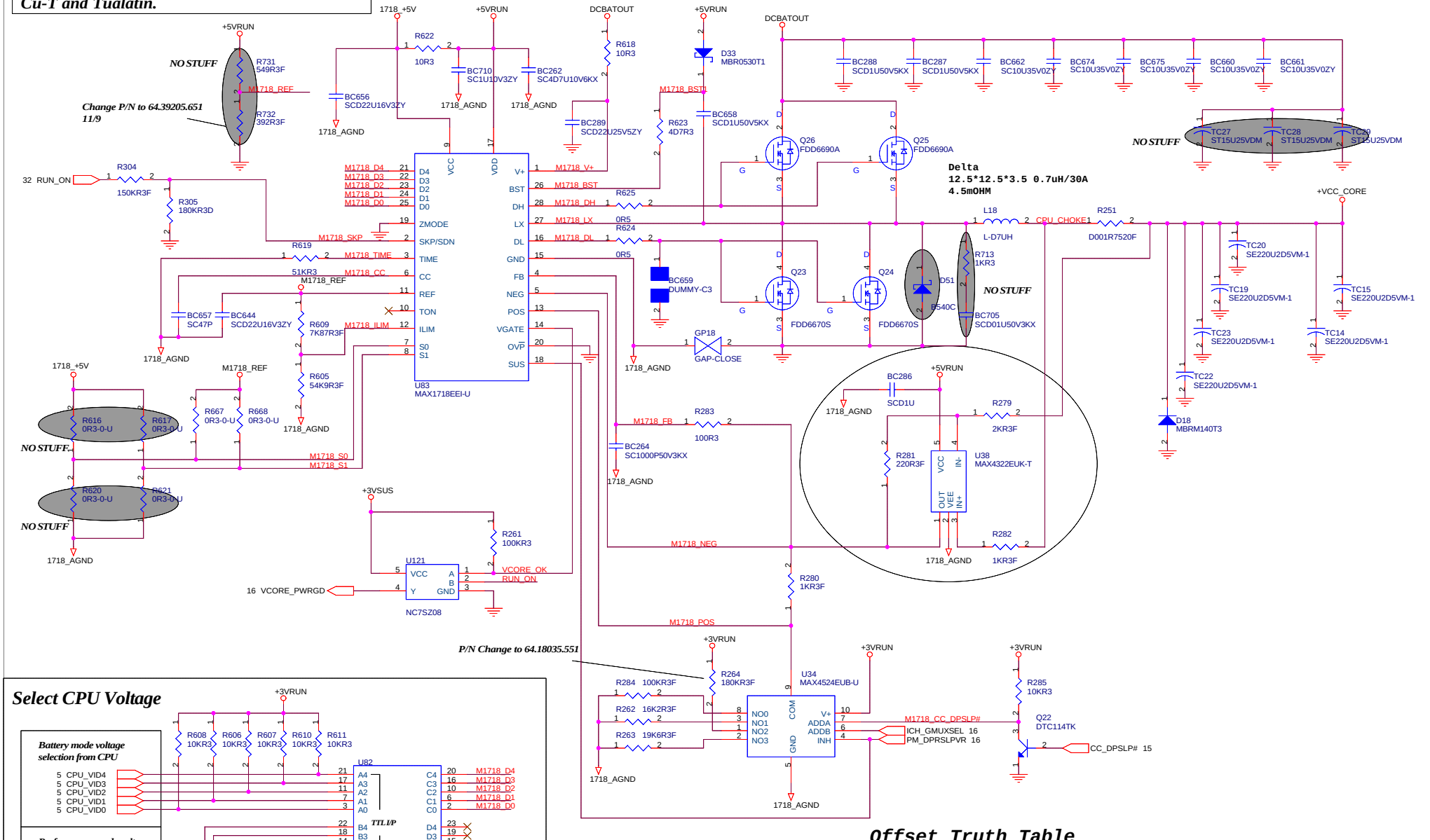
Plz refer to P.2 for the Setting Difference between Cu-T and Tualatin.



Offset Truth Table

PM_DPRSLPVR	CC_DPSLP#	ICH_GMUXSEL	Voffset
1	X	X	0mV
0	0	0	-59mV
0	0	1	-52mV
0	1	0	-29mV
0	1	1	-3mV

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Title: **CPU VCORE**

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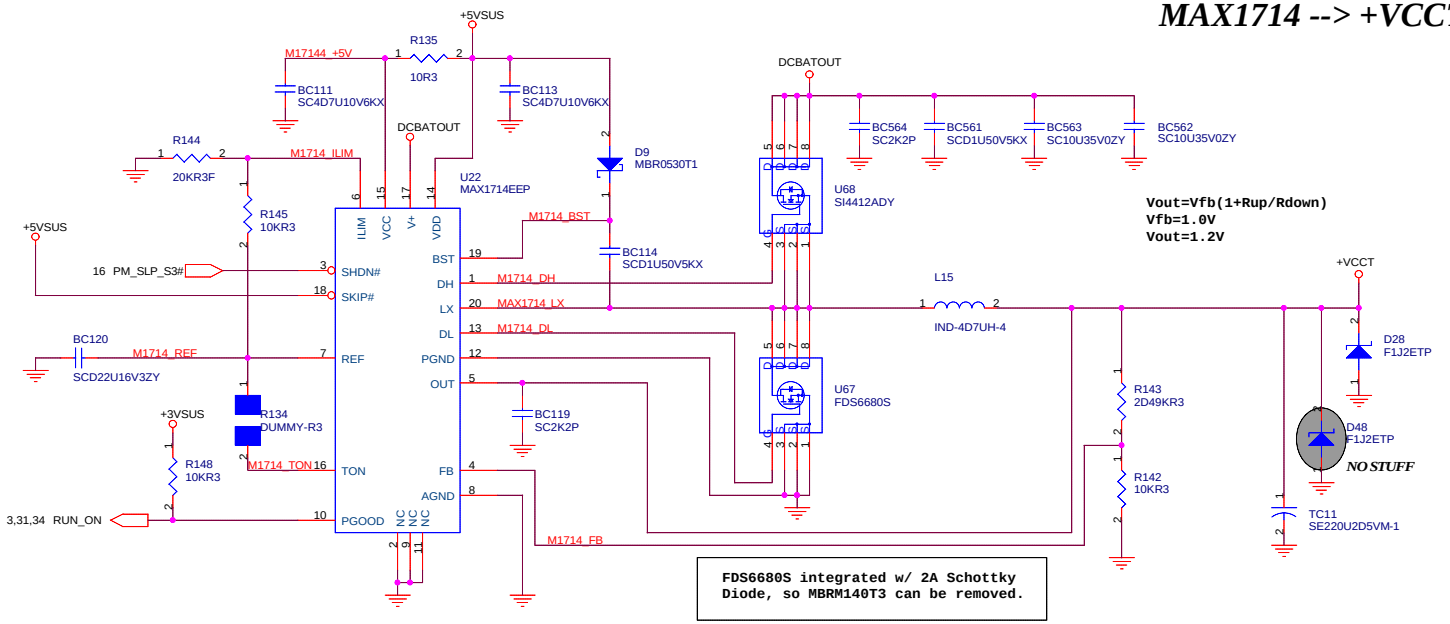
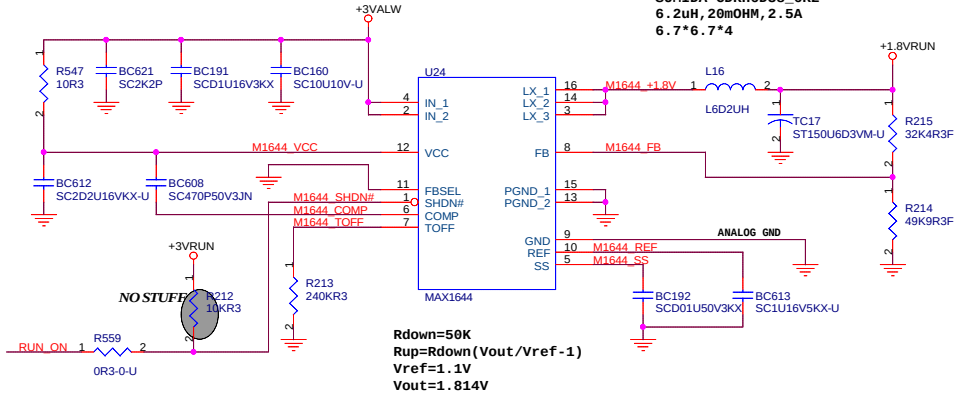
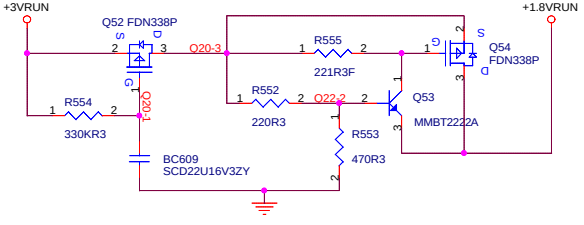
MAX1714 --> +VCCT (CPU_I/O 1.25V)



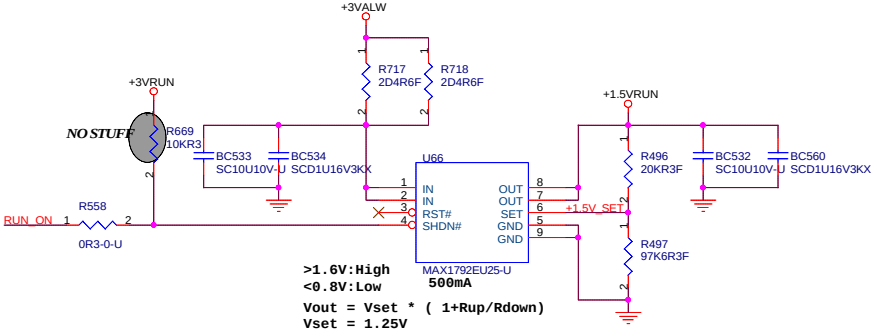
MAX1644 --> 1.8VRUN





To make sure the delta-V between +3VALW & +1.8VALW power plane will not exceed 2V at any time.

MAX1792 --> 1.5VRUN



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Taiwan, R.O.C.

Title: CPUIO 1.25V,1.5V,1.8V

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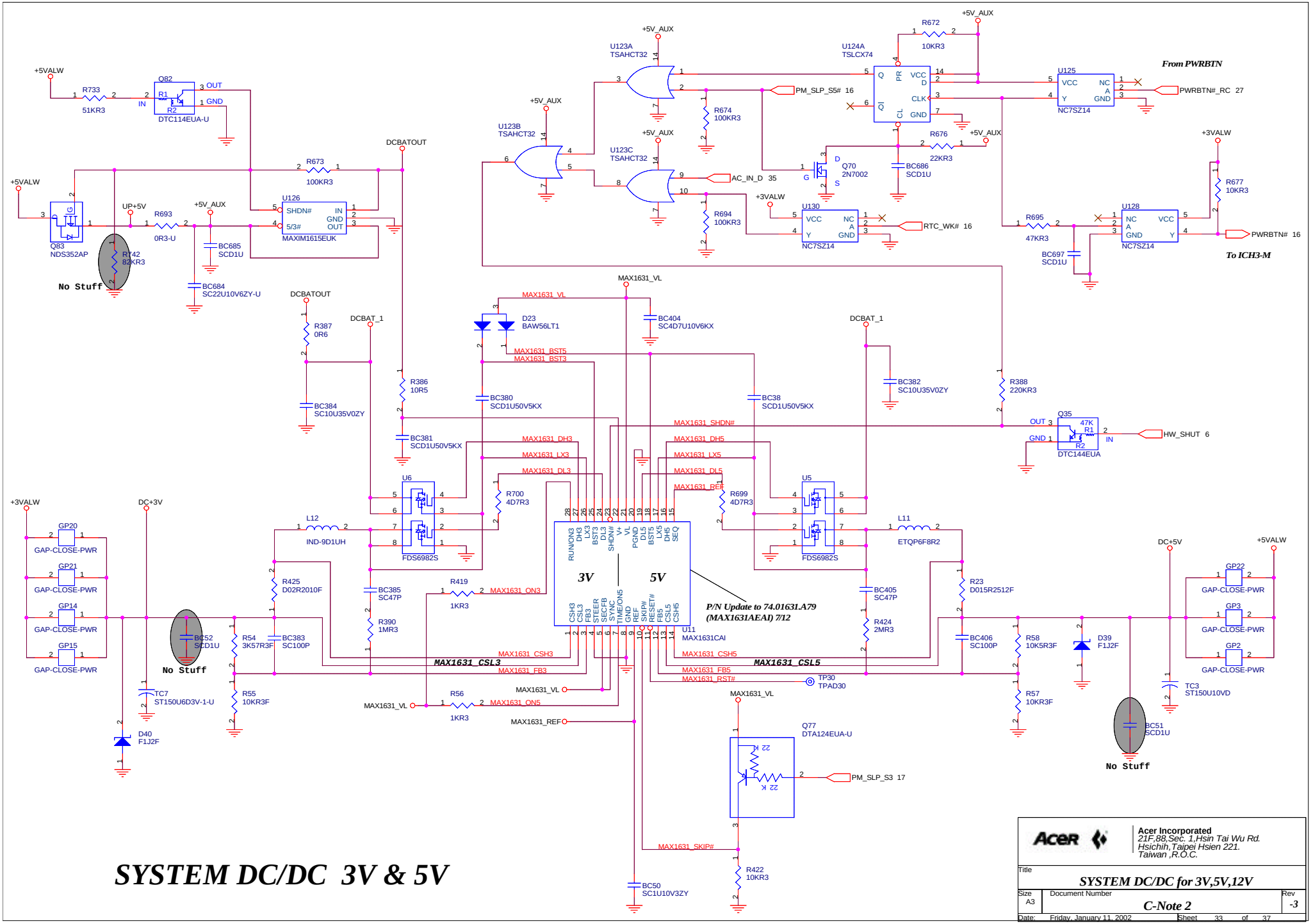
SYSTEM DC/DC 3V & 5V
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Hsichih,Taipei Hsien 221.
Taiwan ,R.O.C.
Title
SYSTEM DC/DC for 3V,5V,12V
Size A3
Document Number
C-Note 2
Rev -3
Date: Friday, January 11, 2002
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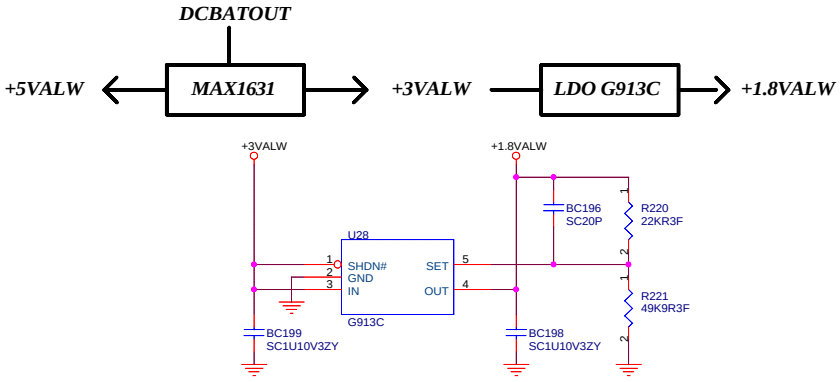
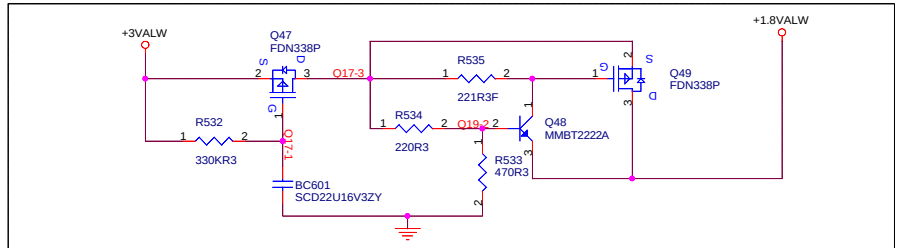
From PWRBTN
To ICH3-M
No Stuff
P/N Update to 74.01631.A79
(MAX1631AEAI) 7/12
MAX1631_CSL3
MAX1631_CSL5
3V
5V
+5VALW
+5V_AUX
+3VALW
DCBATOUT
DCBAT_1
DC+3V
DC+5V
MAX1631_VL
U11 MAX1631CAI
U6 FDS6982S
U5 FDS6982S
U126 MAXIM1615EUK
Q83 NDS352AP
Q82 DTC114EUA-U
Q35 DTC144EUA
Q77 DTA124EUA-U
Q70 2N7002
U123A TSAHCT32
U123B TSAHCT32
U123C TSAHCT32
U124A TSLCX74
U125 NC7SZ14
U128 NC7SZ14
U130 NC7SZ14
D23 BAW56LT1
D40 F1J2F
D39 F1J2F
L12 IND-9D1UH
L11 ETQP6F8R2
TC7 ST150U6D3V-1-U
TC3 ST150U10VD
TP30 TPAD30
PM_SLP_S5# 16
PM_SLP_S3 17
AC_IN_D 35
RTC_WK# 16
PWRBTN#_RC 27
PWRBTN# 16
HW_SHUT 6

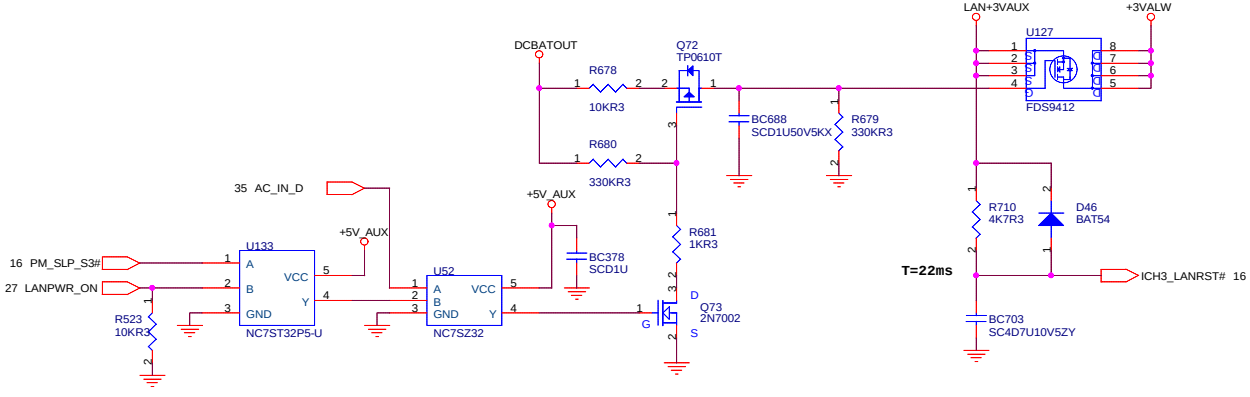
Always Power

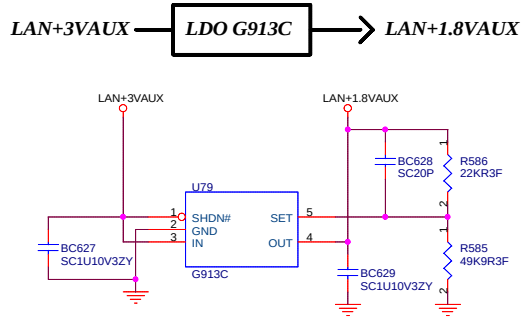




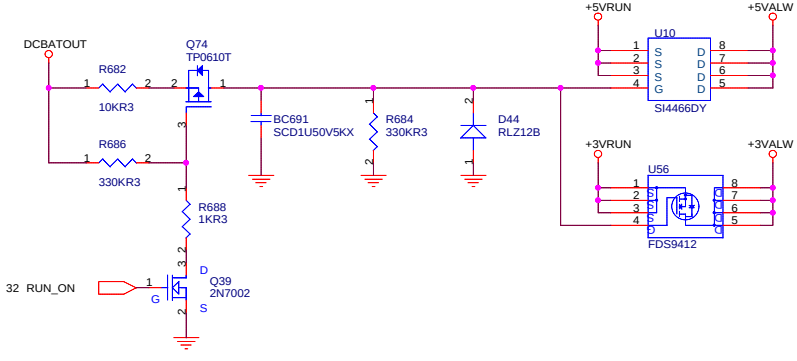
To make sure the delta-V between +3VALW & +1.8VALW power plane will not exceed 2V at any time.

LAN+3VAUX

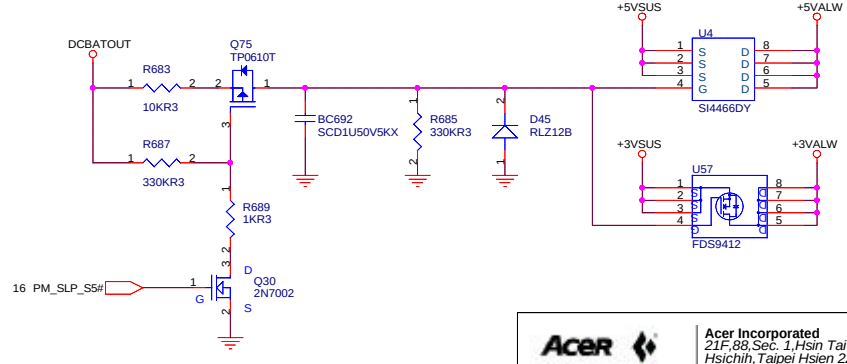




Run Power



Suspend Power



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Title: **PWR PLANE & RESET LOGIC**

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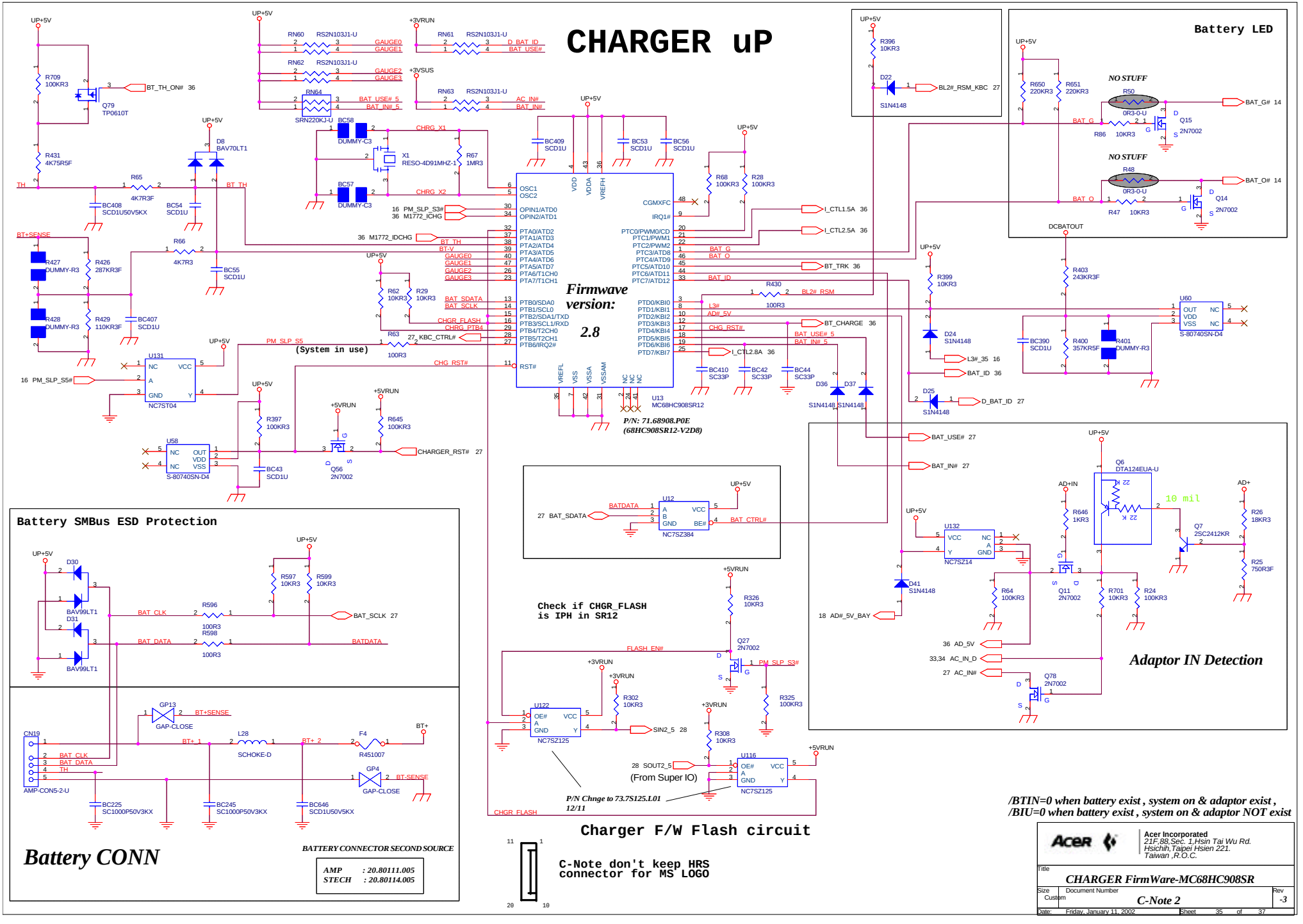
CHARGER uP


Battery LED
Battery SMBus ESD Protection
Battery CONN
Charger F/W Flash circuit
Adaptor IN Detection
Firmwave version: 2.8
P/N: 71.68908.P0E (68HC908SR12-V2D8)
(System in use)
Check if CHGR_FLASH is IPH in SR12
(From Super IO)
P/N Chnge to 73.7S125.L01 12/11
C-Note don't keep HRS connector for MS LOGO
/BTIN=0 when battery exist , system on & adaptor exist ,
/BIU=0 when battery exist , system on & adaptor NOT exist
BATTERY CONNECTOR SECOND SOURCE
AMP : 20.80111.005
STECH : 20.80114.005
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CHARGER FirmWare-MC68HC908SR
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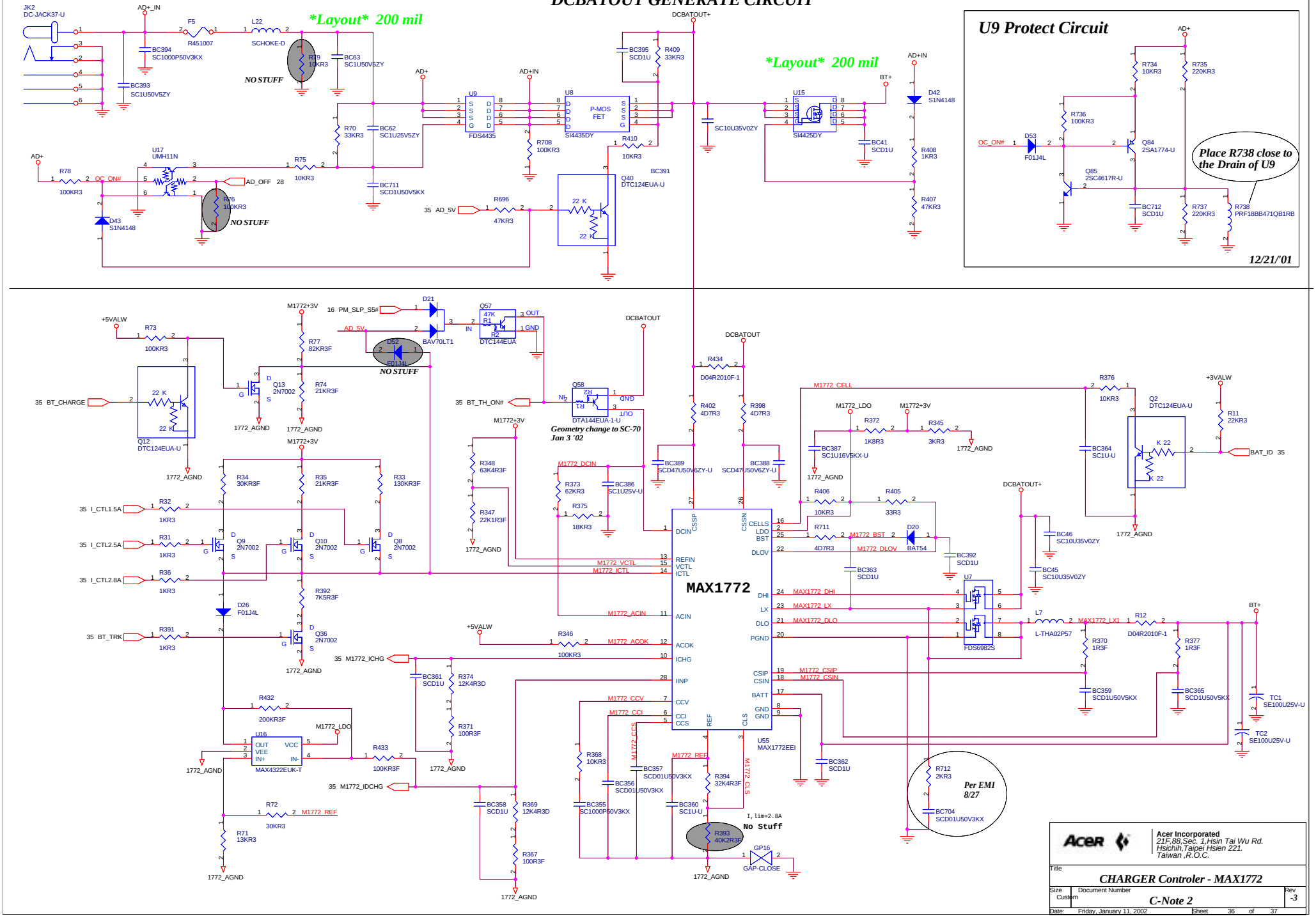
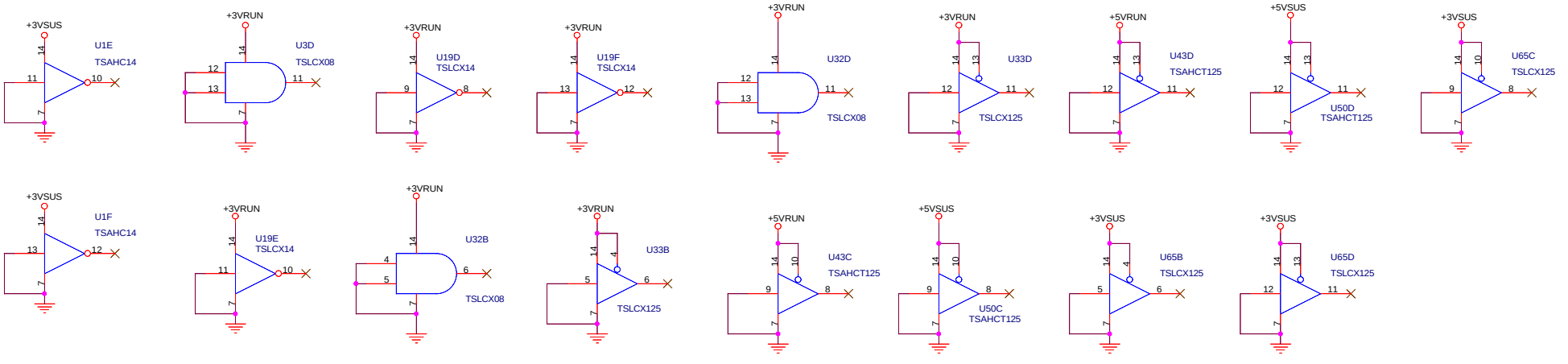
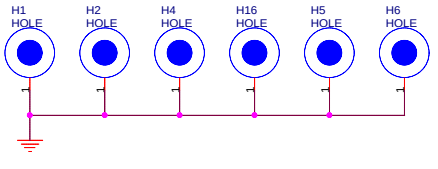
DCBATOUT GENERATE CIRCUIT

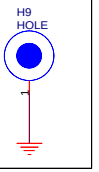


NO USE LOGIC

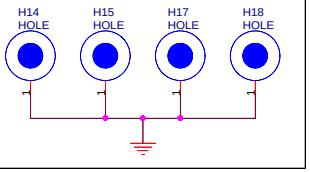




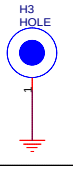
CDC BOSS
34.42G11.001



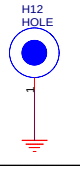
CPU BOSS
34.49G03.001

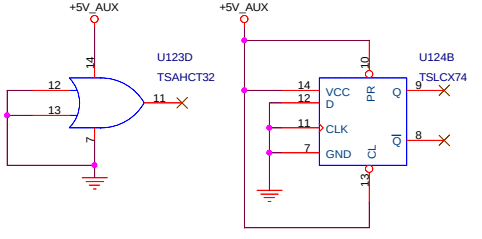


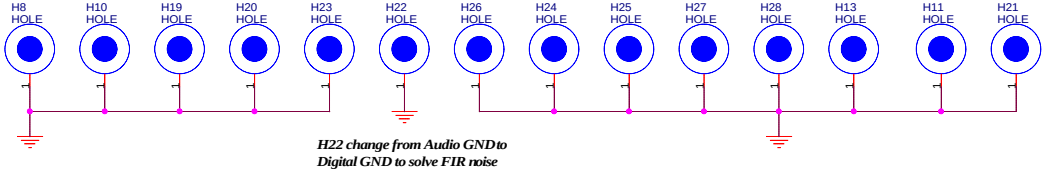
LCD BOSS
34.42G10.001



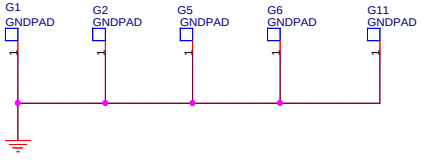
HEAT SINK
34.47R08.001



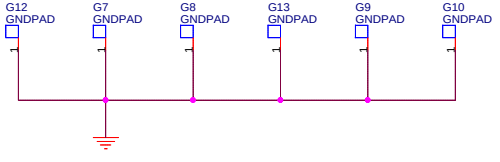




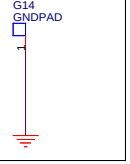
H22 change from Audio GND to Digital GND to solve FIR noise Jan 04 '02



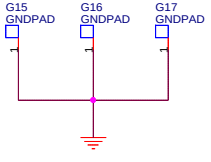
EMI SPRING
34.42P26.001



EMI SPRING (LCD)
34.47R27.001



EMI SPRING (DIMM)
34.47R31.001



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Title: ***HOLES, GND PADS & No-use GATES***

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